

Det1 TOF DAQ (pre) Strawman

Tonko Ljubicic (BNL)
June 2022

Geometry

- Barrel
 - 63 cm radius, 2x128 cm length
- Electron Endcap
 - smaller disk; 64 cm radius
- Hadron Endcap
 - larger disk; 85 cm radius
- Total area $\Rightarrow 14 \text{ m}^2$

Channel Count

- **under flux at the moment**
 - strip size 0.5 mm X 1cm [ATHENA]
 - strip size 0.5 mm x 0.3 cm [ECCE hardware proposal]
 - pixel size 0.5 mm x 0.5 mm [assumption in ECCE simulations]
 - or some combination of the above??
 - **from 3-50(!) Mchannels** ⇒ the big unknown
 - should be known “soon”....
- for this pre-Strawman I will assume 0.5 mm x 1 cm
 - but at the end I will show which numbers are sensitive

Fiber Count

- Barrel
 - my assumptions: 5 cm wide staves, each stave 1 fiber \Rightarrow 160 fibers
- Electron (smaller) Endcap
 - maintaining similar channel count per fiber \Rightarrow 30 fibers
- Hardron (larger) Endcap
 - as above \Rightarrow 50 fibers
- total: 240 fibers
- channel count per fiber \sim 13000
- Comment: number of fibers will mostly be determined by the geometry of the readout scheme, mechanics, fiber routing etc and *not* throughput requirements

Rates on the fiber

- Data

- 50 particles per event x 500 kHz x 3 strips per particle x 32 bits per strip / 240 fibers
 - $\Rightarrow \sim 1 \text{ MB/s per fiber}$ [puny]

- Noise

- personal assumption $\rightarrow 1 \text{ kHz per strip}$ x 3M channels x 32bits / 240
 - but also NOTE: noise strongly depends on various discriminator settings so it is somewhat under our control
 - $\sim 50 \text{ MB/s per fiber}$ [dominates the rate but not too bad]

- Total: $\sim 50 \text{ MB/s per fiber}$

- not a problem
- BTW: I will be assuming “conservative” 10 Gbs fiber links towards the Global DAQ PCs



DAQ PCs: Incoming & Processing Side

- *assumption: PCIe Receiver Boards with 24 fibers*
 - ⇒ 10 DAQ PCs
 - BTW: Receiver Boards and DAQ PCs are designed and specced by the Global DAQ Group
 - but under discussions with detector subgroups, naturally
- **processing on the DAQ PCs**
 - 24 fibers x 50 MB/s ⇒ 1.2 GB/s of incoming data into a single DAQ PC
 - not a problem, similar processing rates already exist in e.g. the STAR TPC
 - **noise removal**
 - require hits ~in time with the collision [10x noise rejection]
 - require clusters of at least 2 close strips [10x noise rejection]
 - require close strips to have ~same time [10x noise rejection]
 - total ~1000x rejection
 - noise becomes small and is ignored :-)
 - caveat: synchrotron radiation not included but under investigation
 - **cluster finding for higher precision xy as well as time**
 - final “point” size 16 bytes per particle

DAQ PCs: outgoing to the Event Builders (tape)

- from previous slides:
 - 16 bytes per track x 50 tracks x 500 kHz \Rightarrow 400 MB/s to tape
- add fudge factor of 1.5x \Rightarrow 600 MB/s to tape expected (max)
 - fudge factor incorporates “known” unknowns at this moment
 - note that this *does not depend* on the channel count and all those uncertainties
- perhaps a bit high?

Special Runs

- “pedestal”-like runs to determine various discriminator thresholds
 - proposal: done “privately” using “private” (non-Global) commands to the TOF FEEs
 - no real involvement from Global DAQ (assumed)
 - apart from a Run Control setup (if that...)
 - will be done “rarely” (once a day, max)
 - results stored on local PCs
 - for efficiency & robustness since they will be constantly used
 - but also in a database provided by Global DAQ for reference and Offline use
- internal pulser runs to determine working channels
 - depends on ASIC functionality
 - otherwise same as above (but even rarer)
- TBD but I don’t foresee any issue here
 - nor do I expect any large involvement from the Global DAQ

Timing (a crucial component *expected* from Global DAQ)

- TOF needs a very low jitter EIC clock
 - under deliberation but I'm assuming 50 MHz
 - NOTE: usual LHC ASICs use the unfortunate 40 MHz but we assume that the EIC-specific EICROC ASIC will be able to handle 50 MHz (*but not 100 MHz*)
 - TOF FEEs will house clock cleaner devices to get to required **~5 ps jitter**
 - TOF is a special case so we assume we *will handle this locally within the TOF electronics sub-group*
- But we also want/need constant phase to the EIC Global clock
 - the collision timing relative to the clock edge is fixed, does not change power-up to power-up
- Question to Global DAQ: will/can this be done and how??

Summary

| | this Strawman | maximum |
|---------------|---------------|----------------------|
| fiber count | 240 | ~500 |
| channel count | 3 M | 50 M [very unlikely] |
| rates/fiber | 50 MB/s | 500 MB/s |
| DAQ PCs | 10 | 30? |
| rates to tape | 400 MB/s | 600 MB/s |