EICROC status and plans

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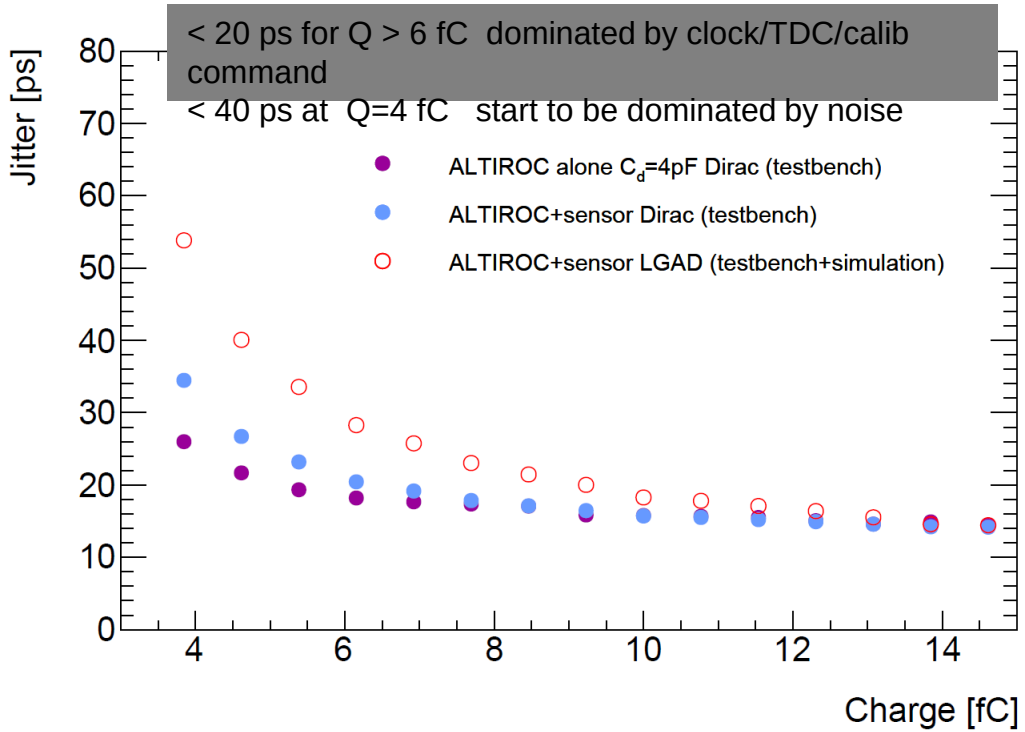
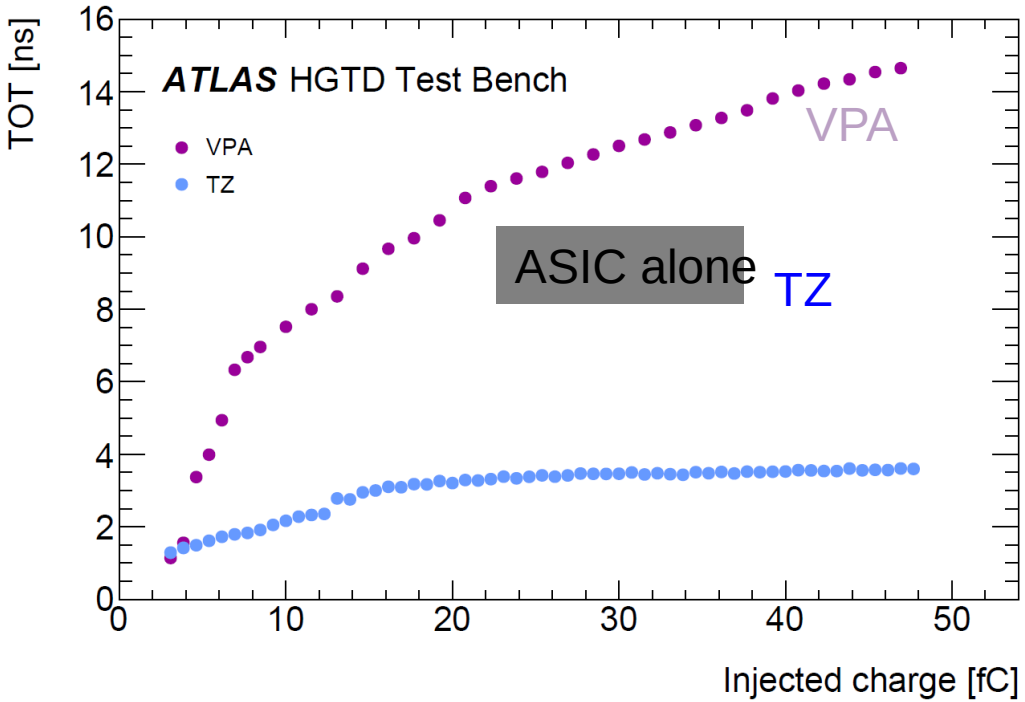
Altiroc1 : ATLAS HGTD LGAD ASIC prototype

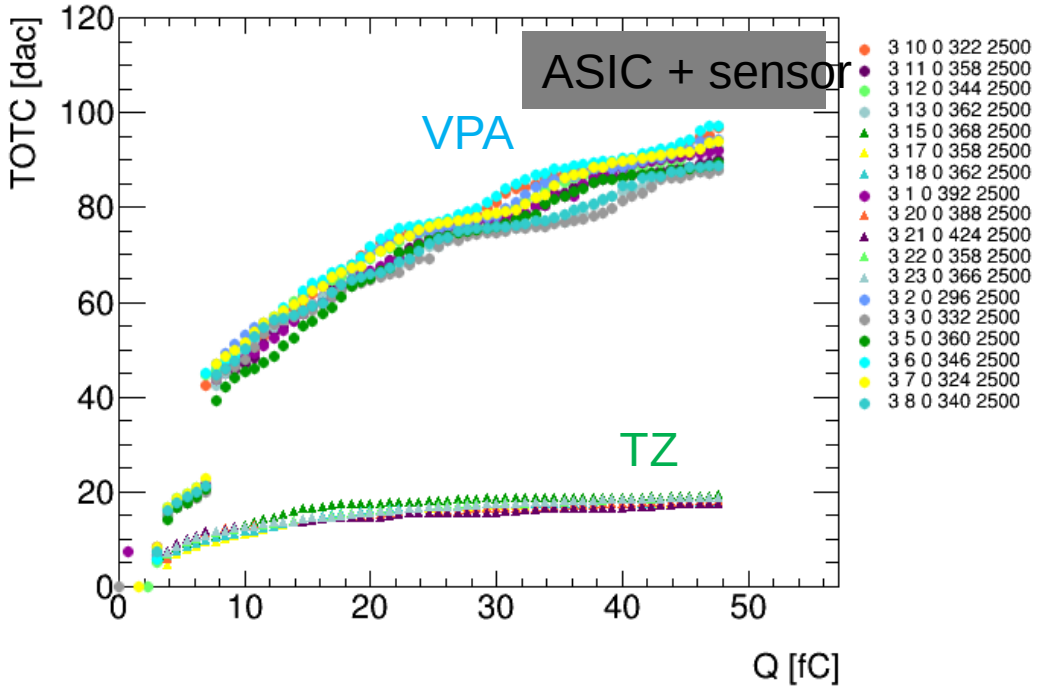
- Altiroc1 prototypes since 2018 , 25 channels (Preamp + discri + TOA and TDC TDS + SRAM) to validate front-end since 2017
  - TDC performance validated
  - TOA jitter performance validated
  - TOT performance : validated with ASIC alone, but still some concern when connected to sensor + HV connection
  - Phase shifter & PLL performance validated
- Altiroc1 bump bonded onto sensors: Very useful to understand system an integration issues



Altiroc1, TOT and time walk validation

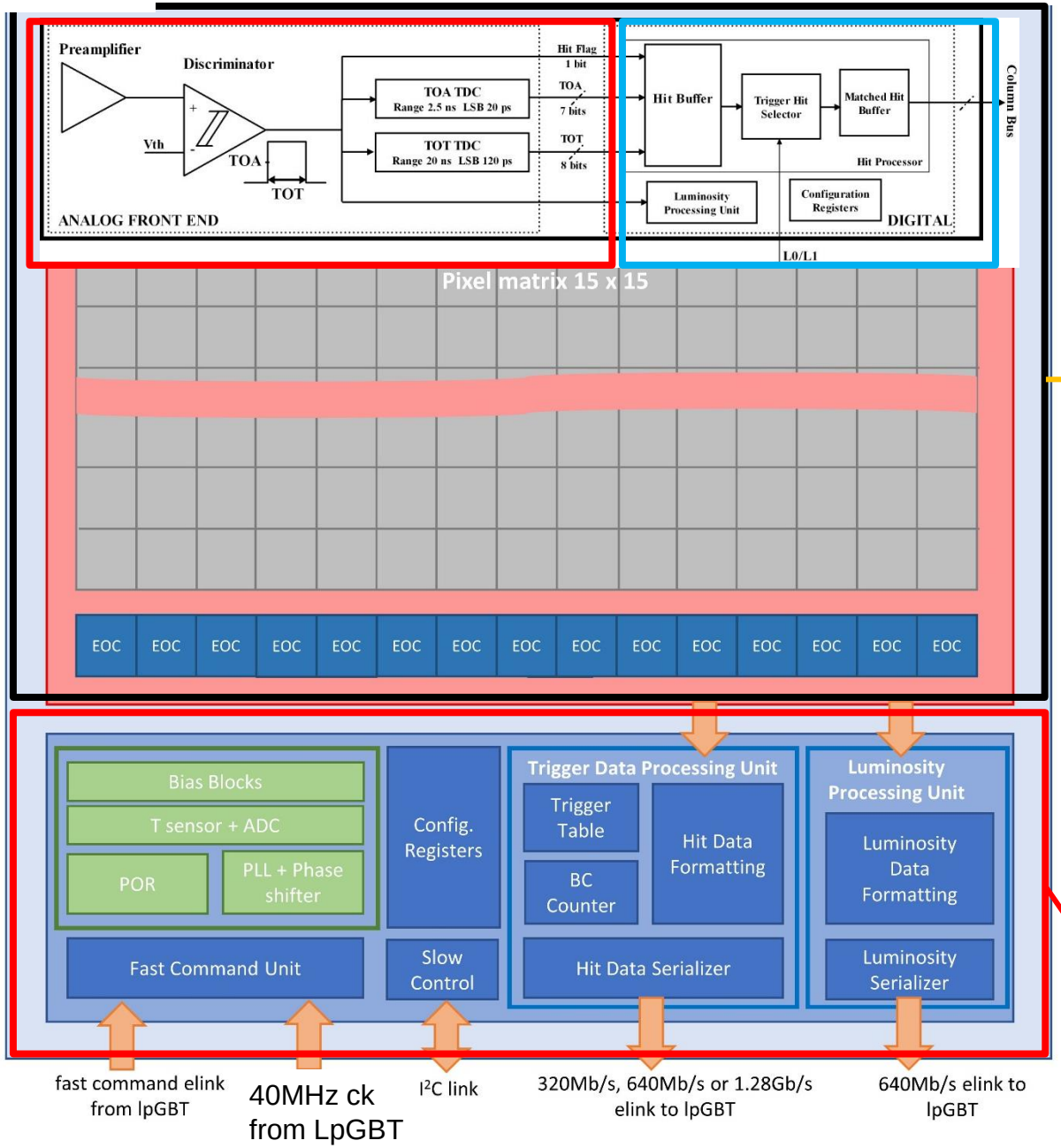
Jitter performance was ok on test bench (see TDR) but no testbeam in 2020 for validation with particles
TOT issue has been further investigated on test bench :

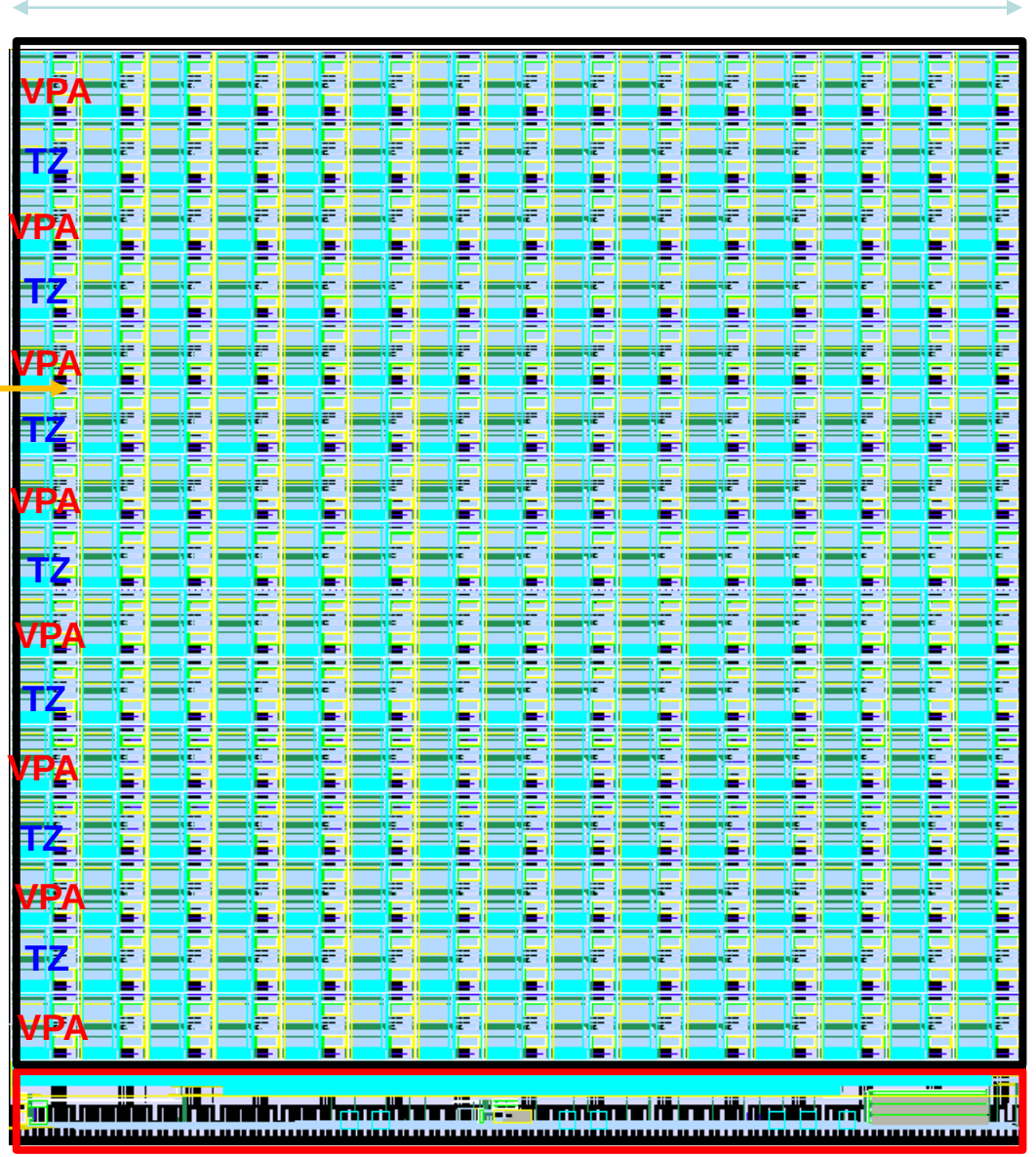




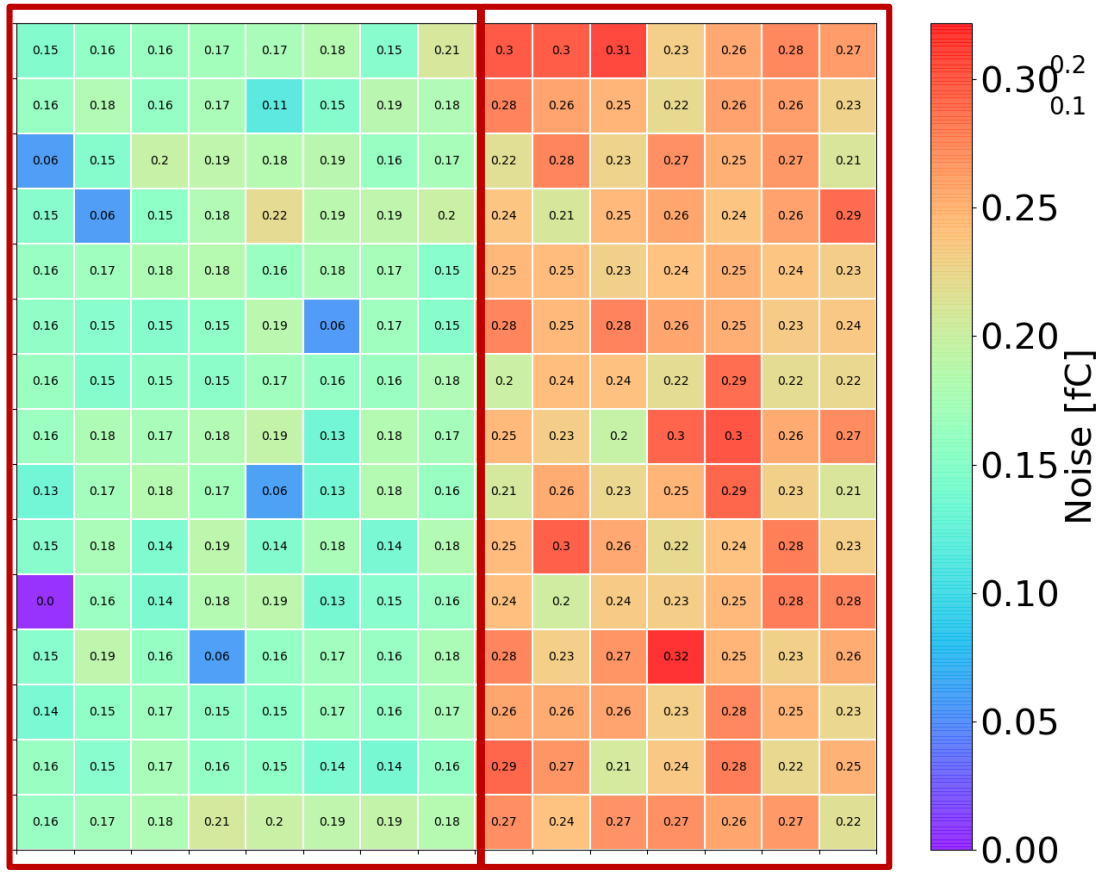
TOT behaviour fine when ASIC alone. It shows small kinks but can be used for time-walk correction
Discontinuities appear when ASIC bump bonded to sensor **AND** Bias Voltage wire-bonded….
Better behavior using Transimpedance preamp (TZ) instead of Voltage preamps (VPA)
=> integration of both preamps types in Altiroc2

Altiroc2 full size ASIC

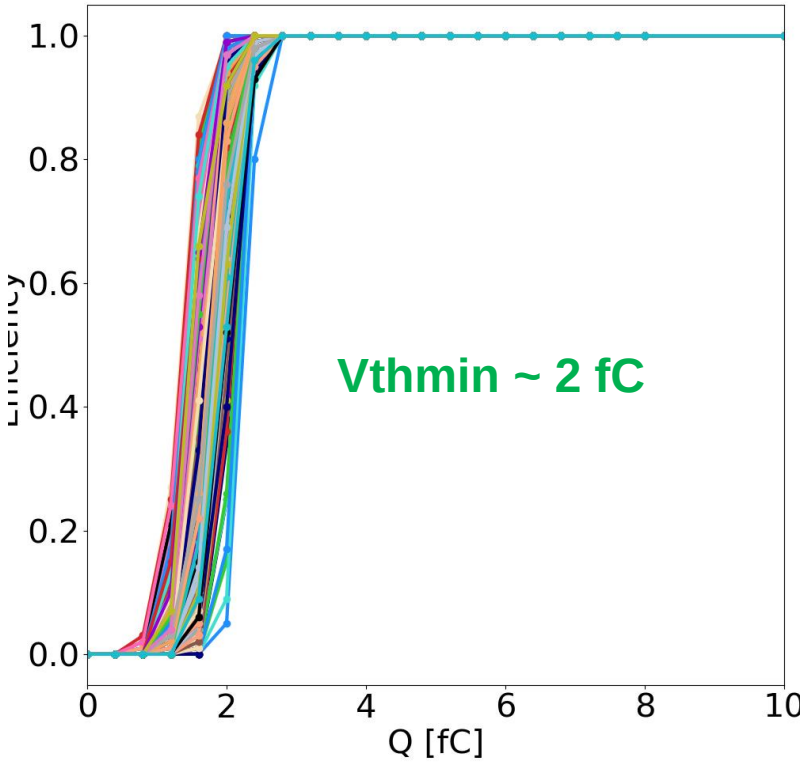


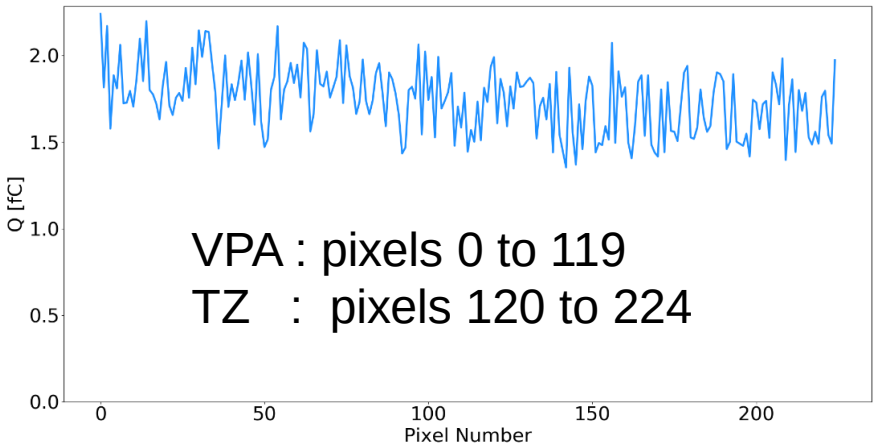


Altiroc2 preliminary measurements: B8 (ASIC alone)



VPA : pixels 0 to 119 TZ : pixels 120 to 224

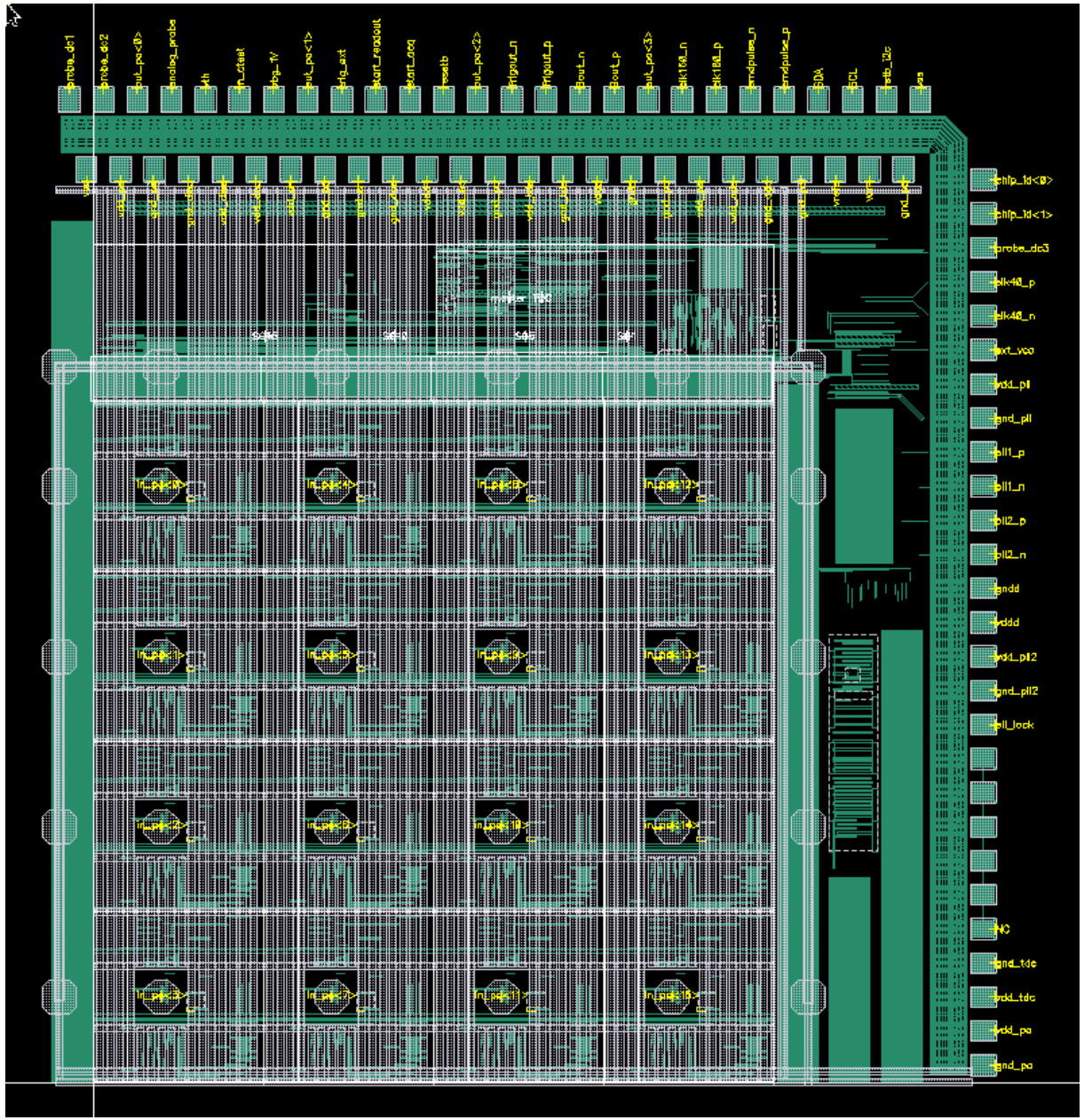




Overview EICROC0

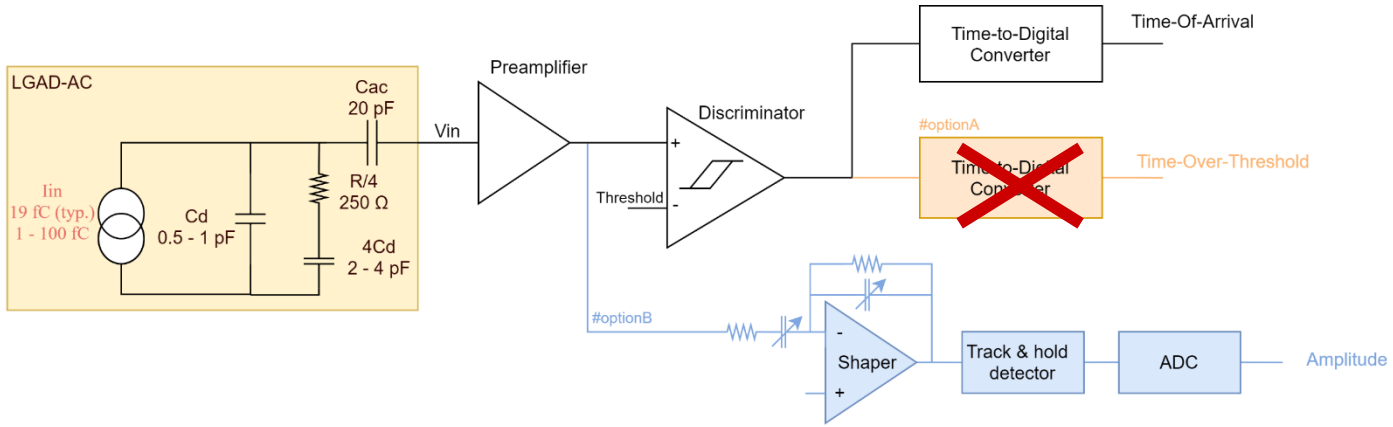
- 4x4 500 um pixels matrix
  - Notice bump pad slightly off-centered by 50um (x=200,y=250)
  - Wire bonds on top only
    - Double row with 100 um pitch. 80um pads
    - 50 um effective pitch
    - *Right side pads for PLL test structures for ATLAS and CMS*

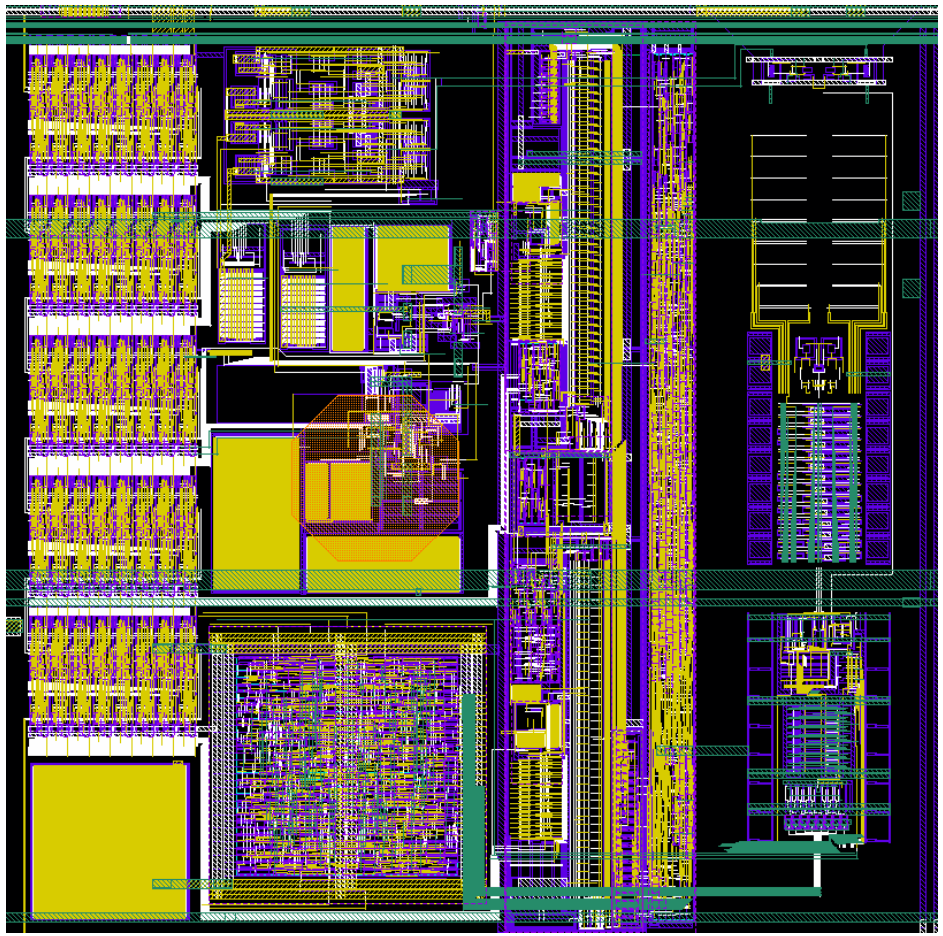
- Sent to fabrication in march 2022
  - Expected back end june/beg july



One pixel

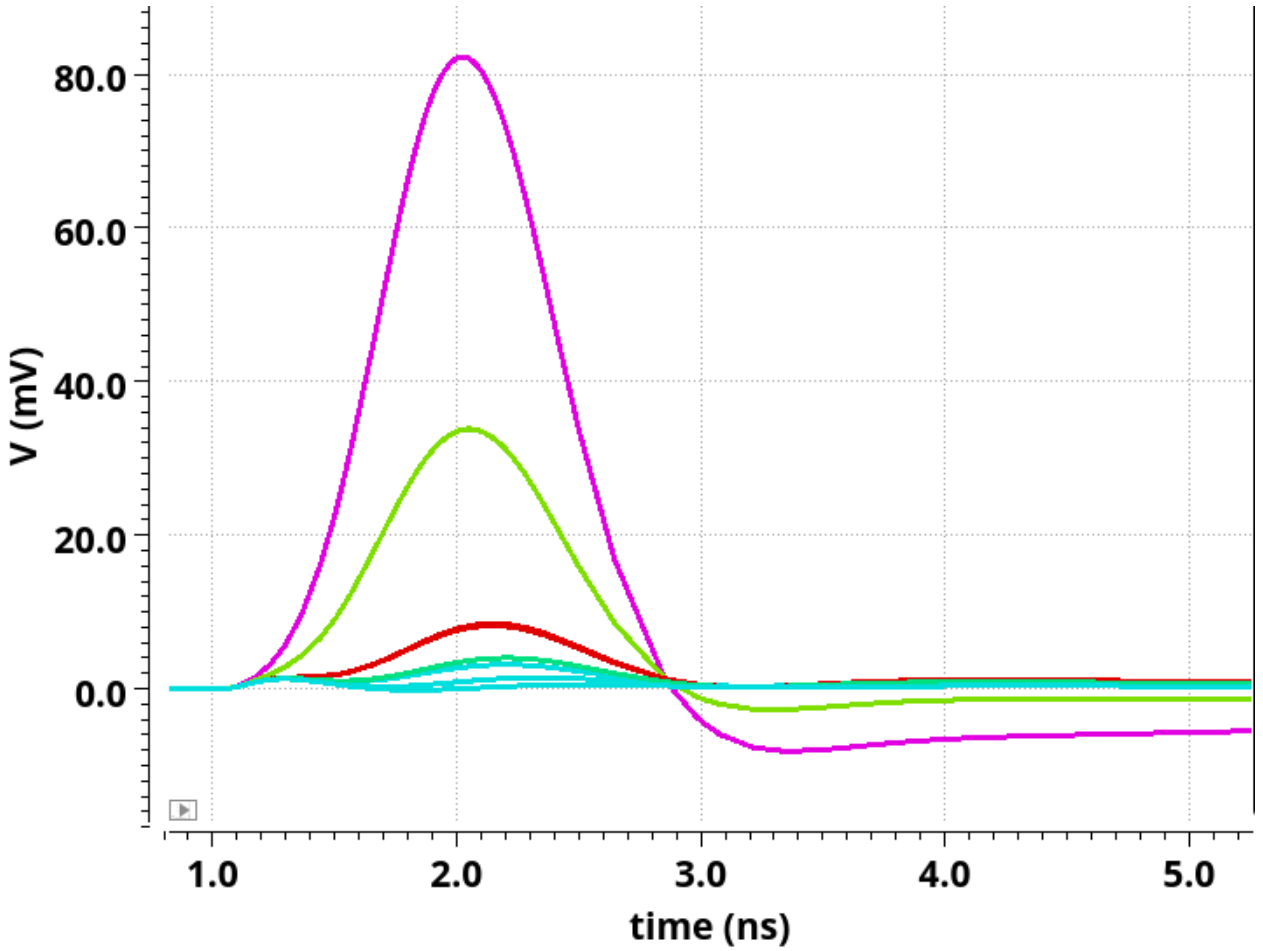
- One pixel design
  - Preamp, discri taken from ATLAS ALTIROC
  - I2C slow control taken from CMS HGCROC
  - TOA TDC adapted by IRFU Saclay
  - ADC adapted to 8bits by AGH Krakow
  - Digital readout : FIFO depth 8 (200 ns)
- 5 slow control bytes/pixel
  - 6 bits local threshold
  - 6 bits ADC pedestal
  - 16 TDC calibration bits
  - Various on/off and probes



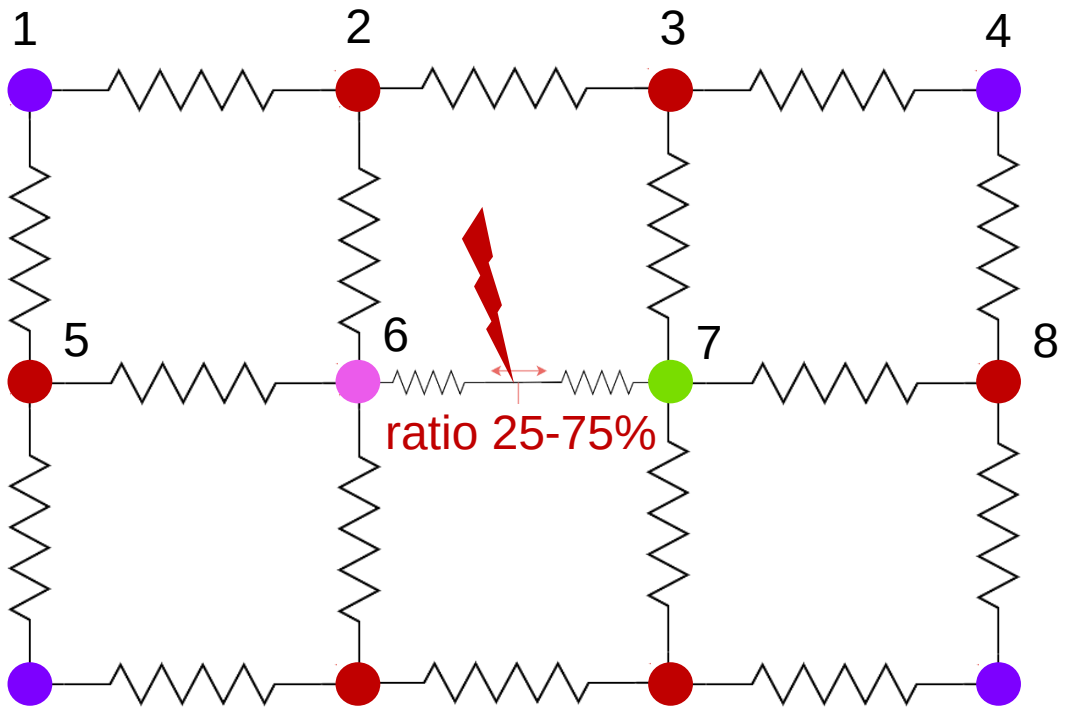


Slow control | PA +discri | TOA TDC | 8b 40M ADC

Preamplifier output signal with 25-75%

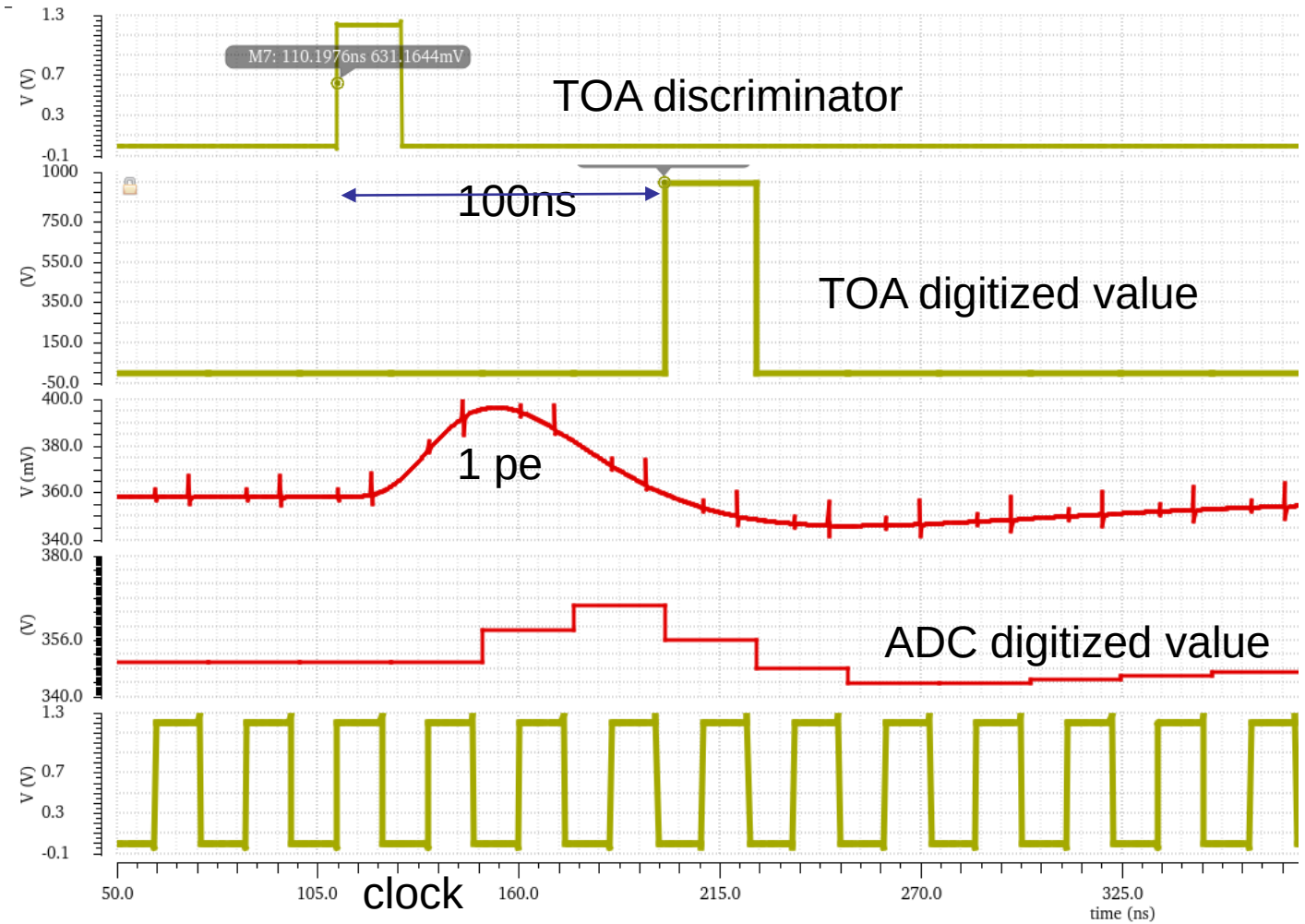


When charge deposition (19 fC) at distance ratio 25-75%



$R_{sheet} = 1\ kOhm$

- Illustration from another (similar) chip

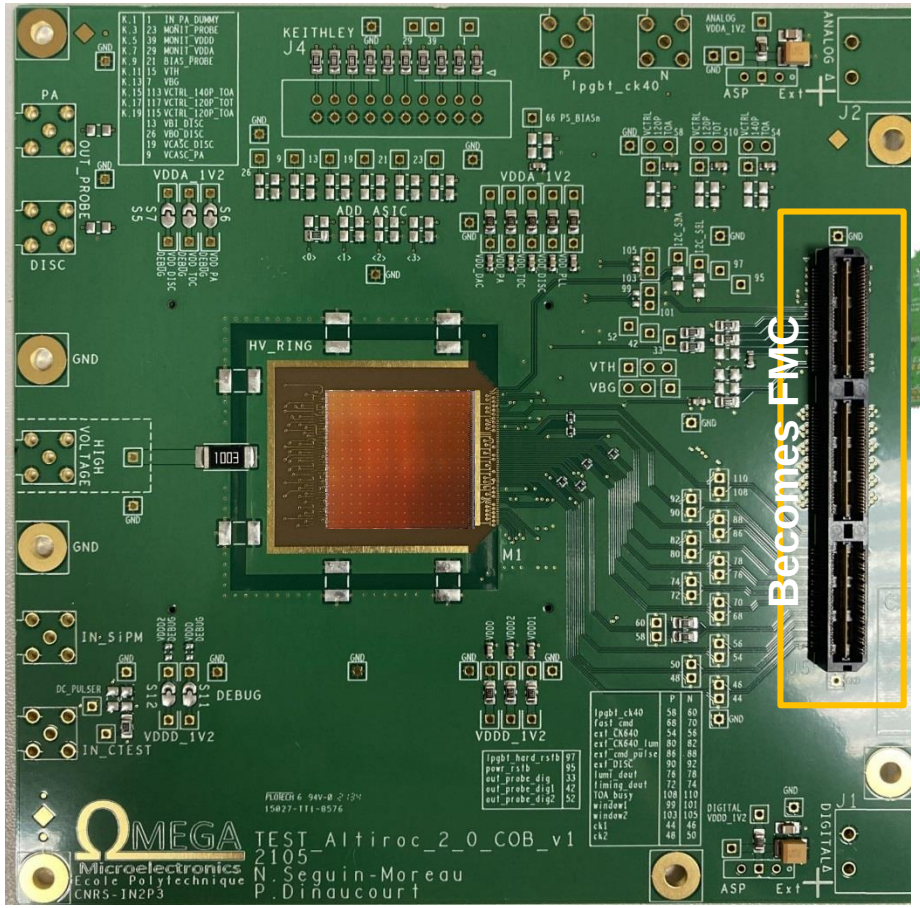


testboard

- Connect to KCU via FMC connector
- Level translators 1.2V – 2.5V
- Space near chip to accomodate sensor
- 4 SMAs for preamps outputs
- On-board regulators for LV

- Wirebonds in 4 rows 200um pitch

- Schematic/layout in progress
- Fabrication mid june



Next steps

- Profit from AIDA engineering run nov 2022 to fabricate EICROC1
- EICROC1 : larger chip to study floorplanning and EIC DAQ
  - Probably with variants of columns to study different low-power front-end and digitization
  - Target 1 mW/ch
  - May also put variants of EICROC0 to test with existing sensors and setup

=> Will come up very quickly, inputs from the collaboration are very welcome