Inputs and updates from EIC SC on technology

L. Gonella on behalf of the EIC EIC Detector 1 Meeting 23 June 2022

Introduction

- The technology chosen for the EIC Detector 1 Silicon Vertex and Tracking Detector is the ITS3 MAPS sensor.
- For the vertex layers, we will adopt the ITS3 sensor and the ITS3 detector concept.
- For the sagitta layers and disks, we will create a smaller version of the ITS3 sensor and develop our own support structures and cooling infrastructure.
- The EIC SC is exploring a number of optimisations of the reference design folding in technology constraints.
- This talk and the talks from Stephen and Ernst will present some of the ongoing studies for the barrel region.
- Please note that nothing is final yet.

The ITS3 sensor and detector concept

• Three layers vertex detector with 0.05% X/X0 per layer.



ALICE

Material budget

→ irregularities due to overlaps

M. Mager | ITS3 kickoff | 04.12.2019 | 6

Material budget



➡ Si only 1/7th of total material			
 irregularities due to overlaps support/cooling 			
emove water cooling			
 possible by reducing power consumption in fiducial volume to <20 mW/cm² 			
emove external data lines + ower distribution			
possible by making a single large chip and that for distribution			
nove mechanical support utside acceptance			
 benefit from increased stiffness by rolling Si wafers 			

Wafer-scale, low power sensor design in 65 nm CMOS technology, thinned and bent around the beampipe.



Table 1: Geometrical parameters of the upgraded ITS.

Beampipe inner/outer radius (mm)	16.0/16.5			
IB Layer parameters	Layer 0	Layer 1	Layer 2	
Radial position (mm)	18.0	24.0	30.0	
Length (sensitive area) (mm)	270	270	270	
Pseudo-rapidity coverage ^a	±2.5	±2.3	±2.0	
Active area (cm ²)	305	408	508	
Pixel sensors dimensions (mm ²)	280×56.5	280×75.5	280×94	
Number of pixel sensors / layer	2			
Pixel size (µm ²)	$O(15 imes15)^b$			

^{*a*} The pseudorapidity coverage of the detector layers refers to tracks originating from a collision at the nominal interaction point (z = 0).

^b For the fallback solution the pixel size is about a factor two larger $(O(30 \times 30) \,\mu\text{m}^2)$.

https://cds.cern.ch/record/2703140/

Stitching for ITS3 sensor

Stitching deployed to design a wafer scale sensor.

Example of stitched wafer layout.



ITS3 stitched sensor

- The ITS3 reticule size is not yet fixed!
- The best value to hit the ITS3 radii is 18.85 mm x 30 mm.



We will NOT change the size of the ITS3 reticule because this requires resources (personnel and time) that we do NOT have.

EIC vertex layers

- Reference detector radii for vtx layers in proposal = 33/43.5/54 mm.
 - These cannot be achieved with the ITS3 reticule size.
 - We now also know for beam pipe bake up we need to be at 36 mm with the 1st layer.



EIC vertex layers

- Option modifying stitching plan of wafer-scale sensor.
 - 2 sensors per layer.
 - L1/2/3 radii = 36/42/48 mm.
 - L1/2/3 active length = 240 mm.
 - 250 mm w/ periphery.

This solution will require more designer time and an EIC specific mask for fabrication of the vertex detector as well \rightarrow more expensive.

• Periphery on one side only, no services in active area.



EIC barrel layers

- Reference detector barrel layers in proposal:
 - L4: R = 210 mm, L = 540 mm.
 - L5: R = 227 mm, L = 600 mm.
- There are various arguments why these layers cannot have the same configuration as the vertex layers and need more conservative support structures and cooling that inevitably increase the material.
 - Stitched, wafer-scale sensor yield.
 - Air cooling and stability of larger structures.
 - Depending on radius, length might exceed 2x max sensor active length (i.e. 54 cm); if more that 2 sensors are needed in z, services need to run along stave, which impacts material.
 - This is the case for the L5 of the reference detector.
- The original estimate by the EIC SC for barrel layers X/X0 is 0.55% X/X0 \rightarrow this number is conservative and very likely to go down.
 - Initial thoughts on what might be possible in Ernst's talk.

EIC barrel layers

• For the barrel layers we will need to create a stitched, large but not waferscale sensor - EIC Large Area Sensor (LAS).



Initial work on disks

- Disks design is challenging to balance low material with full acceptance, down to the beam pipe.
- Various tiling options considered trying to find some common sensor sizes with some different sizes/shape to close around the beam pipe and at disk outer radius.



Work by Ernst Sichtermann

Work by Peter Jones