MPGD tracker frontend alternatives

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Outlook

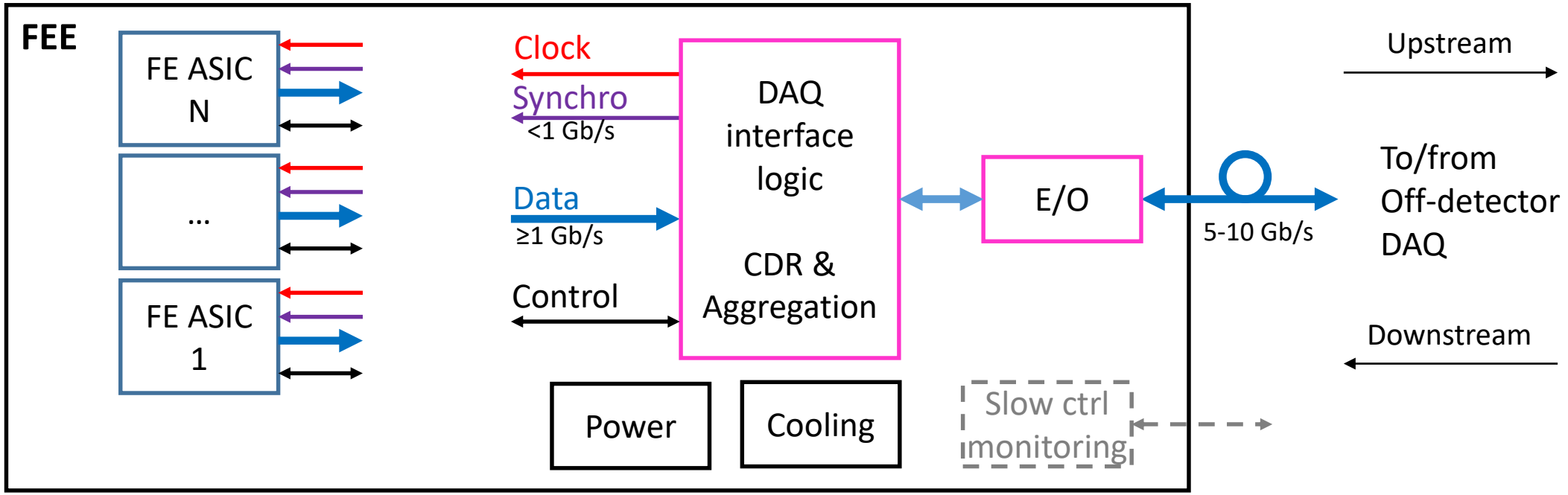
- Some alternatives for frontend organization
- Twinax copper cables
- On-detector VFE and off-detector DAQ interface connectivity
- Summary

Frontend electronics

- Detector-family specific frontend chips
- Common FE-DAQ interface

  → A bi-directional optical link for clock, synchronization (run control), data, configuration

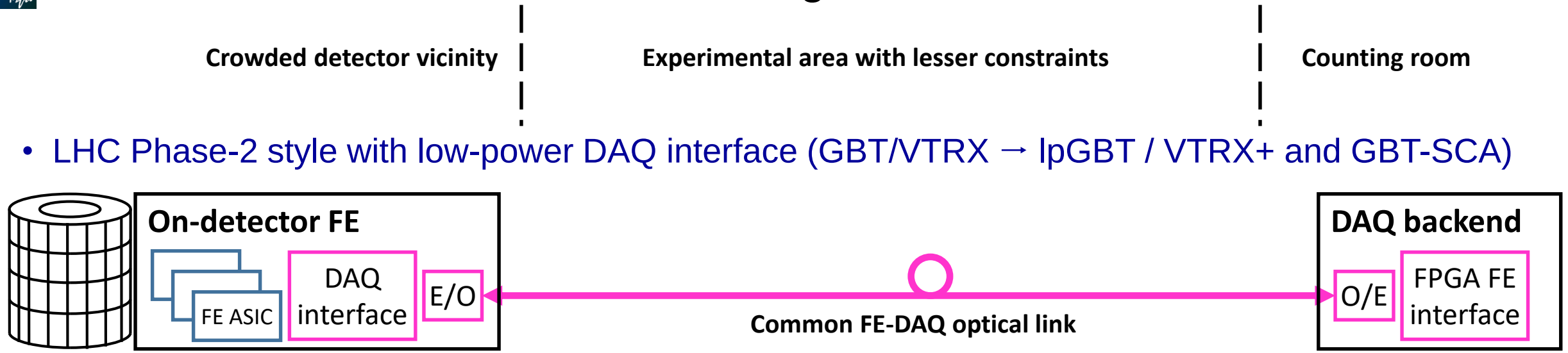
  - Also for slow-control and monitoring, at least partially



- Connectivity between the ASICs and DAQ interface?

  → Few organizational alternatives listed

Frontend organization



- LHC Phase-2 style with low-power DAQ interface (GBT/VTRX → lpGBT / VTRX+ and GBT-SCA)

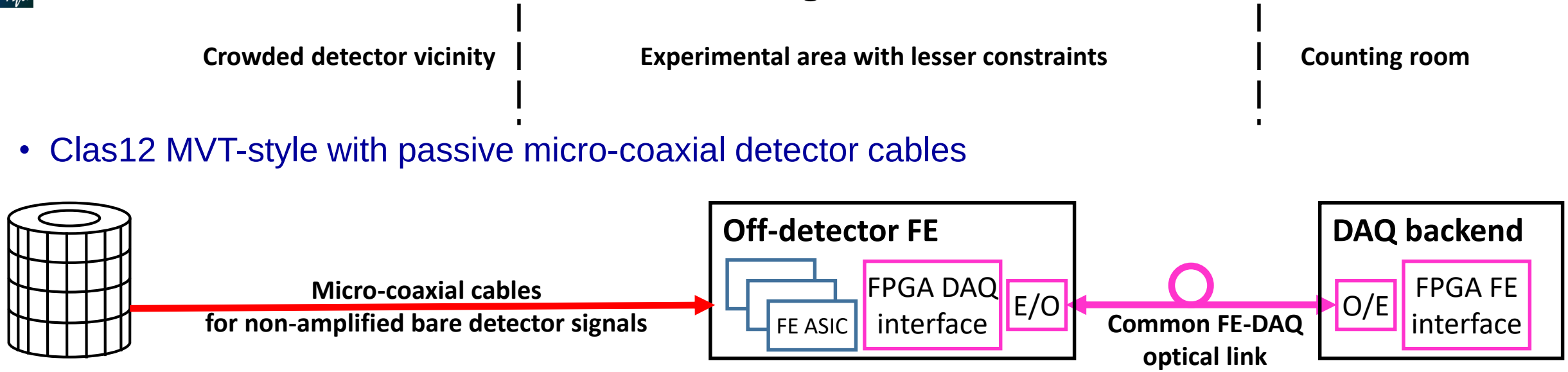
→ Pros:
- Optimal for S/N
- High integration potential
  - Number of channels per DAQ link
- Single type of frontend to be developed and maintained

→ Cons:
- Might be penalizing if implemented with COTS components (FPGA / transceiver)
  - Power (see backup), space, cooling, SEU

→ To be understood:
- Is the commercial component based model acceptable – follow closely eRD104

- For more details see: https://indico.jlab.org/event/519/contributions/9563/attachments/7748/10855/220518_SroX_FrontEnd_IM.pdf

Frontend organization



- Clas12 MVT-style with passive micro-coaxial detector cables

→ Pros:
- Optimal for power/cooling, SEU
- Single type of frontend to be developed and maintained

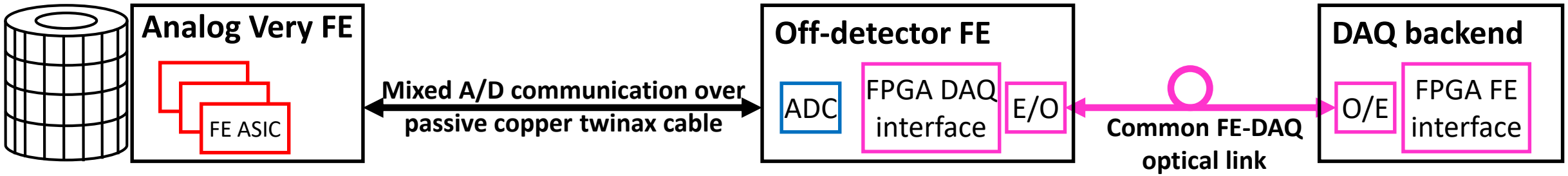
→ Cons:
- Noise due to cable capacitance (50-60 pF/m) + pickup noise
  - Clas12: 40 pF/m Hitachi lightweight cables – not anymore in production
- High number of cables
- Non negligible cable cost

→ To be understood:
- Viability of the solution given the distance between the detector and FE electronics
- For an example see: https://www.sciencedirect.com/science/article/pii/S0168900220300280

Frontend organization: **analog** very frontend

Crowded detector vicinity | **Lesser constraints experimental area** | **Counting room**

- Minimal on-detector analog very frontend electronics with remote off-detector DAQ interface



→ Pros:
- Optimal power/cooling and SEU
- Near optimal for S/N
- Simplest ASIC
- Simplest in downstream communication (*i.e.* I2C, test pulse)

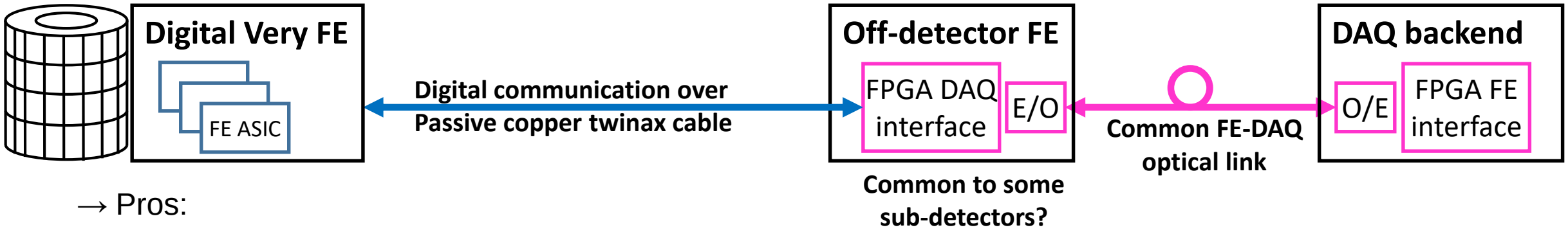
→ Cons:
- Two species of frontends to be developed and maintained
- Large number of bulky copper cables

→ To be understood:
- Acceptable copper cable length for O(300 MHz) bandwidth analog signals

Frontend organization: **digital** very frontend

Crowded detector vicinity | **Lesser constraints experimental area** | **Counting room**

- Minimal on-detector digital very frontend electronics with remote off-detector DAQ interface



→ Pros:
- Optimal for S/N and SEU
- Near optimal for power/cooling

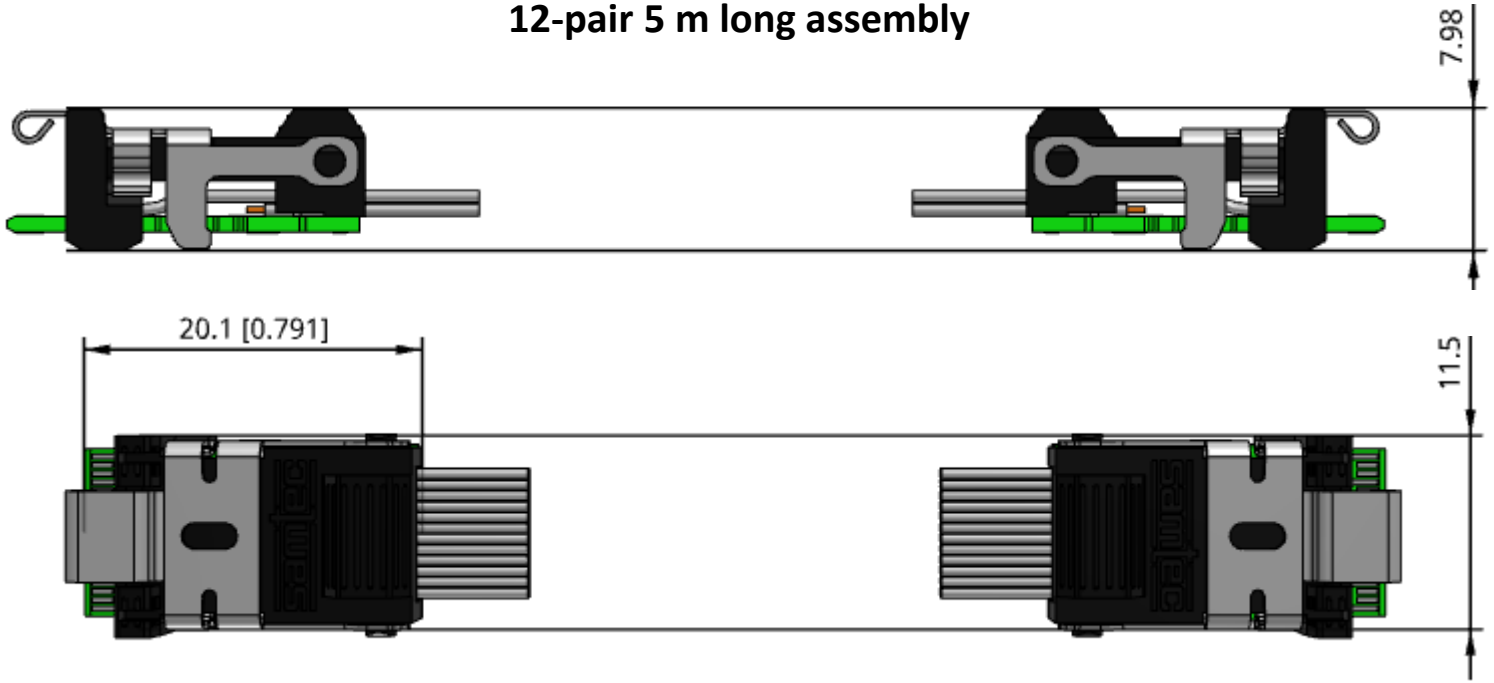
→ Cons:
- Two species of frontends to be developed and maintained
- Copper cables are more bulky than optical cables

→ To be understood:
- Acceptable copper cable length for O(1 Gbit/s) communication speeds
- Number of needed twinax lanes for downstream and upstream communications

Twinax copper cable example: Samtec FireFly

- https://www.samtec.com/products/ecue
- https://suddendocs.samtec.com/catalog_english/ecue.pdf
- Configurable assembly
  - → 8 or 12 pairs
  - → up to 10 m
- Impressive signal integrity figures
  - → Qualified for 10-50 Gbit/s speeds

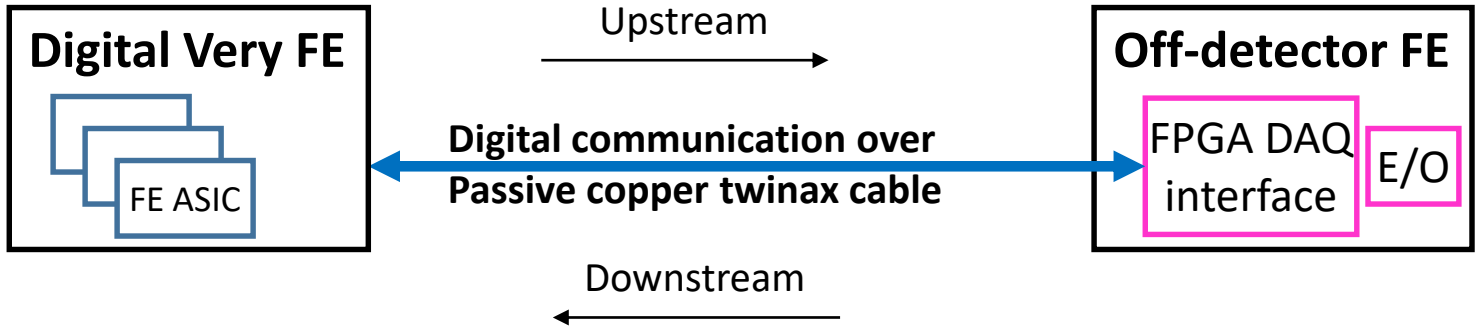
Example of configured part number: ECUE-12-500-T1-FF-01-1
12-pair 5 m long assembly



- Max length for O(1 Gbit/s) speed?
  - → Example in backup
- Rigidity, weight?
- Flammability?
- Cost?
  - → Contact Samtec technical service
  - → R&D on data transmission and on clock / synchronous command distribution?

Very frontend and DAQ interface connectivity

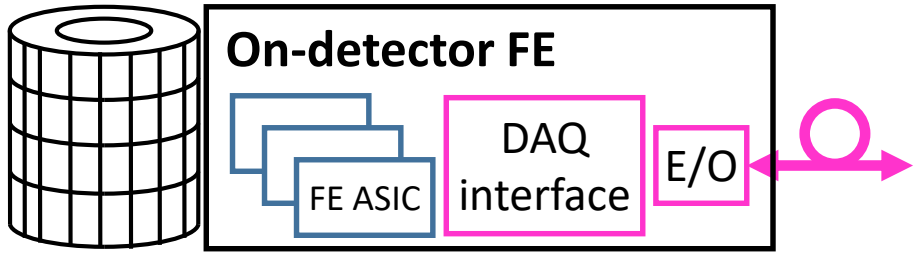
- Downstream
  - → Clock
    - Unique if on-chip clock generation
      - PLL or divider
    - Fan-out to all ASICs
      - See backup
    - Hopefully used for I2C too
  - → Synchronous commands
    - Fan-out to all ASICs
      - See backup
  - → Slow control
    - I2C SDA chain
      - + I2C SCL if a common clock cannot be used
  - → Trigger if not a part of synchronous commands
    - Multi-drop to all ASICs
  - → Test pulse
    - Multi-drop to all ASICs
- Upstream
  - → Acquisition data
    - Point-to-point
    - N ASICs x M output links per ASIC
  - → Slow control
    - If I2C SDA line cannot be bi-directional



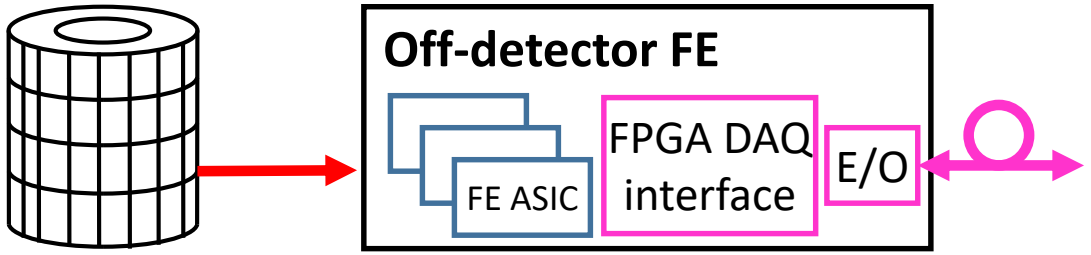
- Optimistic 512-channel FE example
  - → 8 64-channel FE ASIC with
    - 1 Gbit/s output link
    - Unique system clock used for I2C as well
    - Synchronous command encoding trigger
  - → Common on-onboard test pulse logic
  - → Bi-directional I2C SDA
  - → Single 12-pair FireFly interface
    - 3 downstream lines:
      - Clock, command, Test
    - 8 upstream lines
      - 8 data links
    - 1 bi-directional I2C SDA line

Summary

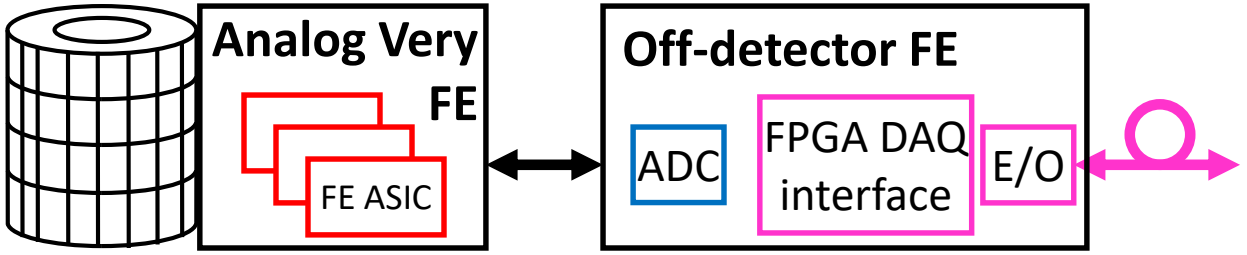
- Fully integrated on-detector frontend can be penalizing
  - → Power / cooling
  - → Material budget
  - → Space
  - → SEU



- Fully integrated off-detector frontend
  - → Will most probably penalize S/N
    - Bare non-amplified detector signals
    - High input capacitance due to long (>3m?) cables
    - Noise pickup
  - → May result in low integration level
    - Large number of detector cables to route-out



- Split analog frontend may penalize
  - → S/N
    - Analog transmission over long cables
  - → Integration
    - Large number of detector cables to route-out



eRD104: follow / collaborate

Summary

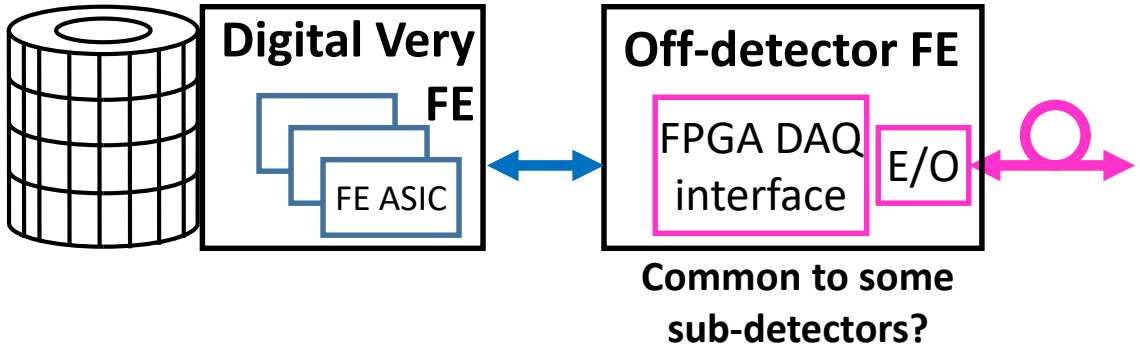
- Split digital frontend

→ Optimal alternative if fully integrated on-detector FE is not viable?

- S/N
- Power / cooling; SEU; material budget

→ Intermediate level of connectivity integration

- Cable count
  - Lower than split-analog or integrated off-detector frontend
  - Higher than integrated on-detector frontend
- FE ASICs with a smaller digital interface are preferable
  - Single clock for acquisition, communication and I2C
  - Single high speed upstream link
  - Trigger being one of the synchronous commands



→ May require companion commercial or ad-hoc ASICs for digital very frontend

- Clock / sync command distribution ASIC
  - See backup
- Bi-directional I2C buffer

eRD104: follow / collaborate

→ The off-detector frontend might be a common development among some of sub-detectors

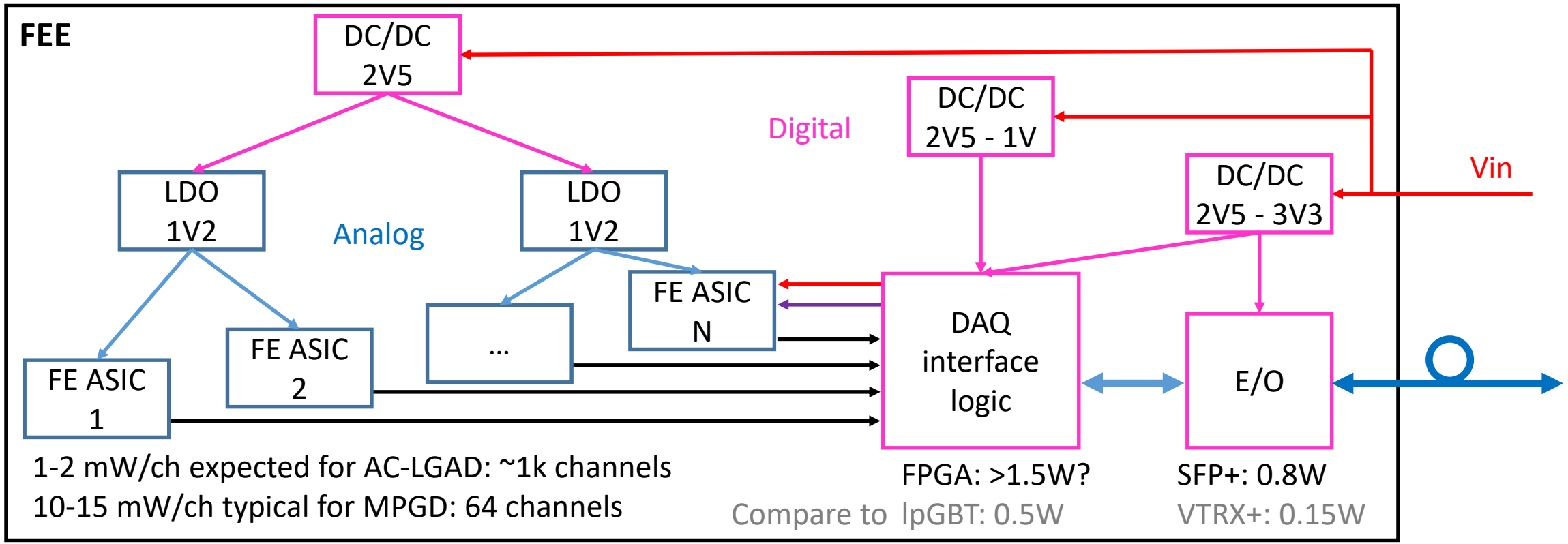
→ A quick R&D to evaluate copper twinax cable performance for considered communication speeds?

- Achievable length for acceptable signal integrity; rigidity; weight; encumbrance; flammability

Backup

Power: is an FPGA-based integrated on-detector FE viable

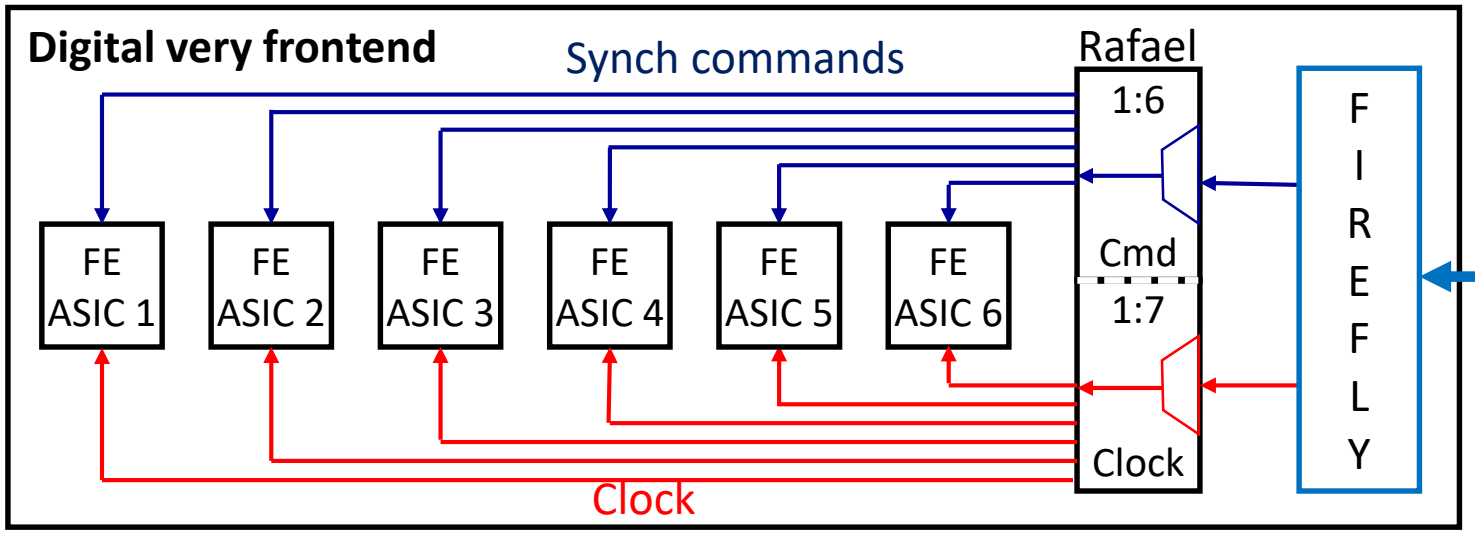
- 1.5 T magnetic field requires efficient power regulation
  - → High efficiency DC/DC converter for digital power
  - → LDO regulators for analog circuitry



  - → Frontend board with MPGD ASICs: 4-8 W + DAQ logic and E/O power
    - 4 – 8 ASICs per frontend; ~1 W per ASIC
  - → Frontend board with AC-LGAD ASICs: ~3 W + DAQ logic and E/O power
    - 2 ASICs per frontend; ~1.5 W per ASIC

Clock and fast command distribution example

- Rafael - Radiation-hArd Fan-out ASIC for Experiments at LHC - developed at Irfu, CEA Saclay
  - → 3 inputs and 13 outputs
  - → CLPS signaling
    - CM voltage: 0.6 V
    - Differential swing: 200-400 mV
    - Programmable drive and emphasis
  - → Single buffer: any input to 13 outputs
  - → Double buffer
    - Input 1 to 6 outputs
    - Input 2 to 7 outputs
  - → Up to 400 MHz and beyond
  - → Low additive jitter of < 2 ps
  - → LHC-level TID, neutron, SEU
  - → 130 nm technology
  - → Possibility to embed a PLL
    - If no jitter cleaner PLL in ASICs



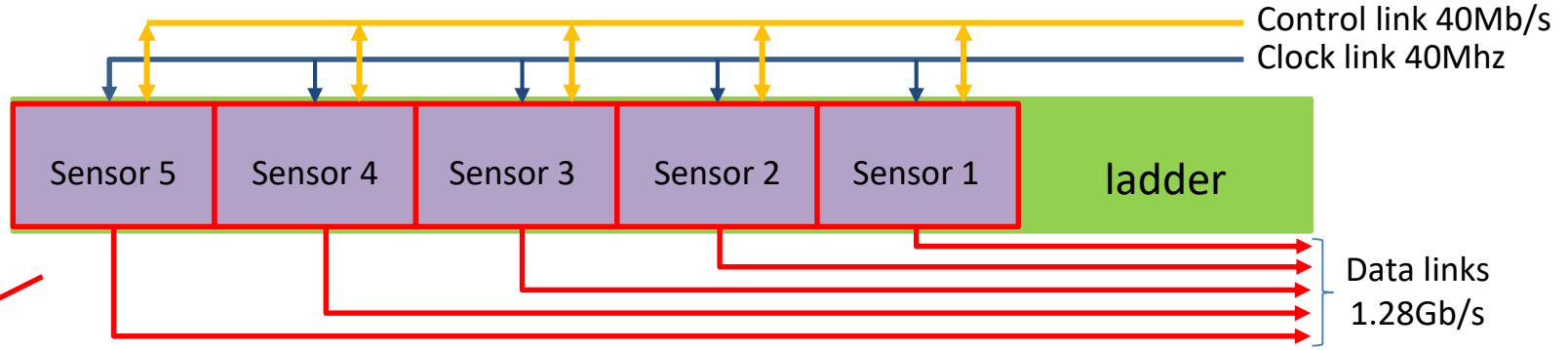
- Commercial counterparts
  - → IDT 8P34S2108: https://www.renesas.com/eu/en/document/dst/8p34s2108-datasheet
  - → TI CDCLVD1216: http://www.ti.com/lit/ds/symlink/cdclvd1216.pdf

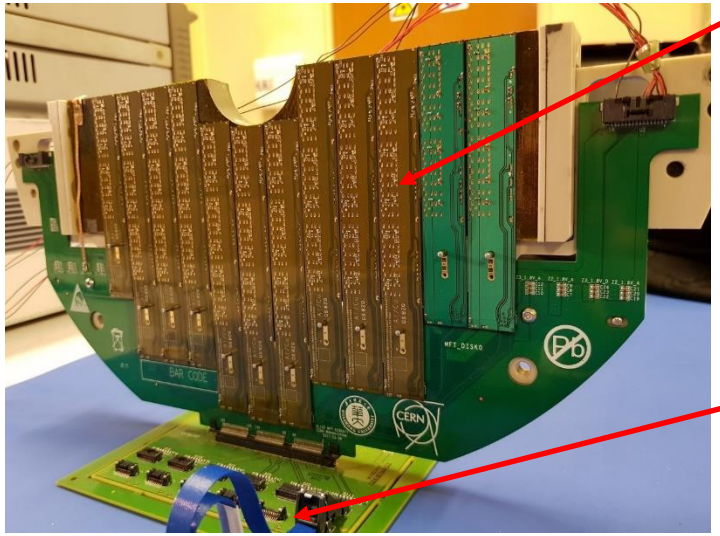
Twinax copper cable performance example: Alice MFT

- Muon Forward Tracker: ladders with a variable number of ALPIDE silicon sensors

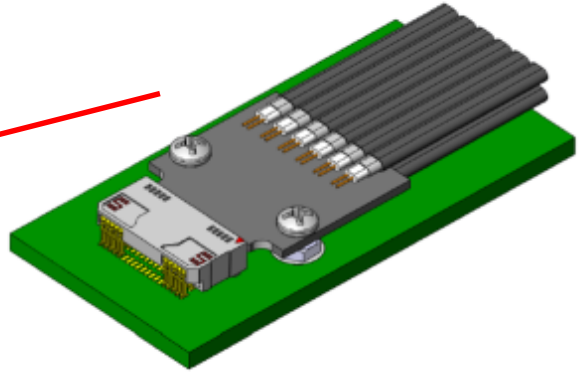
→ ALPIDE sensor: 512K pixels

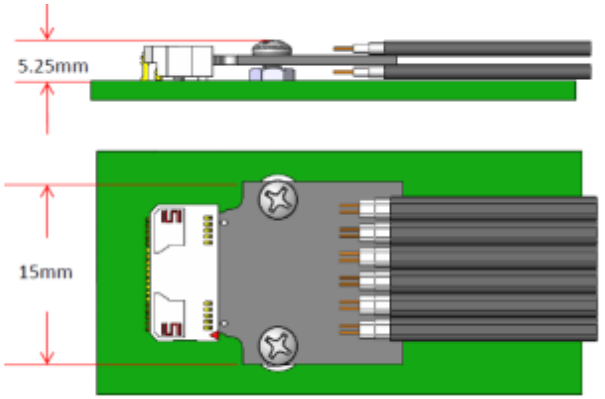
- Pixel = 29 x 27 μm^2
- ZS, triggered or continuous
- 1.28 Gbit/s upstream data link
  - Pre-emphasis capability
- 40 MHz clock
- 40 Mb/s control





Samtec 12-ribbon FireFly twinax cables with low profile connectors





→ Signal integrity studies

- Up to 8m of cable and 9 connectors in the path
- Reliable communication with BER better than 10^{-14}
  - Adjust pre-emphasis