SRO DAQ Options for FPGA-Based Front-End Hardware

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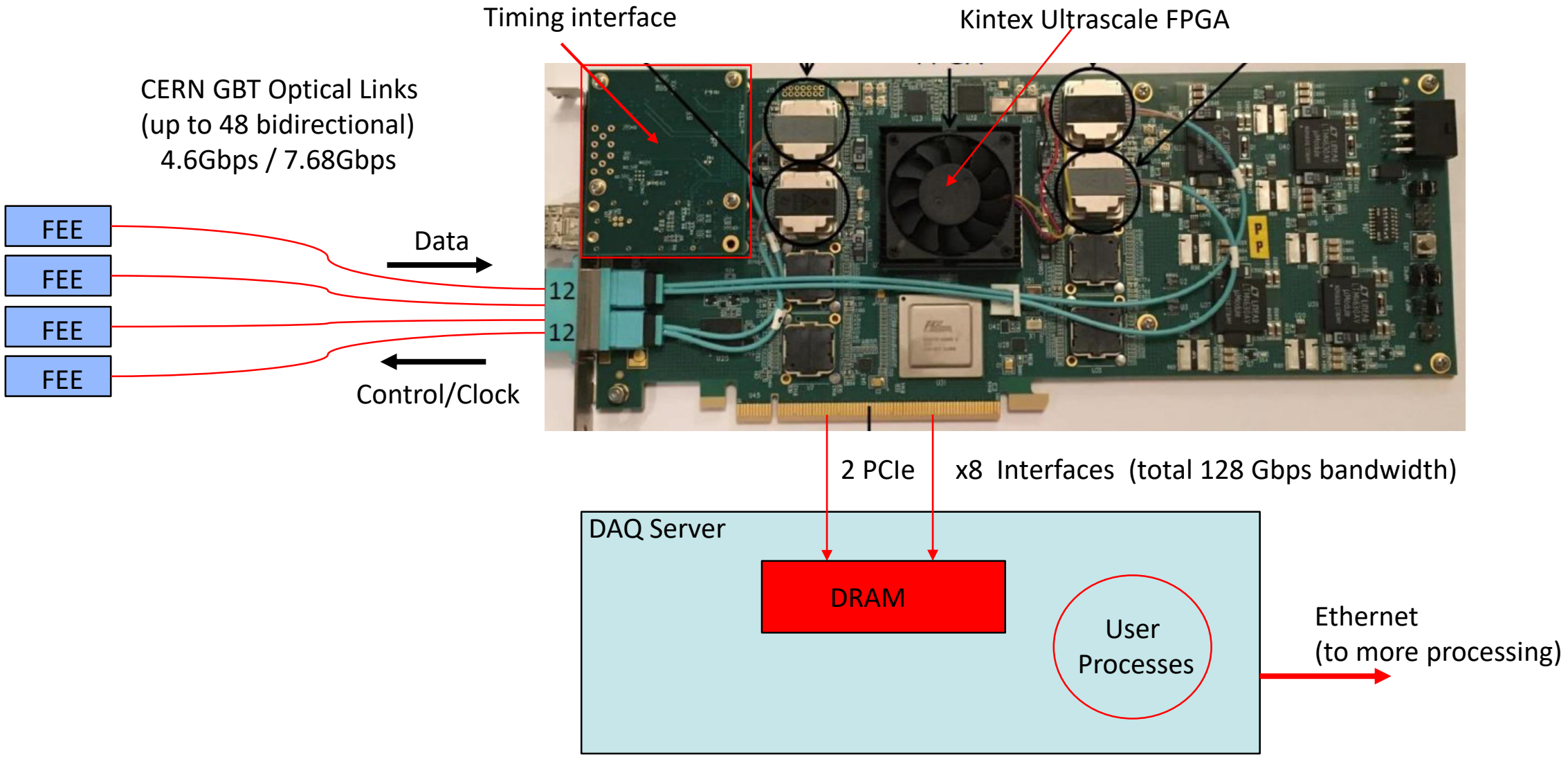
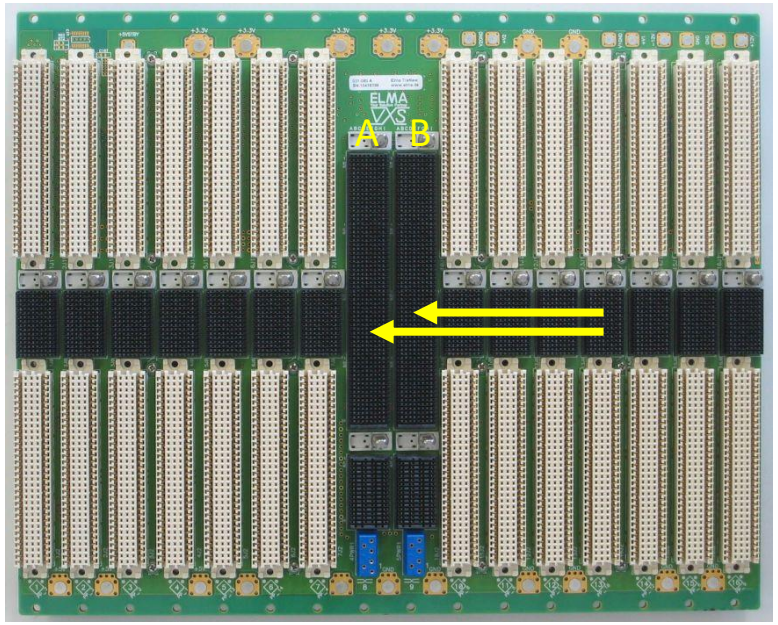
FELIX Hardware



VXS Platform

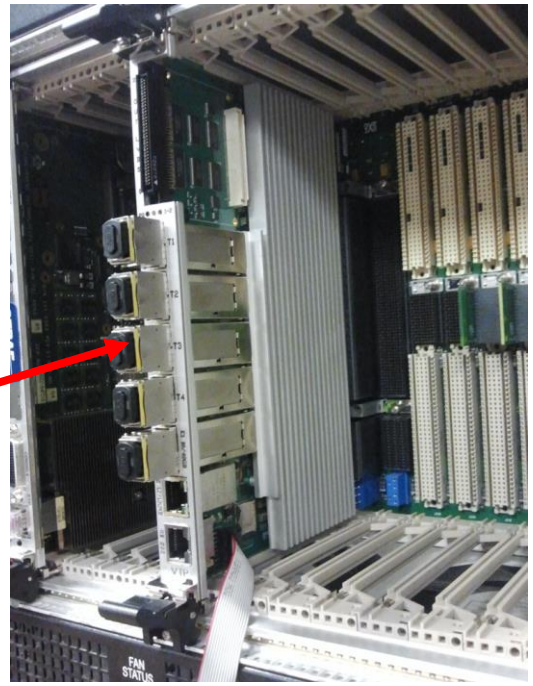


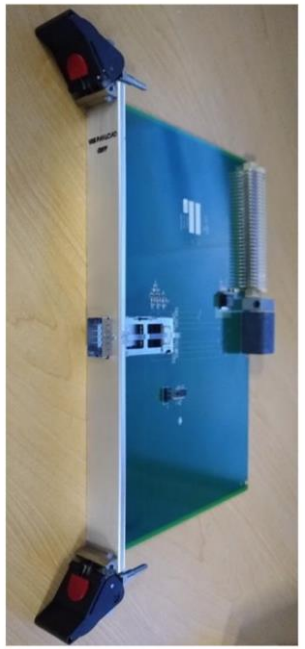
- JLab standardized on this technology for the 12GeV Upgrade
- Originally used for the L1 trigger data path
- Dual Star – switched serial backplane (along with VME)
- Up to 20Gb (4 lanes) from each Payload to the 2 Switch slots (A, B)
- Easy distribution of Trigger or low jitter clock to all modules in the crate.

And there are multiple payload options….

Just need something to manage the system in a Switch Slot:

VXS Trigger Processor (VTP)





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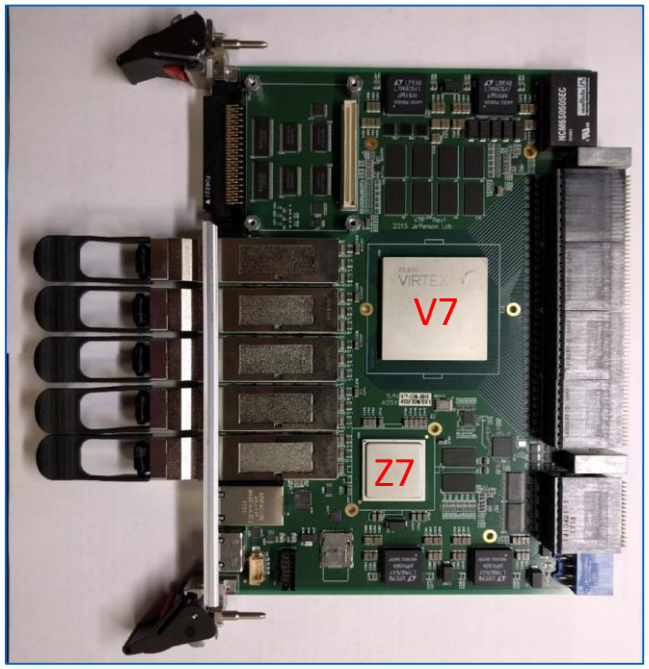
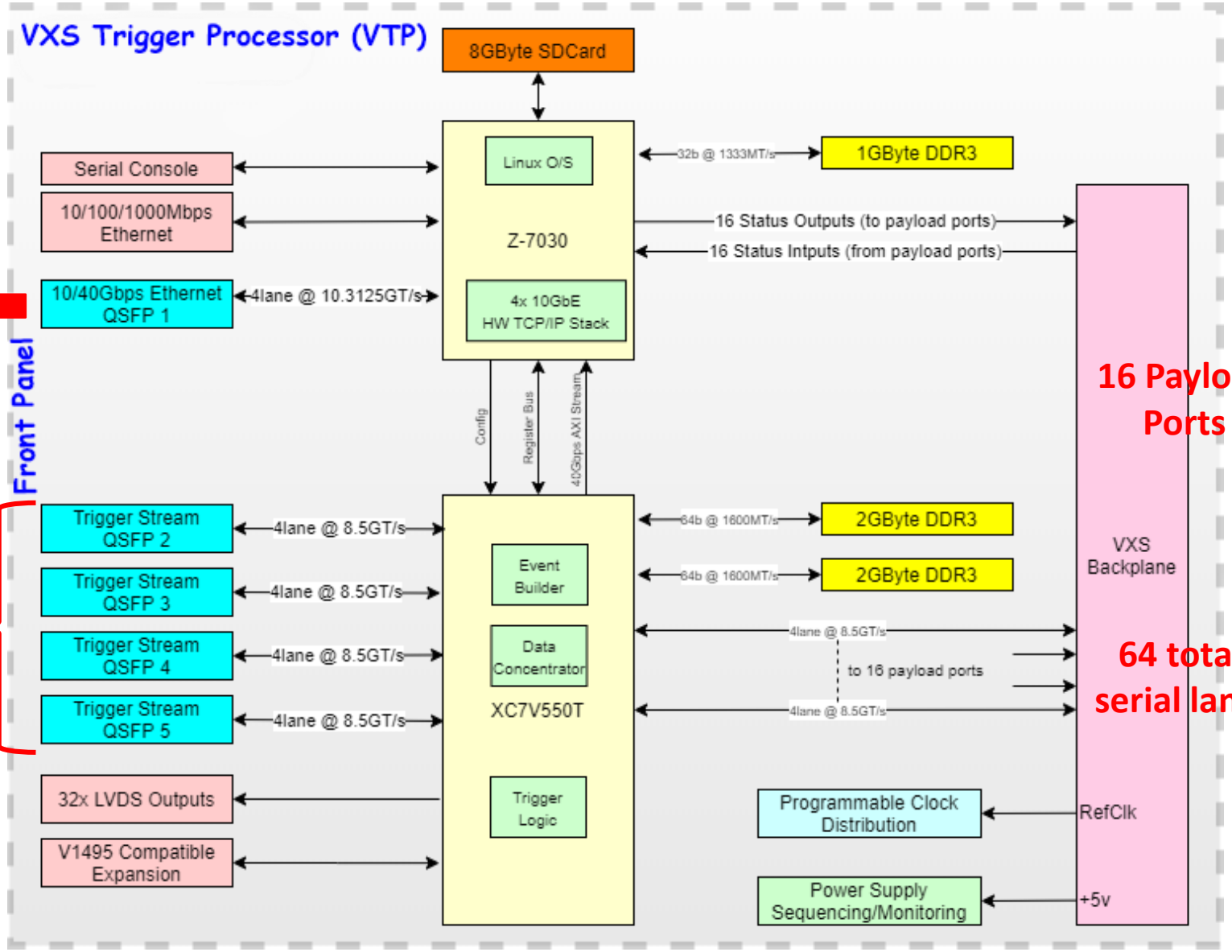
JLAB – VTP Board

Linux OS on the Zync-7030 SoC
(2-core ARM 7L , 1GB DDR3)
10/40Gbps Ethernet option

Xilinx Virtex 7 FPGA
Serial Lanes from both the VXS backplane and the Front panel
4GB DDR3 RAM





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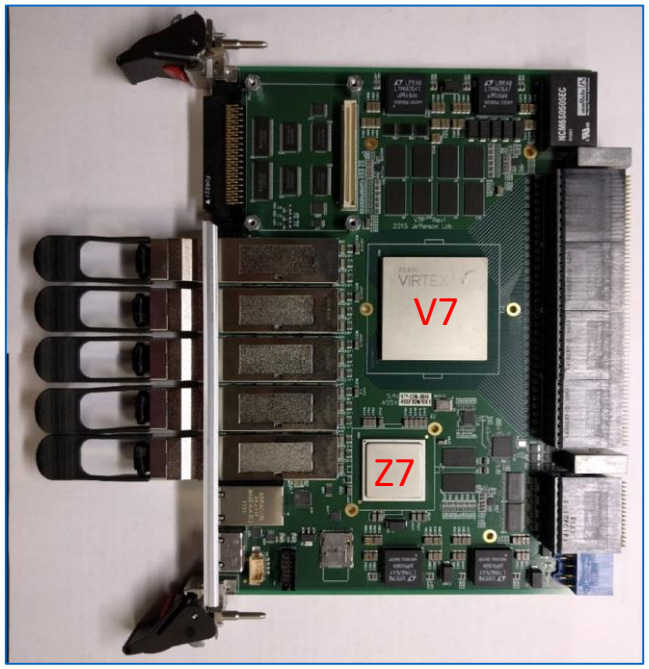
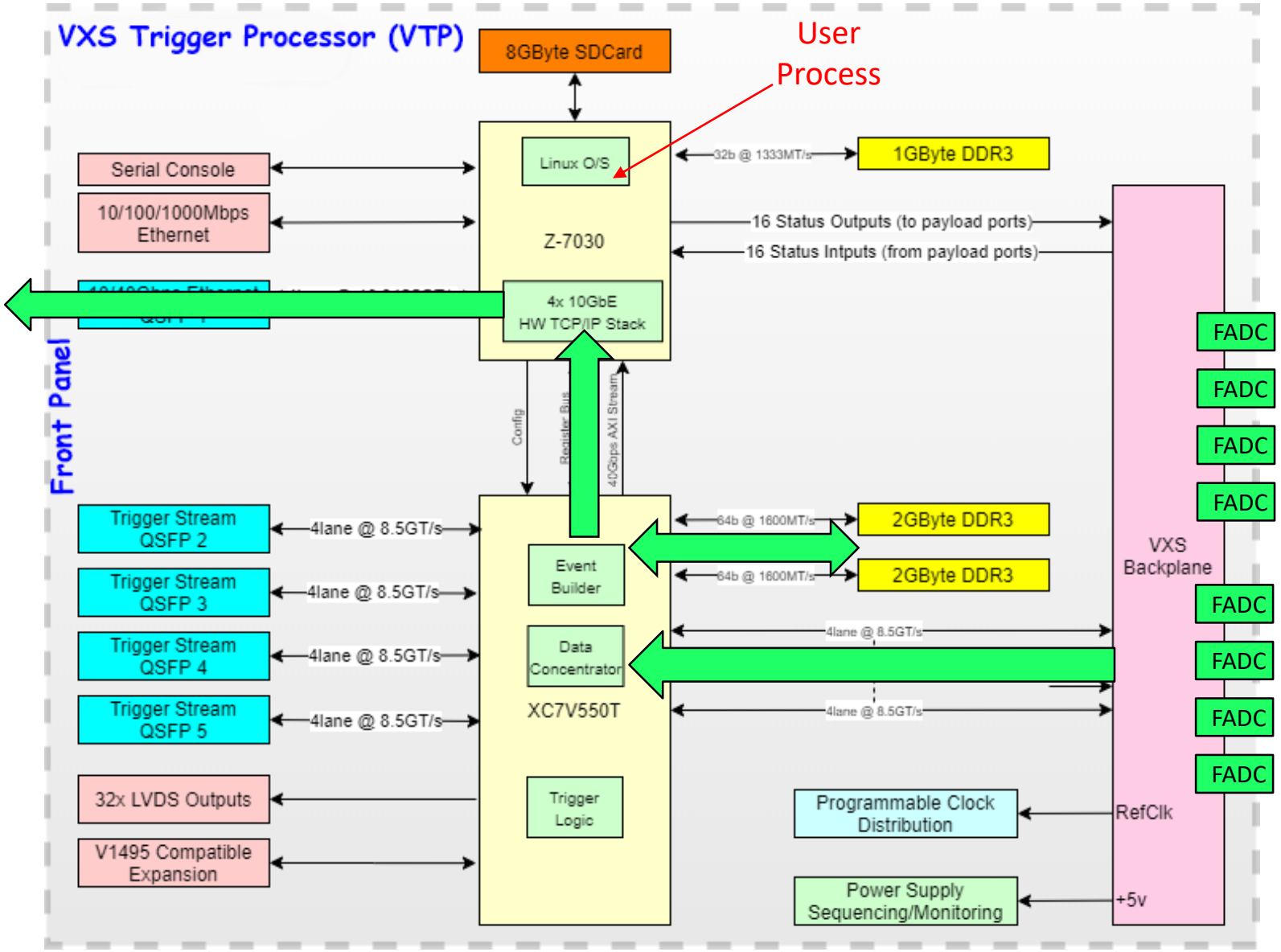
JLAB – VTP Board

- User applications can run on the Zync ARM processor
- Implement firmware & driver libraries that allow control the FPGA config and data flow.





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We are practically “twins”

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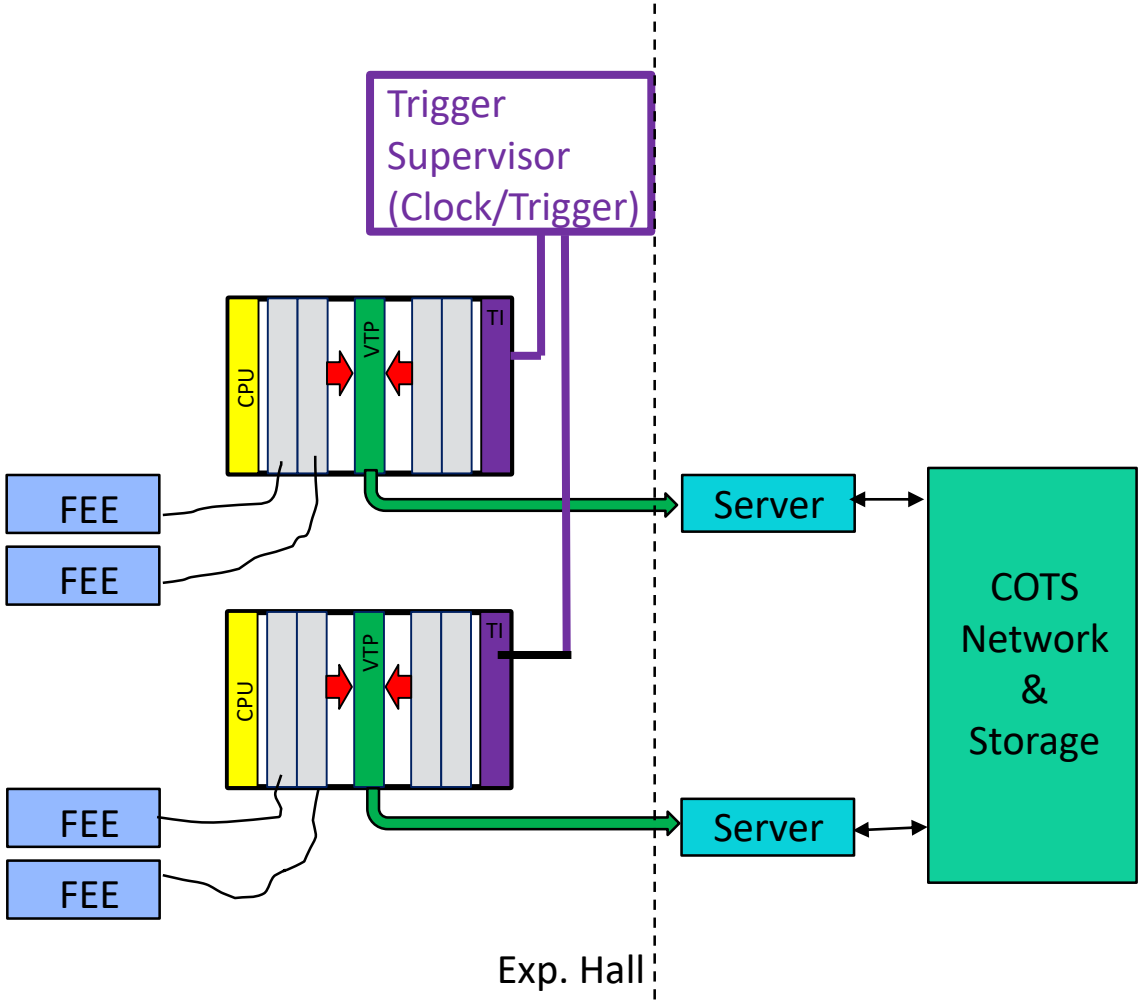
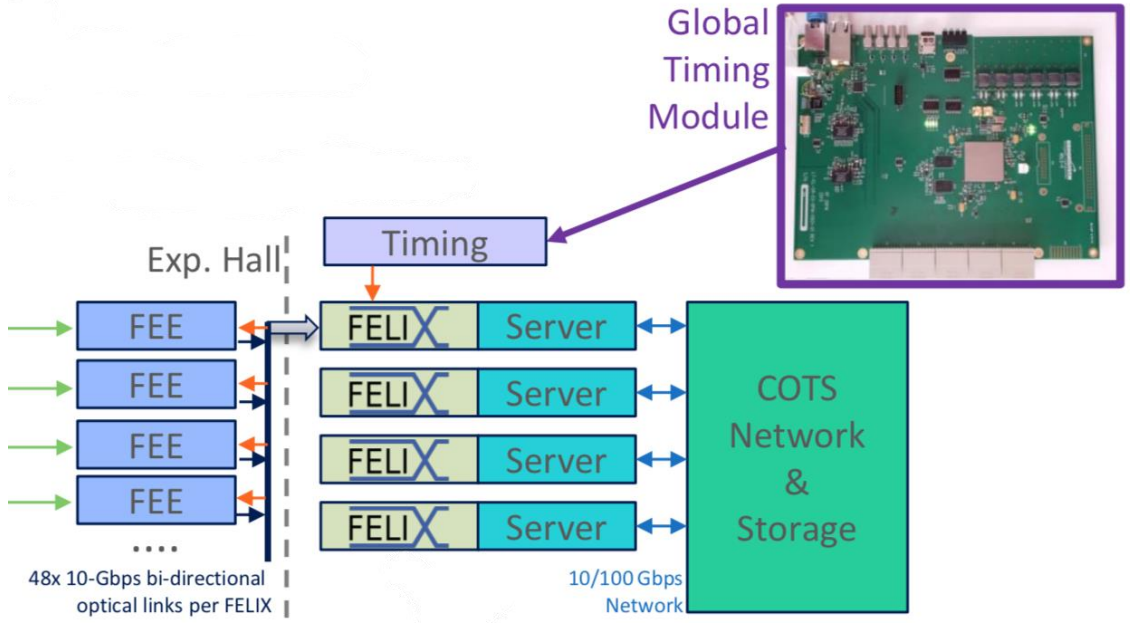


sPHENIX



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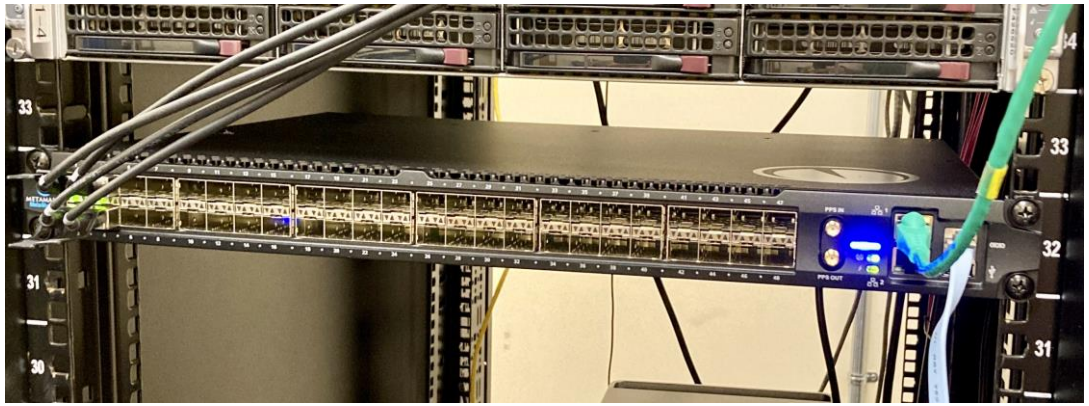
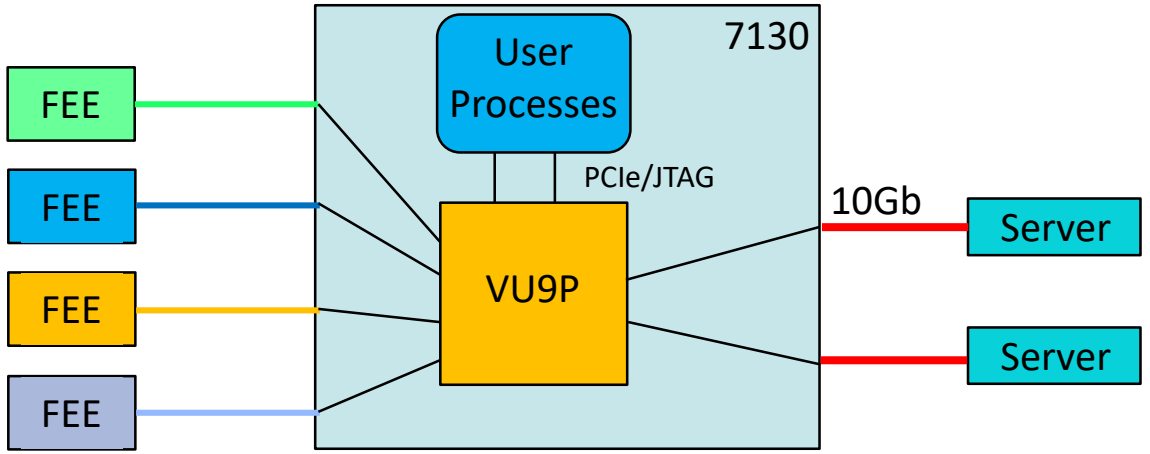
Arista 7130 – FPGA-Based “switch”



- Potentially useful for aggregating serial links from different front-end detector electronics and presenting them as standard ethernet streams for back-end processing.

- Virtex Ultrascale+ VU9P-3 FPGA
- 48 SFP+ Ports can be mapped to 60 application ports directly on the FPGA
- 32 GB (4x8GB) DDR4-2200 RAM
- JTAG and Gen 2 PCIe x8 access to FPGA by on board Intel Atom CPU running Linux.
- Available Vendor application support including - port aggregation and high resolution timestamps.
- All ports can support standard 1/10Gb ethernet or custom serial link protocols.
- Layer 1 switch



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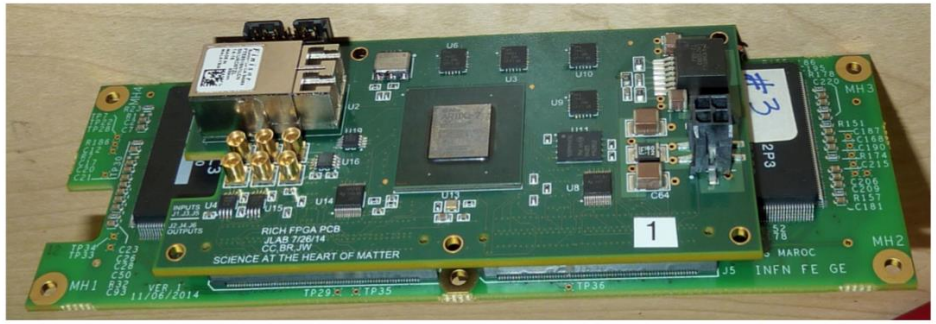
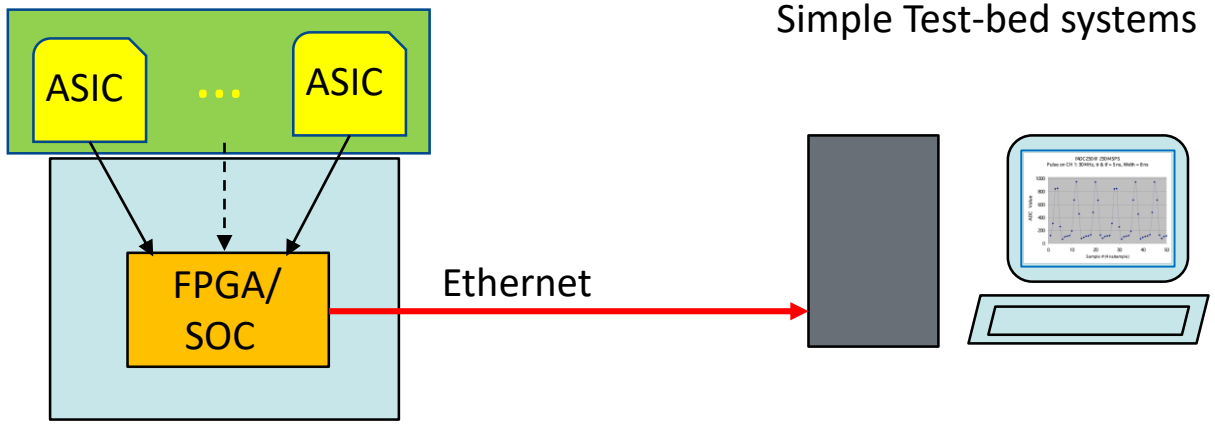
”Smart” Front-End Electronics

ASIC board produced for the RICH detector for CLAS12 with MAROC chips installed

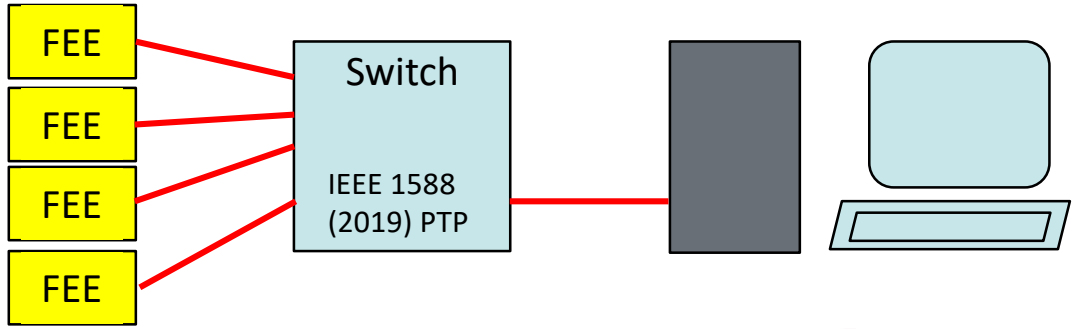


FPGA b Screenshot for the RICH detector for CLAS12 with ASIC board attached

Simple Test-bed systems



Question:
How to distribute a common clock to multiple FEE boards?
Ethernet?



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