BROOKHAVEN NATIONAL LABORATORY

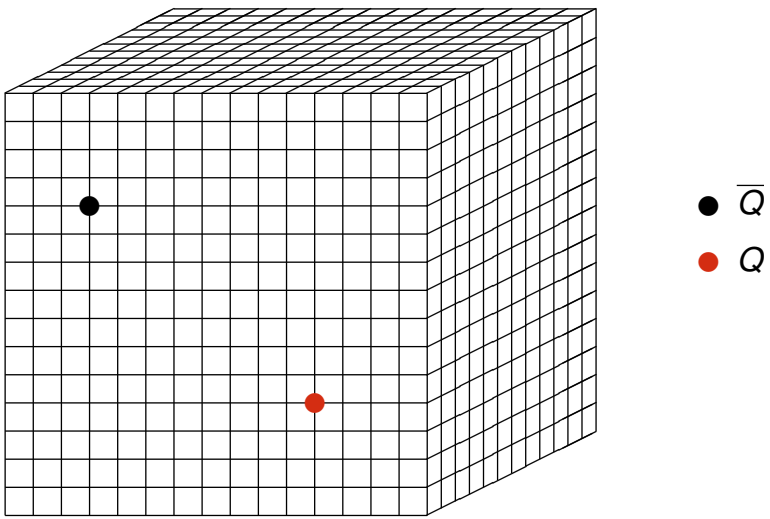
Universität Bielefeld

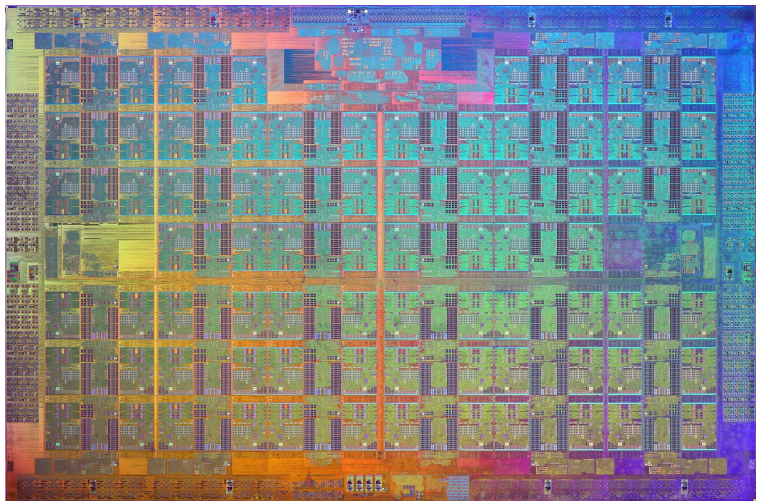
Lattice QCD on modern CPU architectures

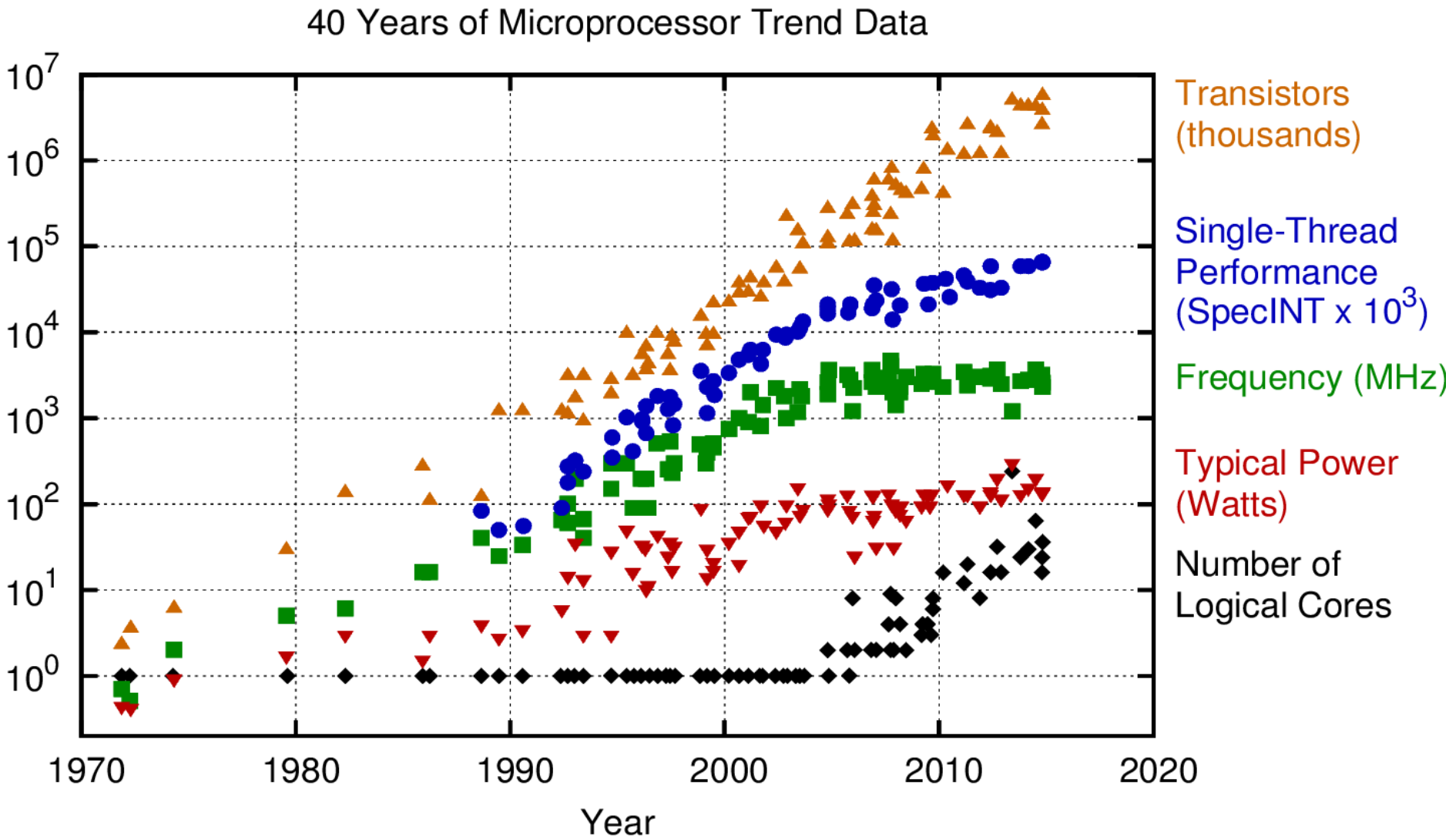
March 10, 2016 | Patrick Steinbrecher

Outline

- The last decade of x86
- Dslash kernel
- The performance gap:
  - plain C vs. optimized code

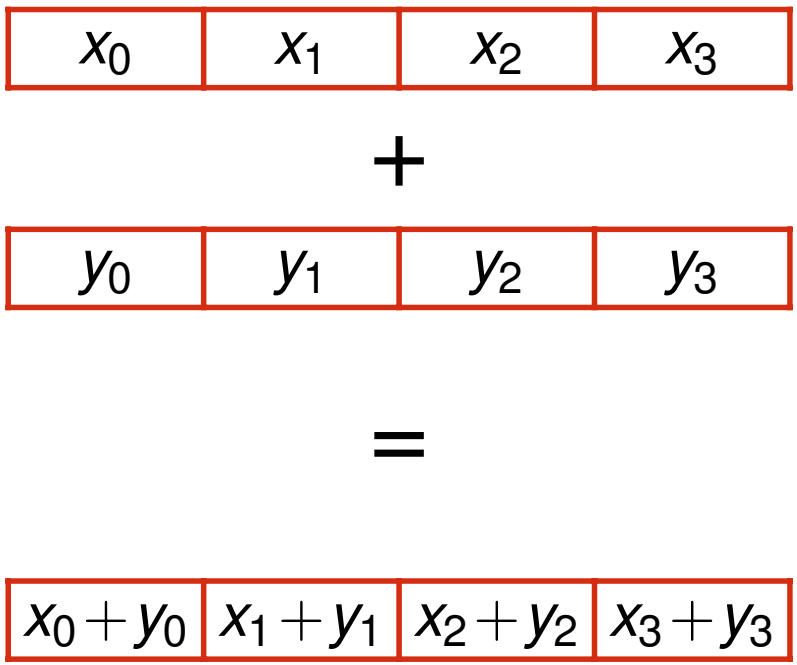






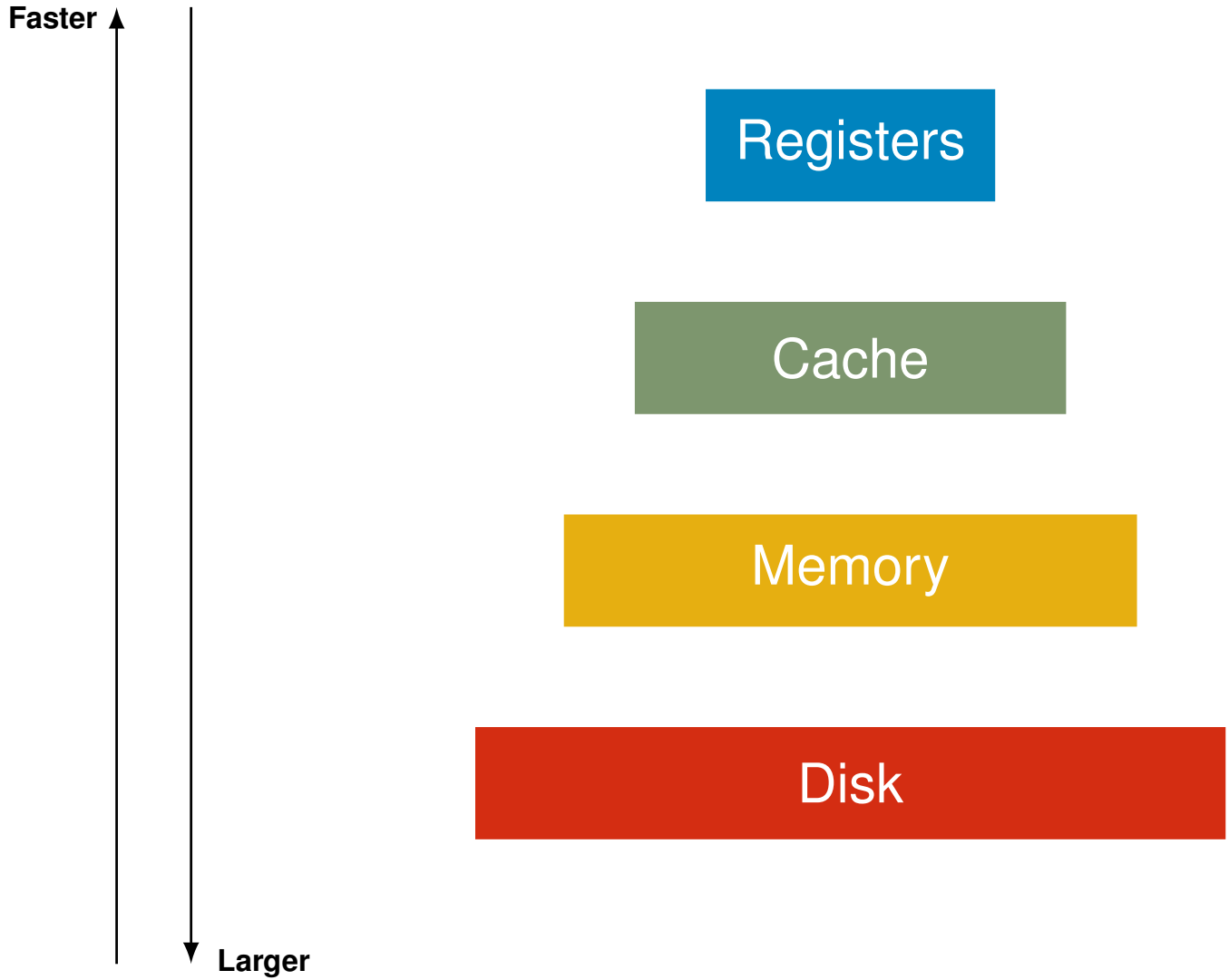
Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2015 by K. Rupp

SIMD: Single Instruction, Multiple Data

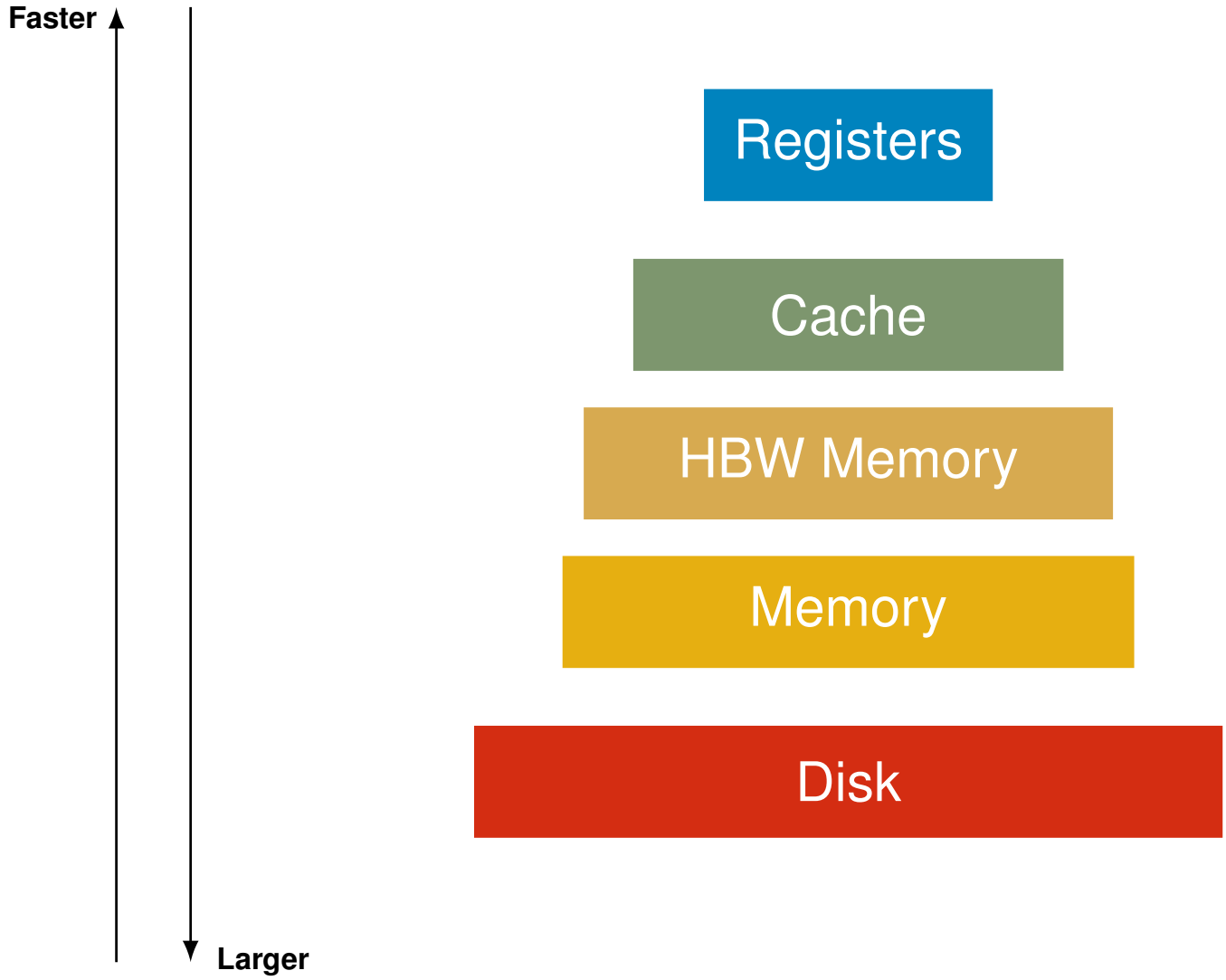


- SISD processor
  - 4 instructions
- SIMD processor
  - 1 instruction

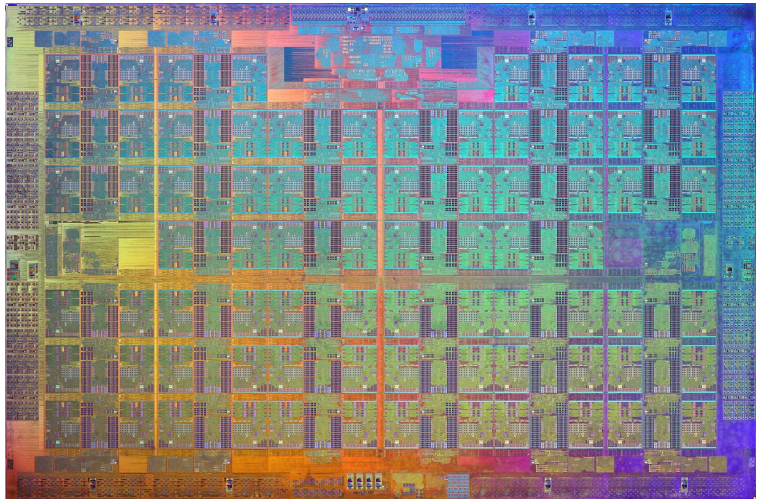
CPU hierarchy



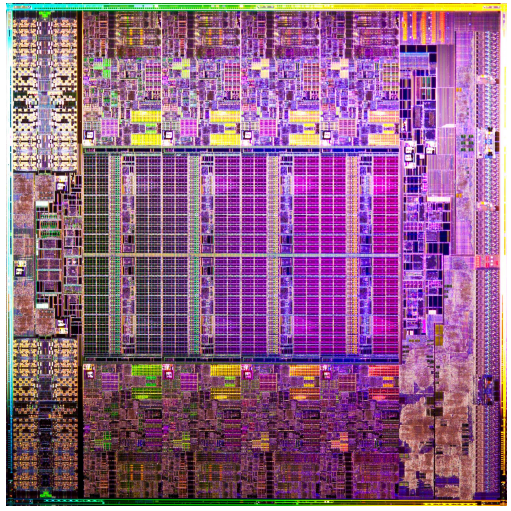
CPU hierarchy



Many- and Multi-core

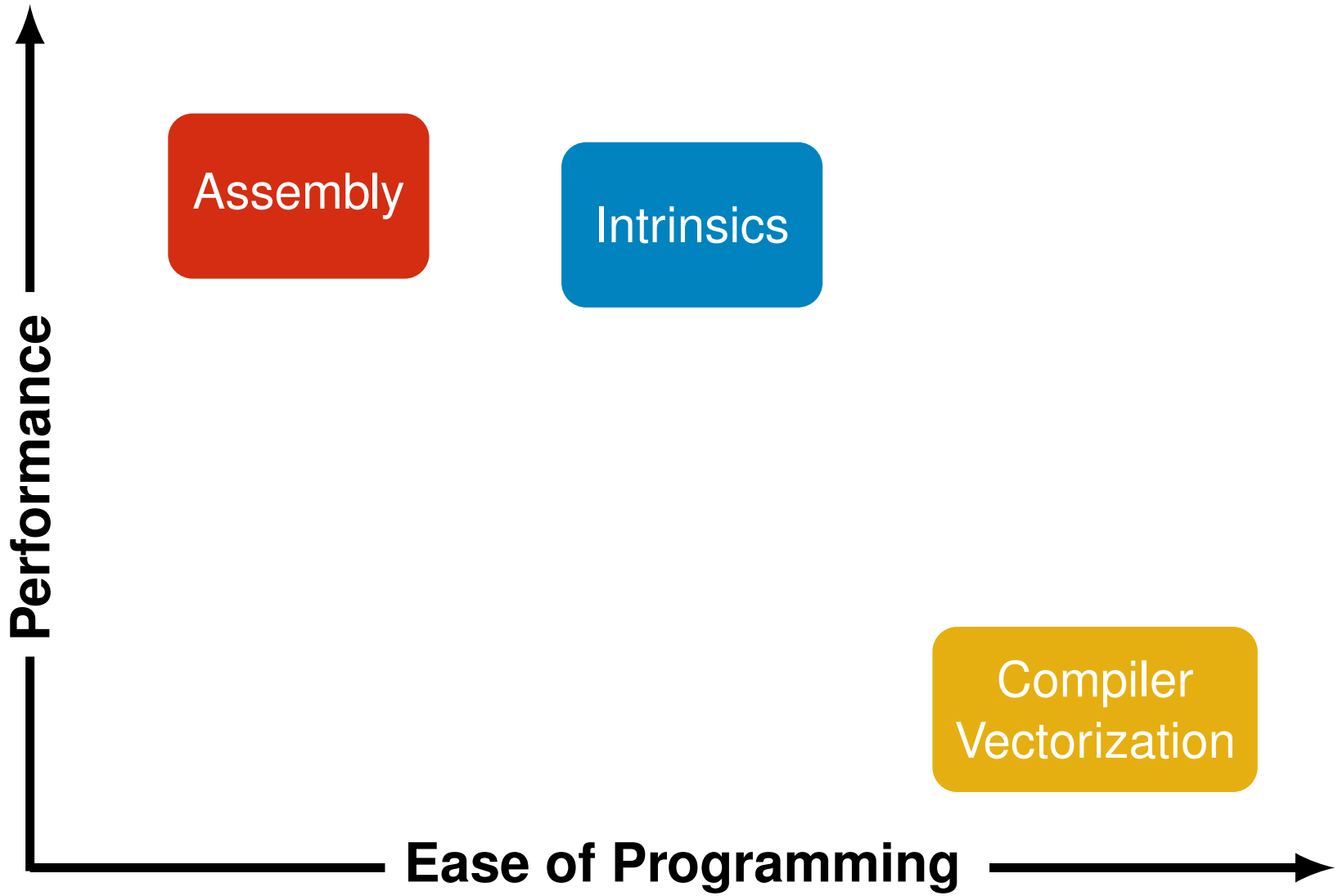


- #cores ≥ 52
- low frequency
- weak/no Out-of-Order
- better energy efficiency
- high $\mathrm{Flop/s}$



- #cores ≤ 18
- high frequency
- deep Out-of-Order
- large shared cache

Vectorization techniques



HISQ Dslash $w = \not{D} v$

$$w_n = \sum_{\mu=0}^{4} \left[\left(U_{n,\mu} v_{n+\mu} - U^{\dagger}_{n-\mu,\mu} v_{n-\mu} \right) + \left(N_{n,\mu} v_{n+3\mu} - N^{\dagger}_{n-3\mu,\mu} v_{n-3\mu} \right) \right]$$

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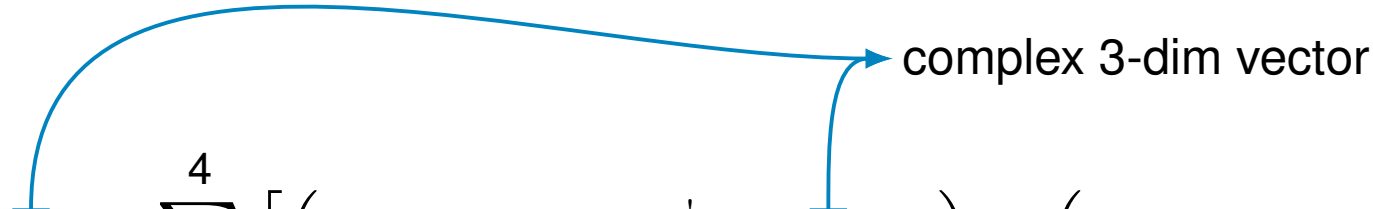

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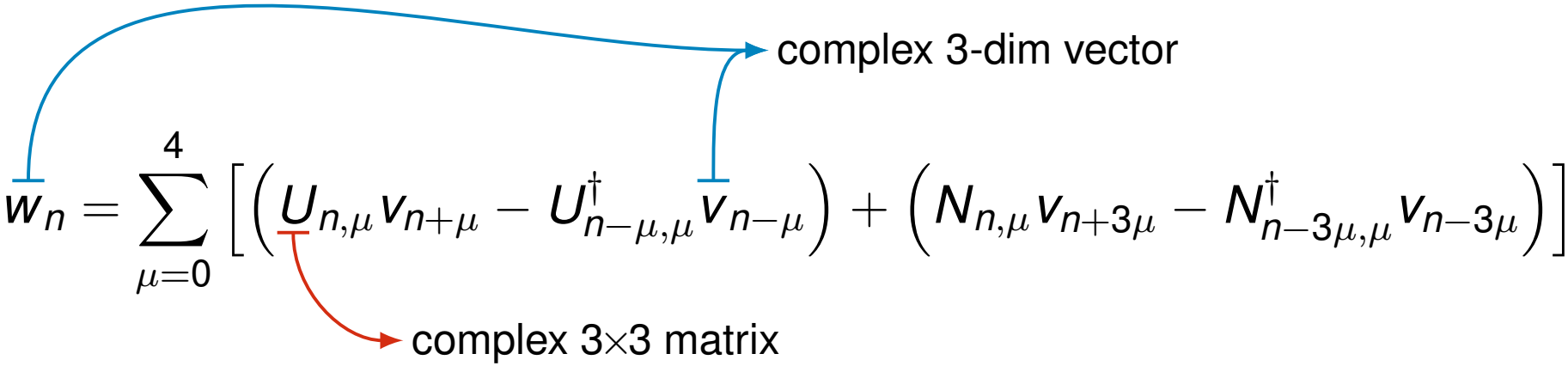

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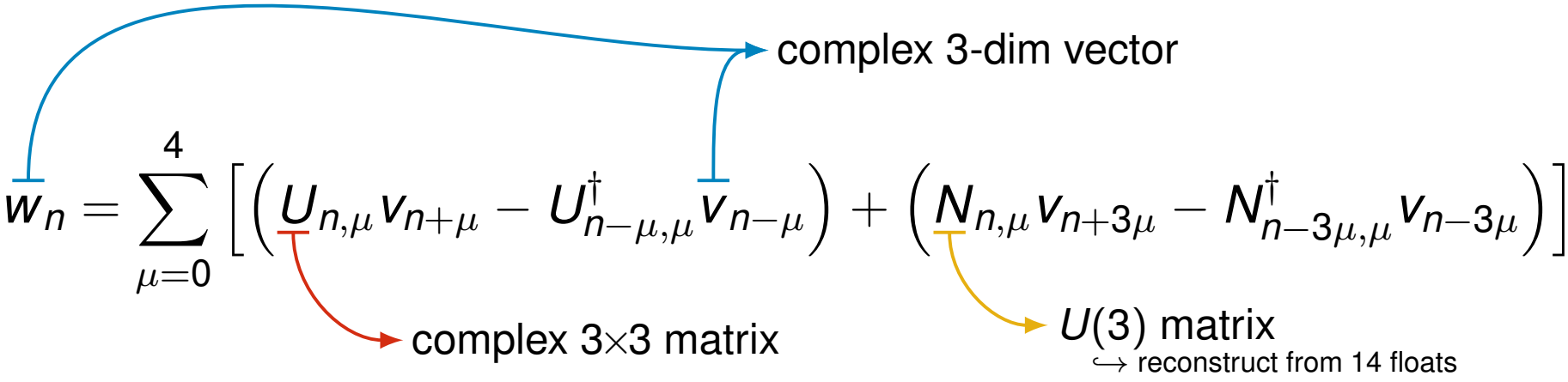


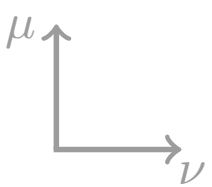
HISQ Dslash $w = \not{D} v$

complex 3-dim vector

$$w_n = \sum_{\mu=0}^{4} \left[\left(U_{n,\mu} v_{n+\mu} - U^{\dagger}_{n-\mu,\mu} v_{n-\mu} \right) + \left(N_{n,\mu} v_{n+3\mu} - N^{\dagger}_{n-3\mu,\mu} v_{n-3\mu} \right) \right]$$

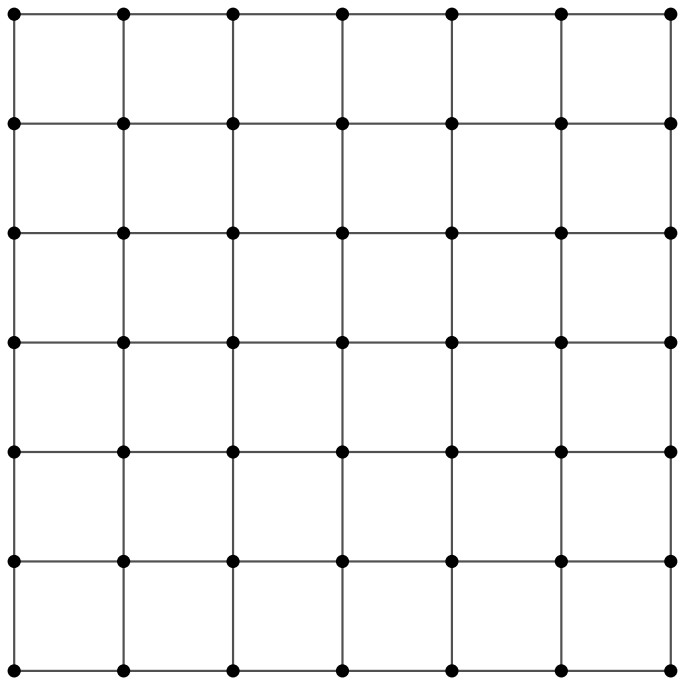
complex 3×3 matrix

$U(3)$ matrix
↪ reconstruct from 14 floats



matrix

vector



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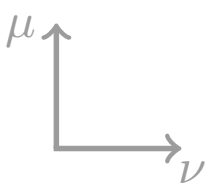

matrix

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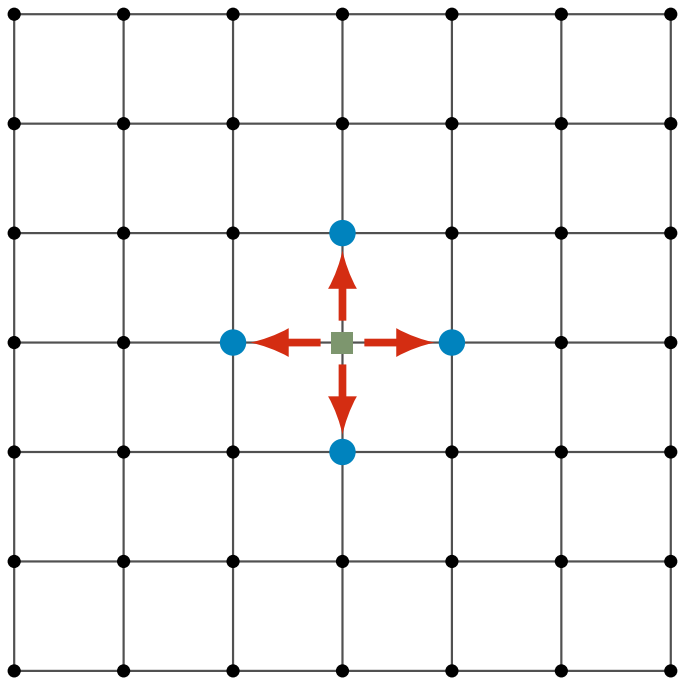

$w_{\blacksquare} =$ standard

HISQ Dslash $w = \not{D} v$

complex 3-dim vector

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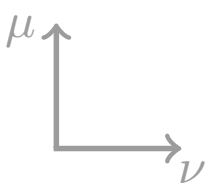
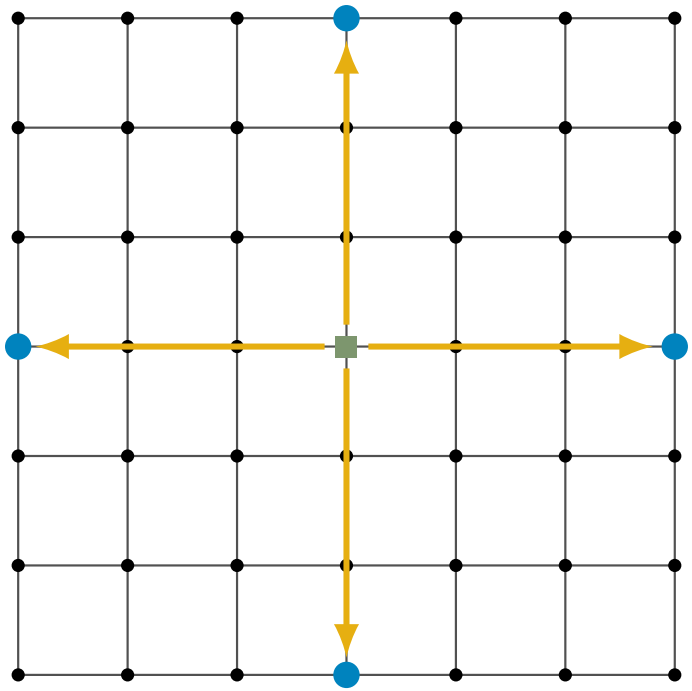


matrix

vector



$w_{\blacksquare}$ = standard

\+ naik

↳ precalculated three-link term

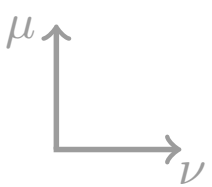
HISQ Dslash $w = \not{D} v$

complex 3-dim vector

$$w_n = \sum_{\mu=0}^{4} \left[\left(U_{n,\mu} v_{n+\mu} - U^{\dagger}_{n-\mu,\mu} v_{n-\mu} \right) + \left(N_{n,\mu} v_{n+3\mu} - N^{\dagger}_{n-3\mu,\mu} v_{n-3\mu} \right) \right]$$

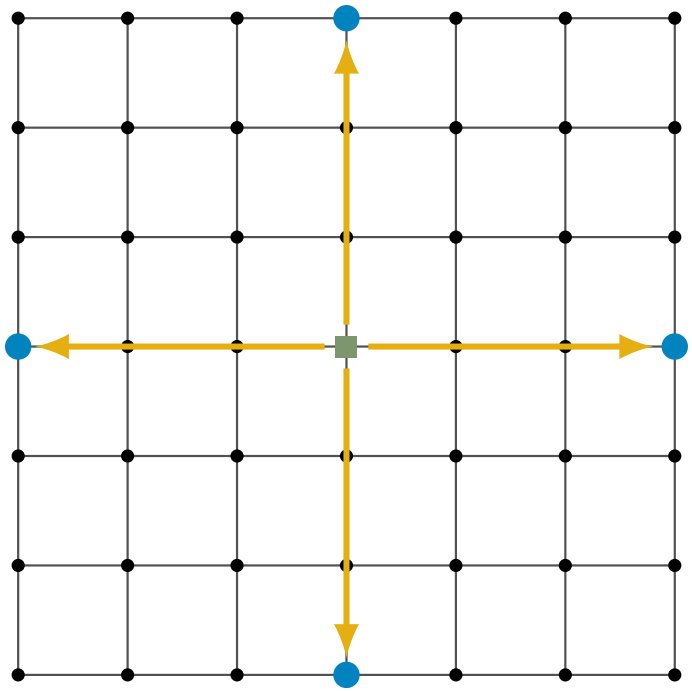
complex 3×3 matrix

$U(3)$ matrix
↪ reconstruct from 14 floats



matrix

vector



1146 Flop/site

0.8 Flop/byte
↪ single-precision

$w_{\blacksquare}$ = standard
+ naik
↳ precalculated three-link term

Multiple right-hand sides

Memory

Memory

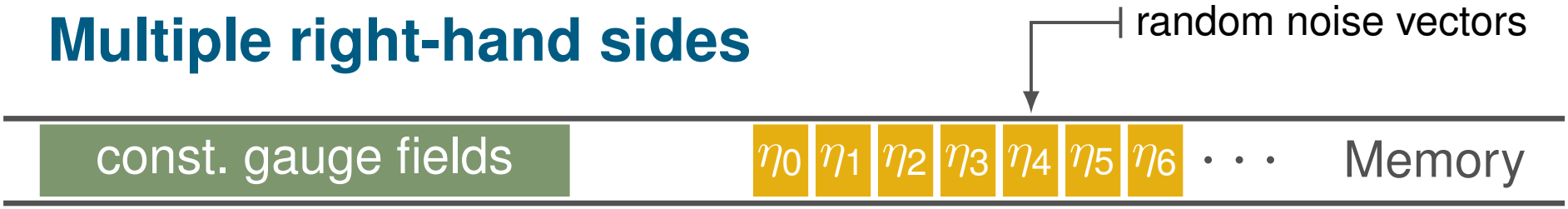
Multiple right-hand sides

const. gauge fields

Memory

Memory

Multiple right-hand sides



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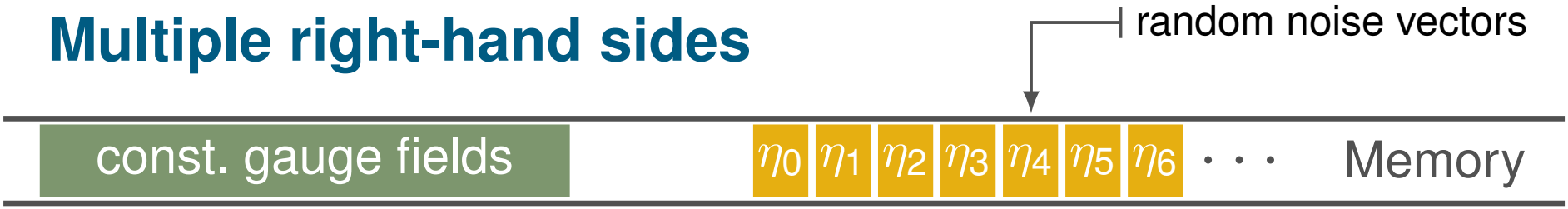

DS( )

Memory

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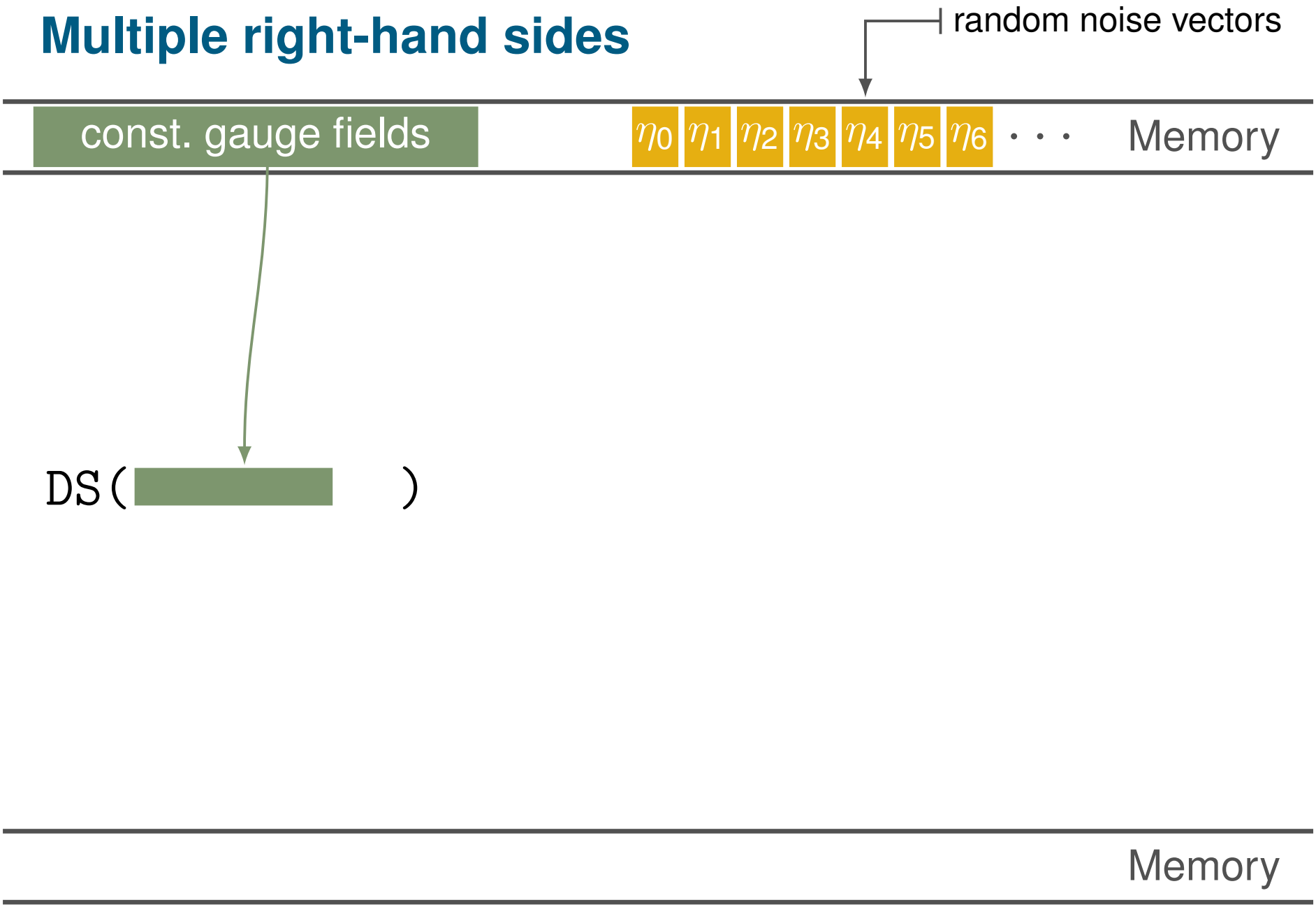

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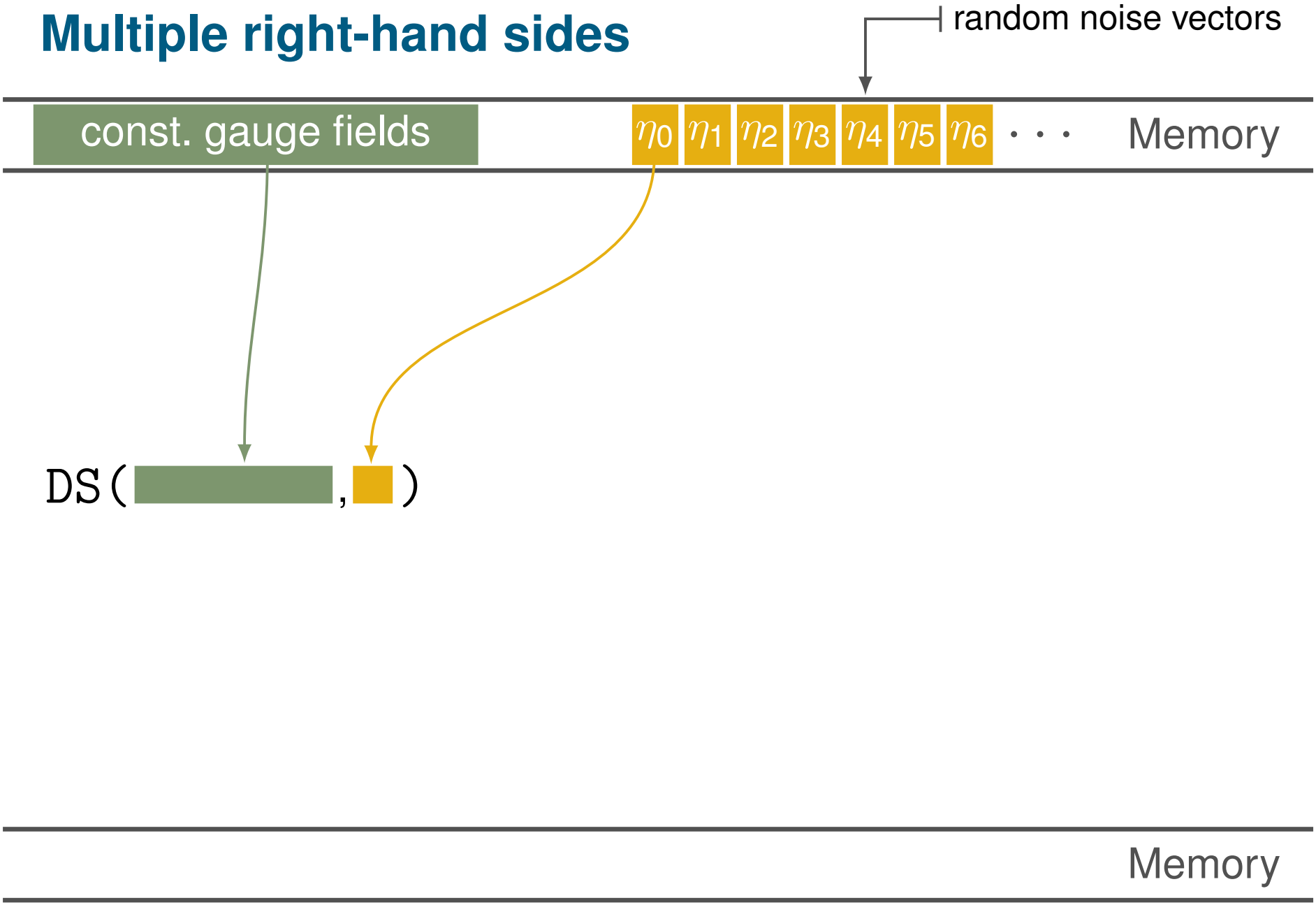

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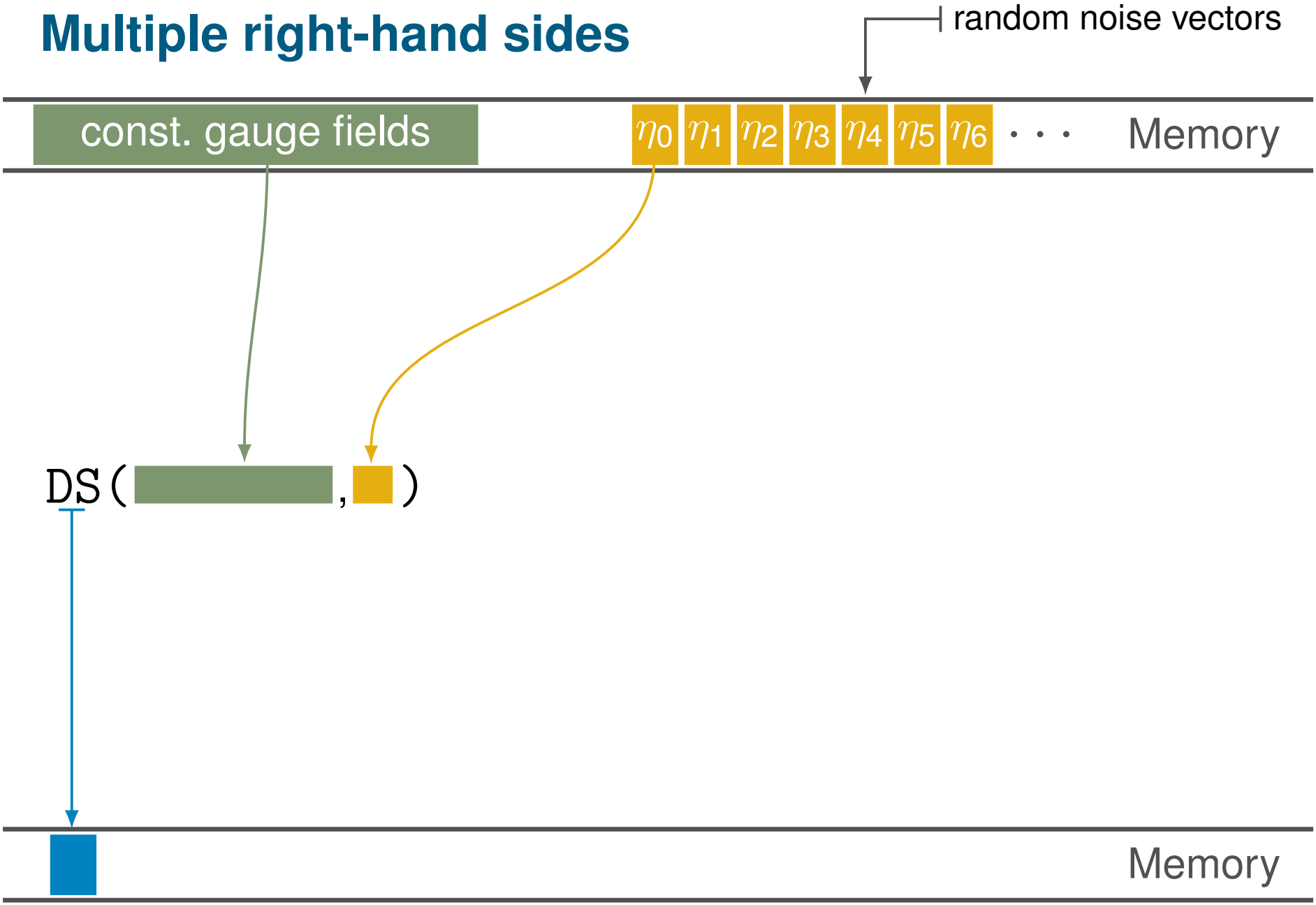

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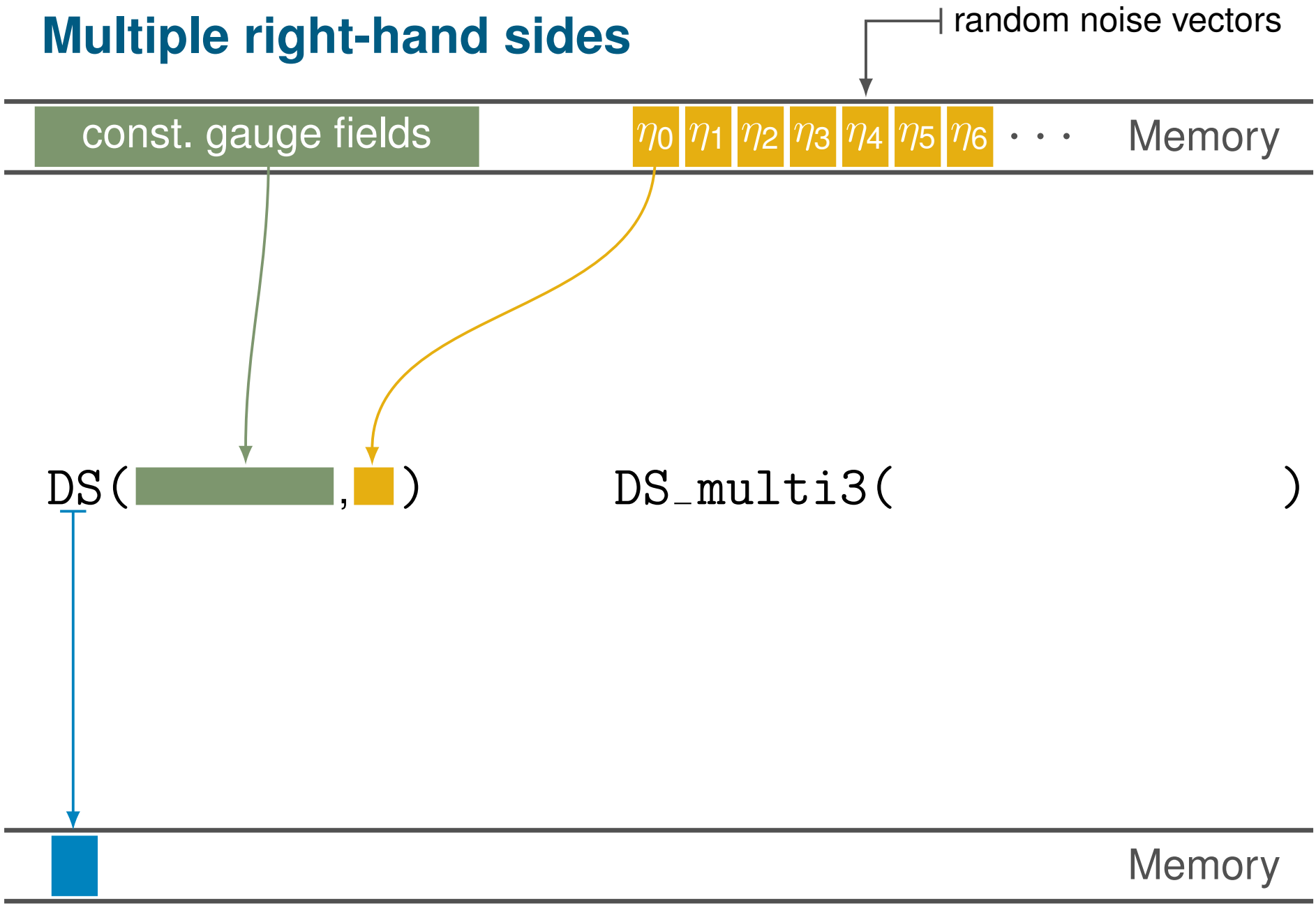

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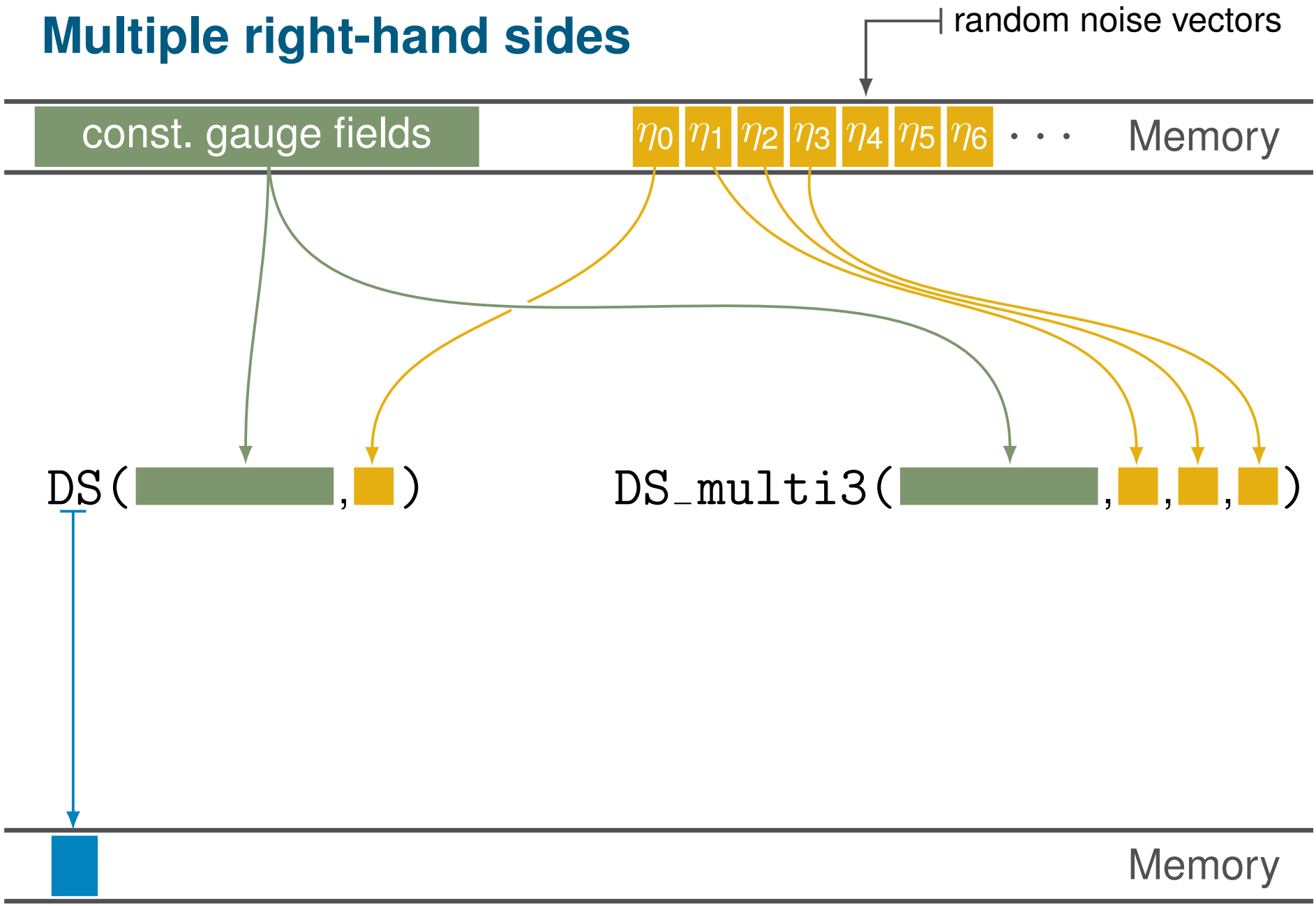

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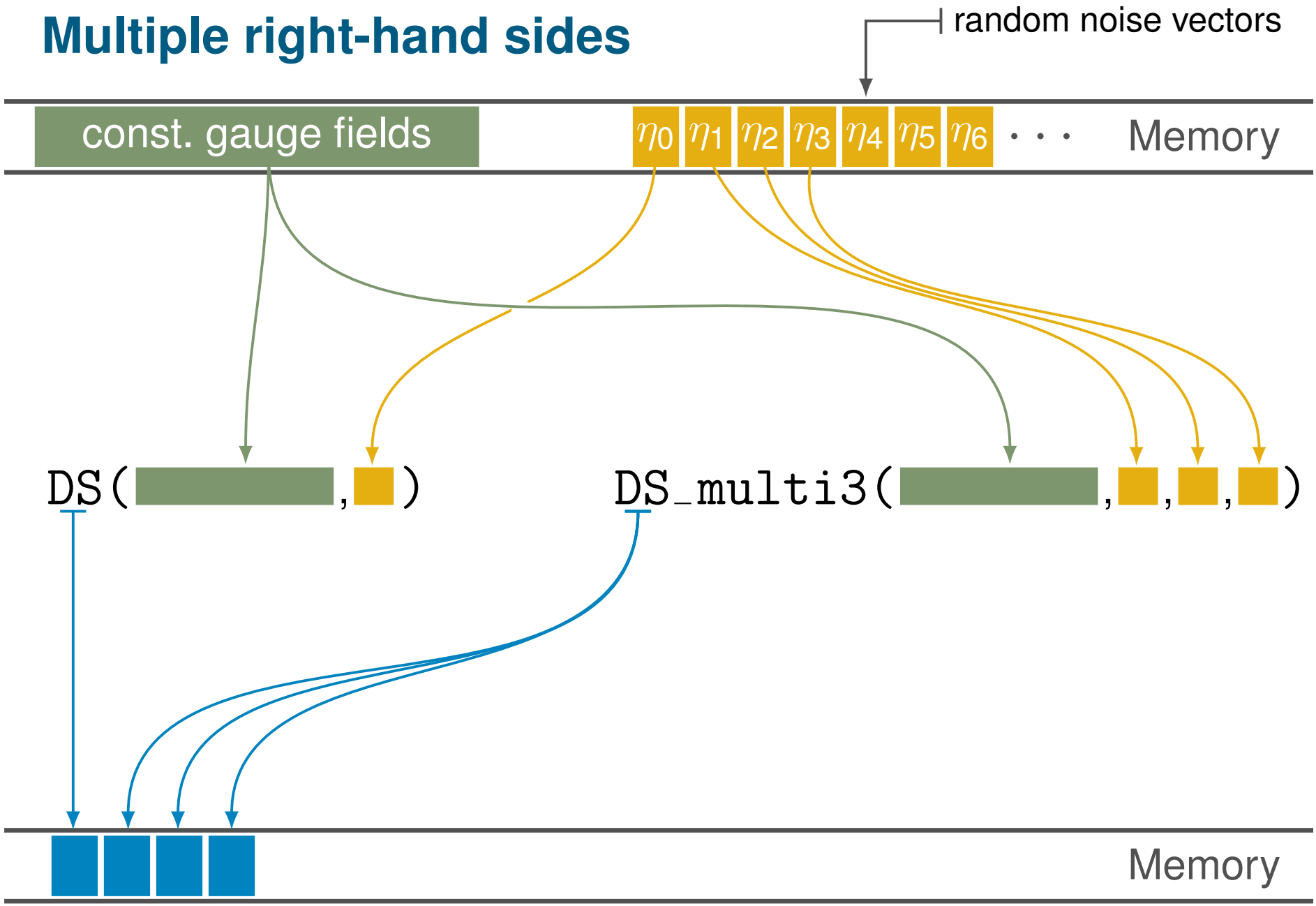

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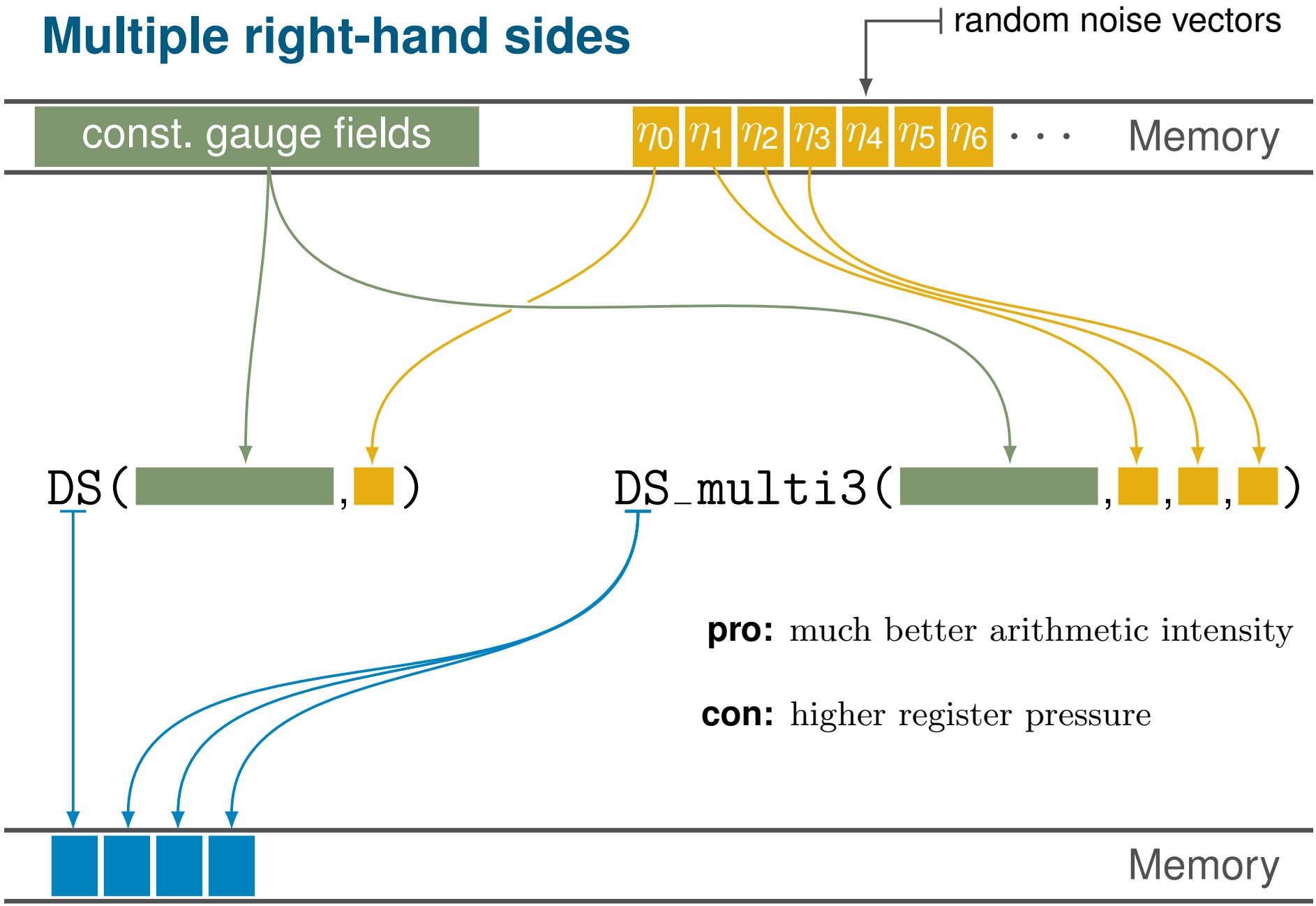
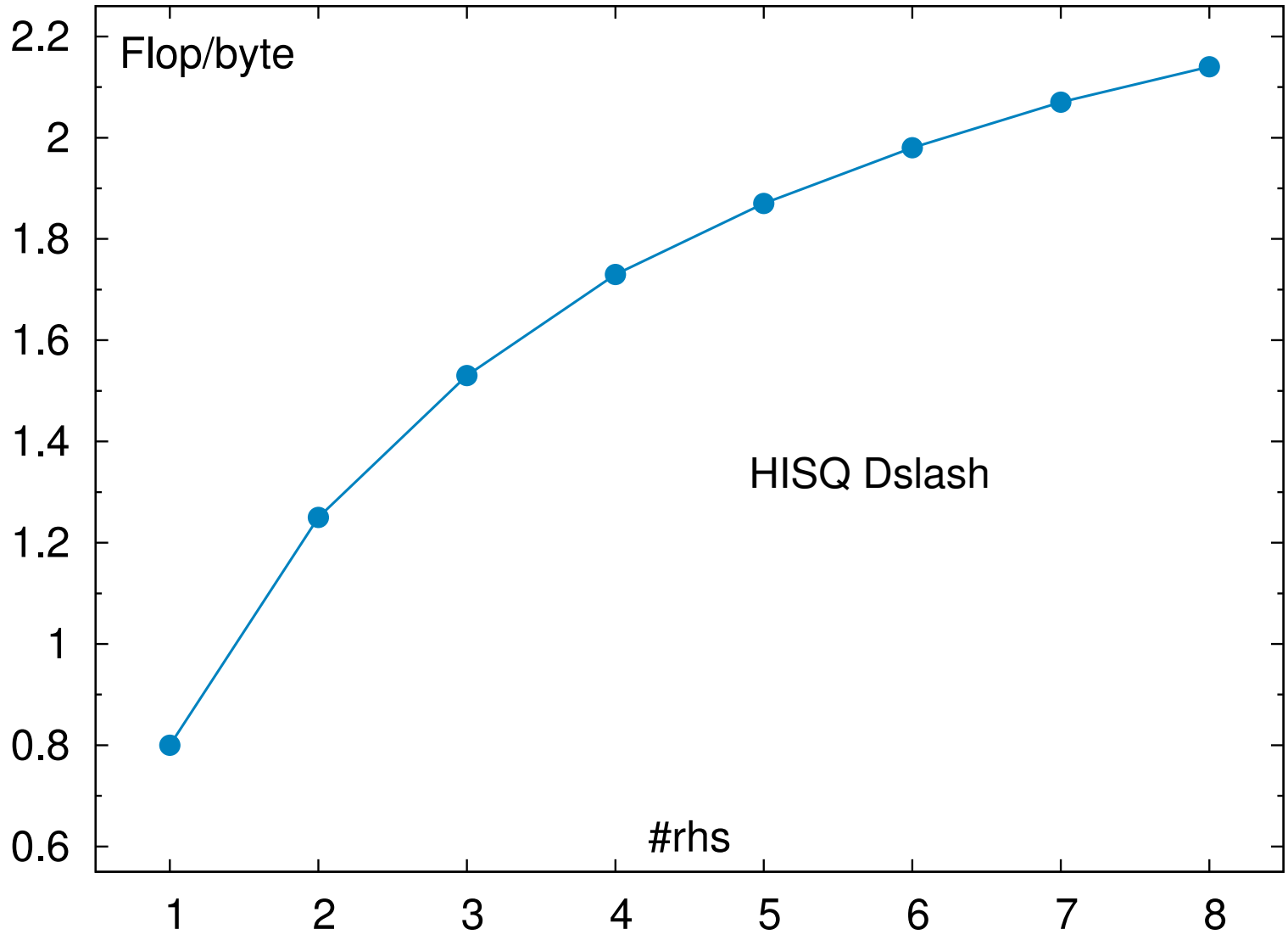


pro: much better arithmetic intensity

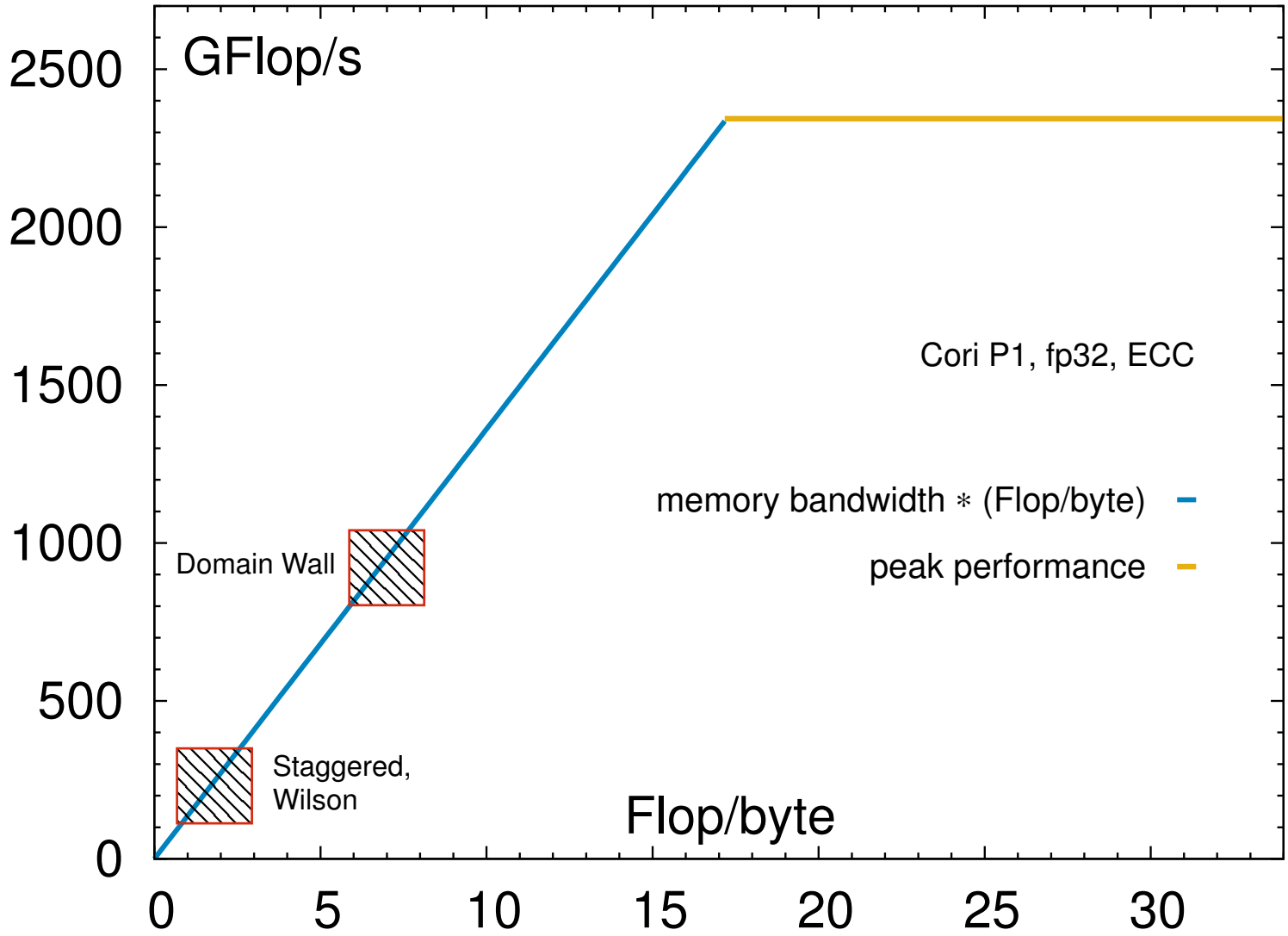
con: higher register pressure

Multiple right-hand sides (rhs)



Performance on Haswell

(dual-socket E5-2698V3, 2.3 GHz, 32 cores)



Dslash on Haswell

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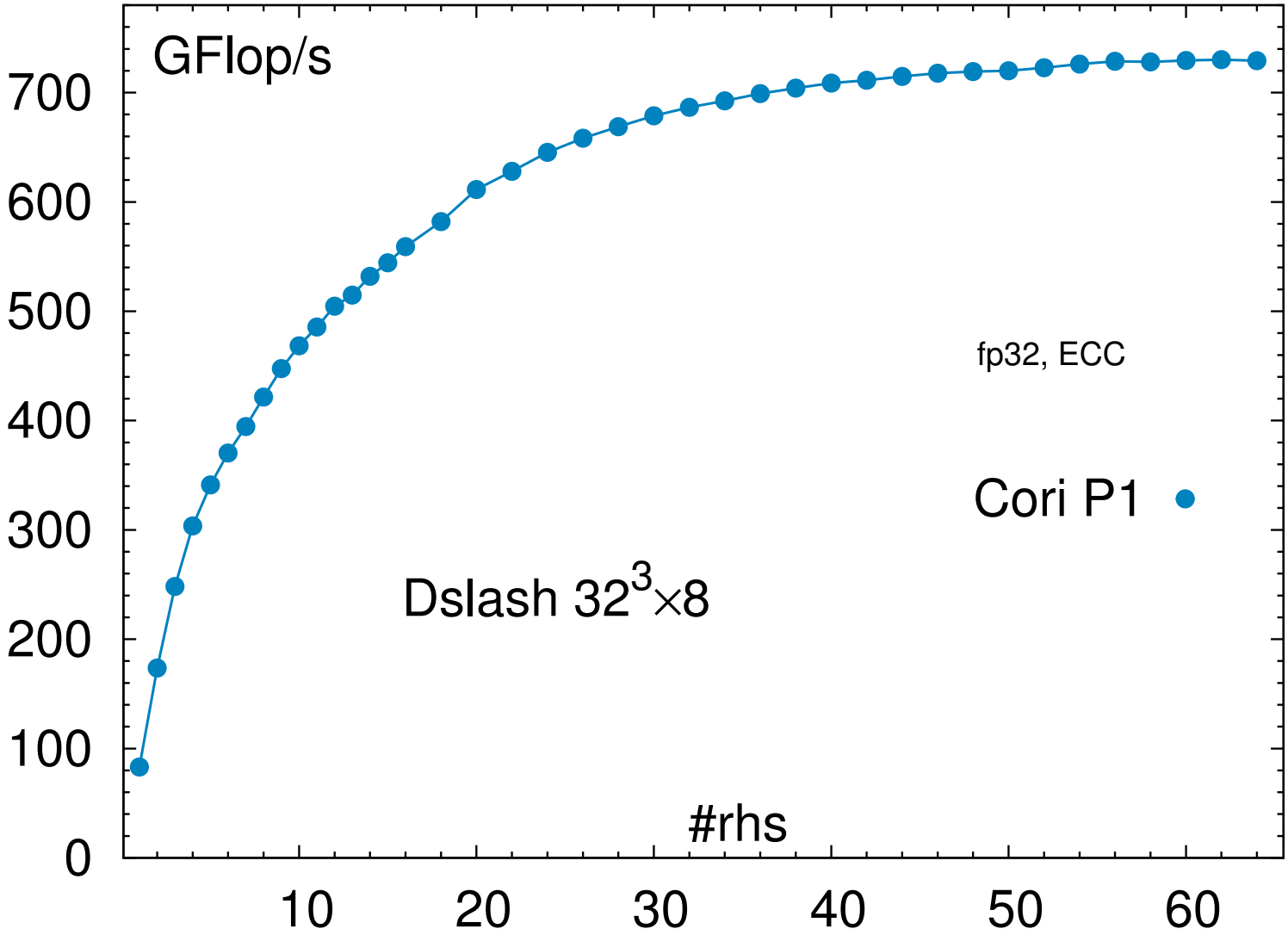
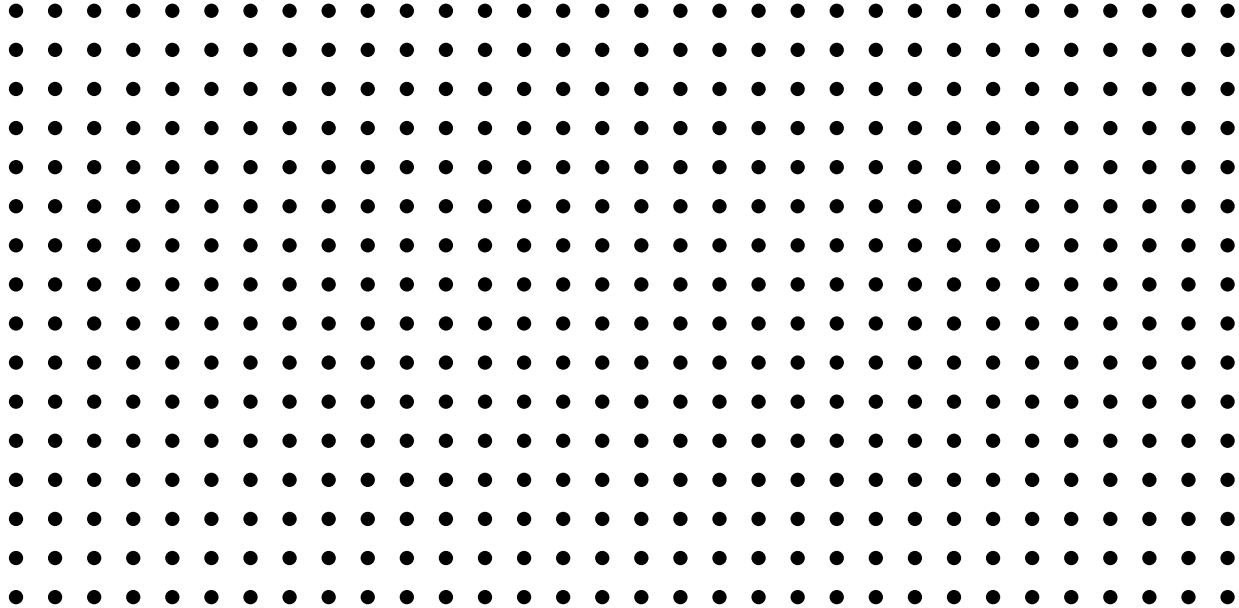


Vectorizing QCD

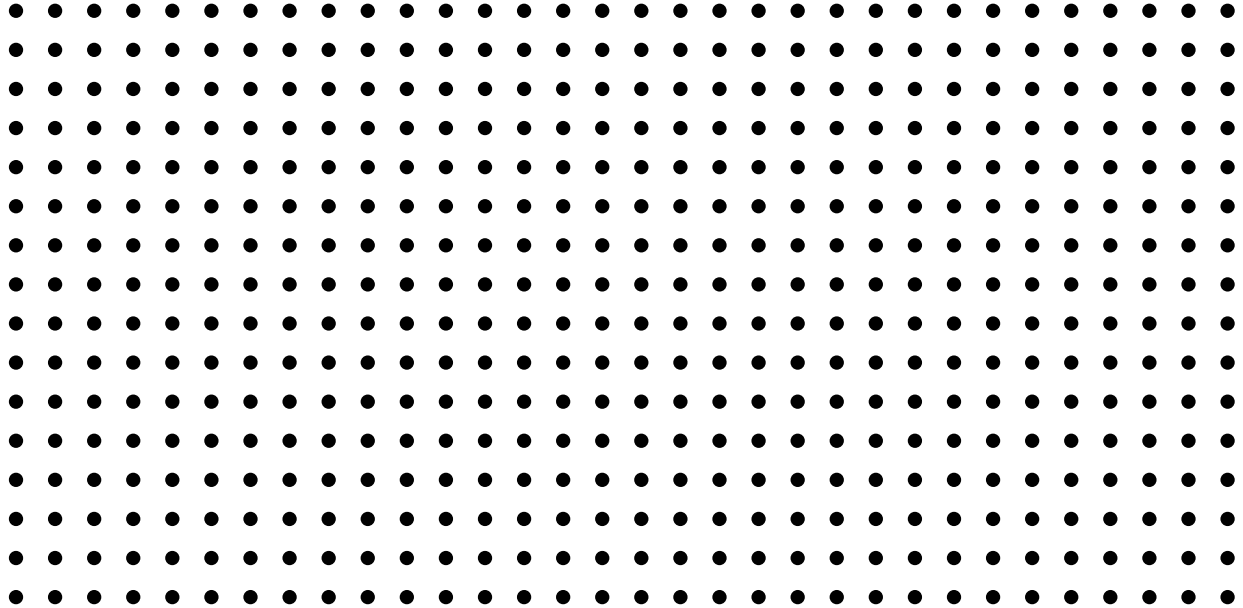
Site fusion



Vectorizing QCD

Site fusion

- even
- odd



- even-odd preconditioning
  - need to fuse sites of the same parity

Vectorizing QCD

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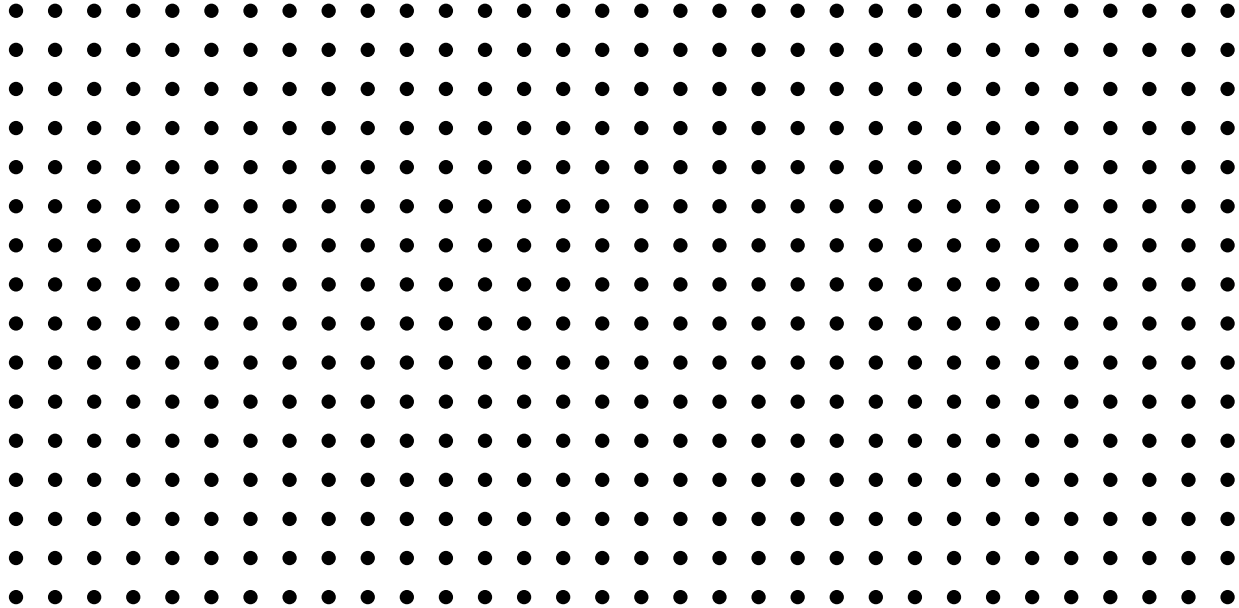

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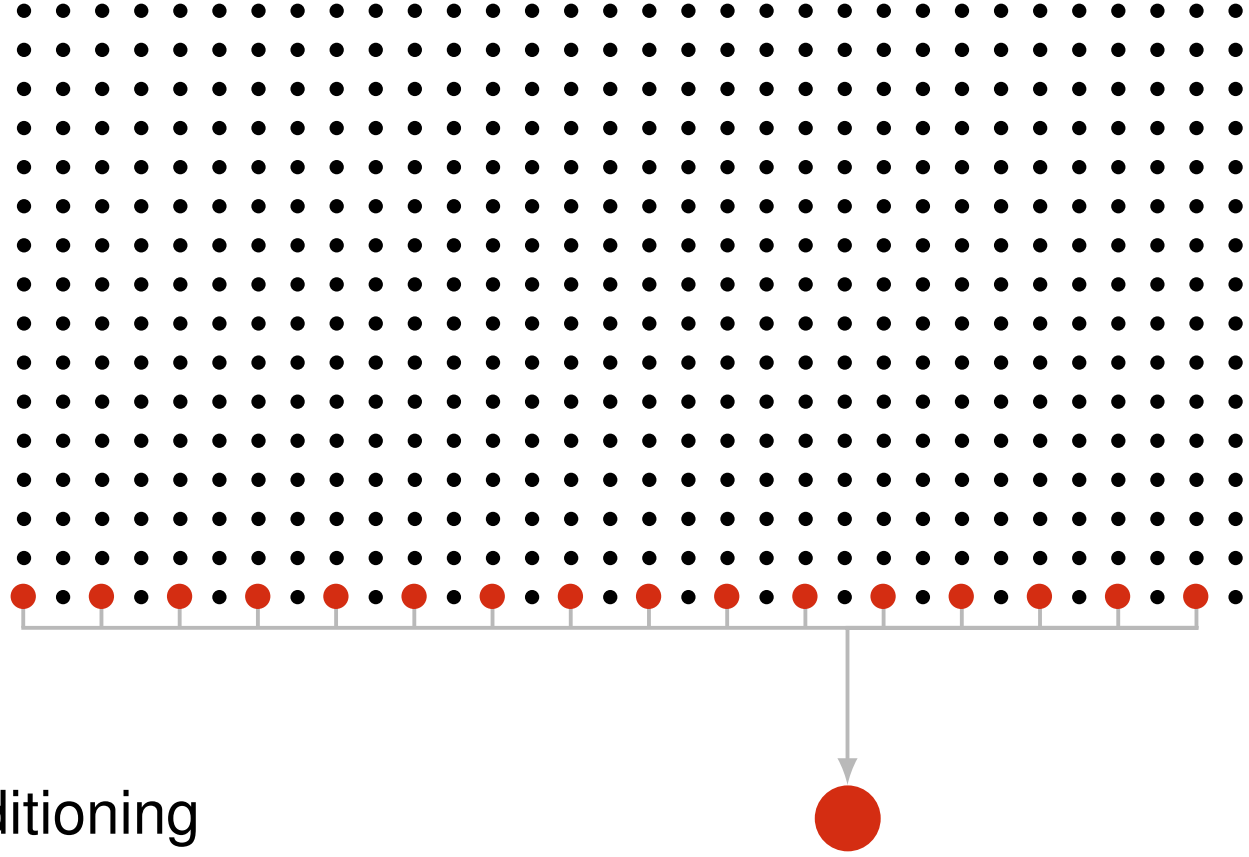

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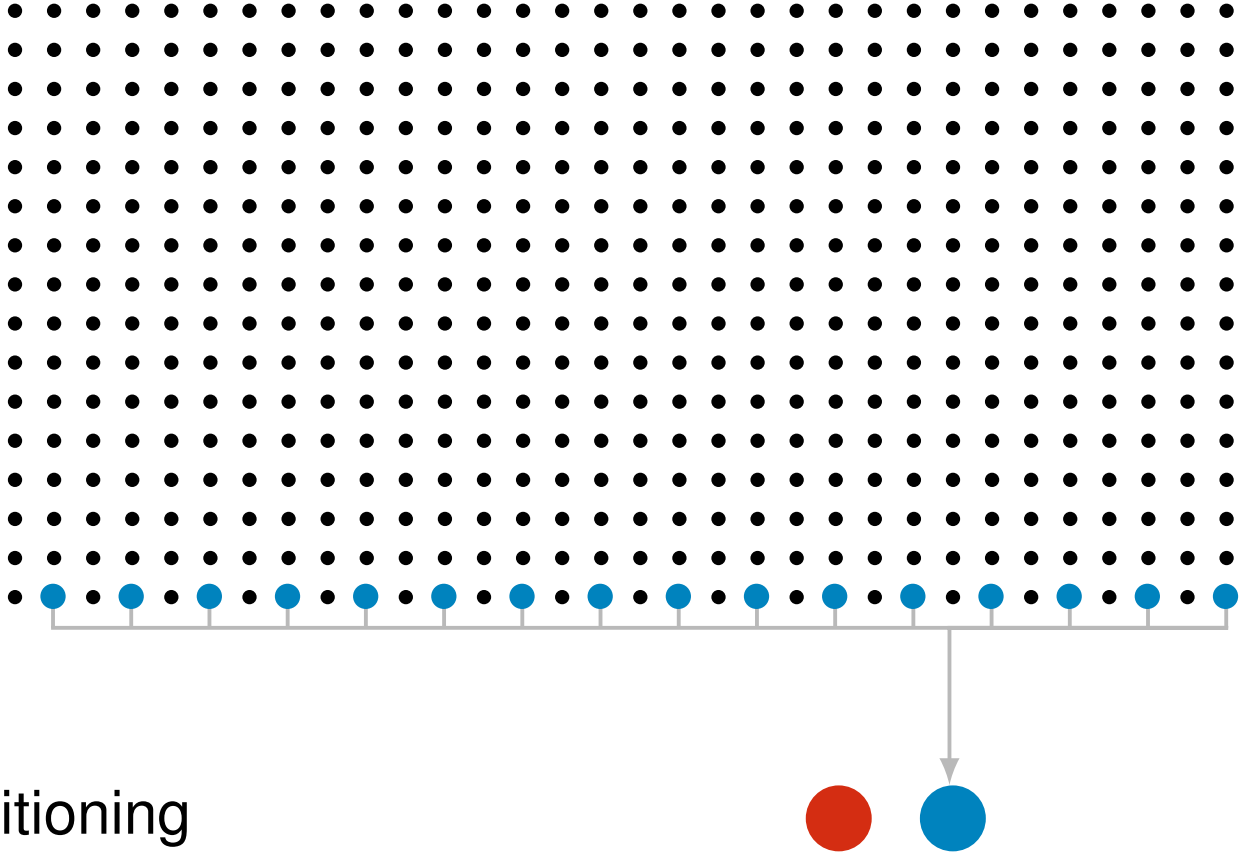

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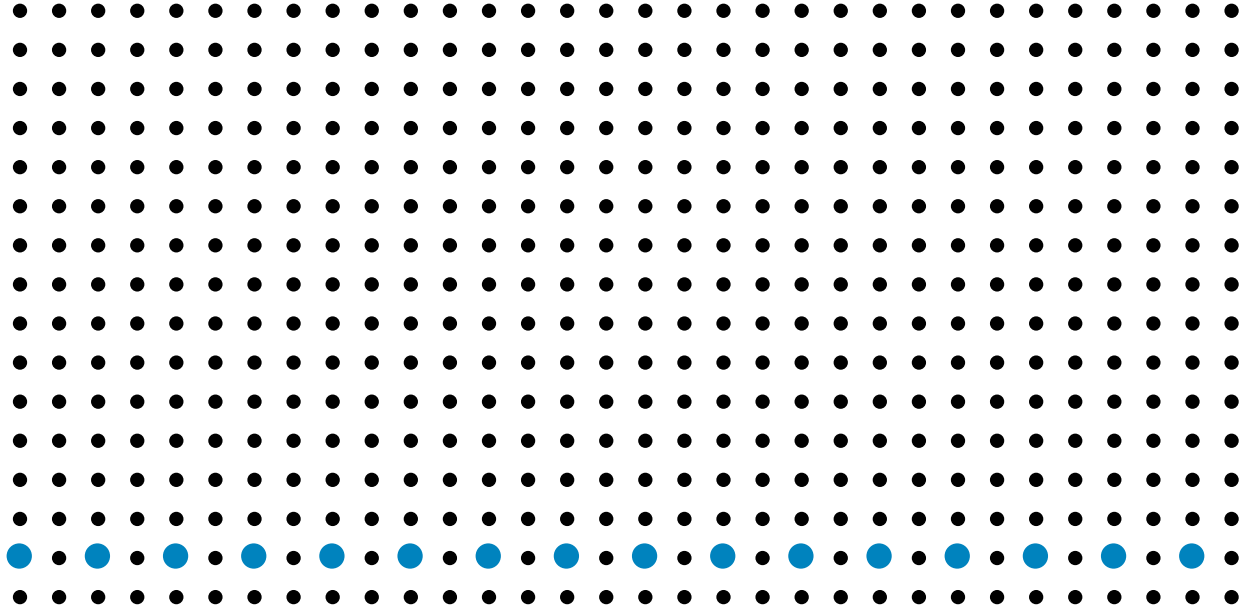

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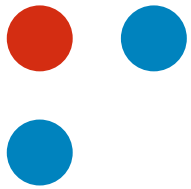

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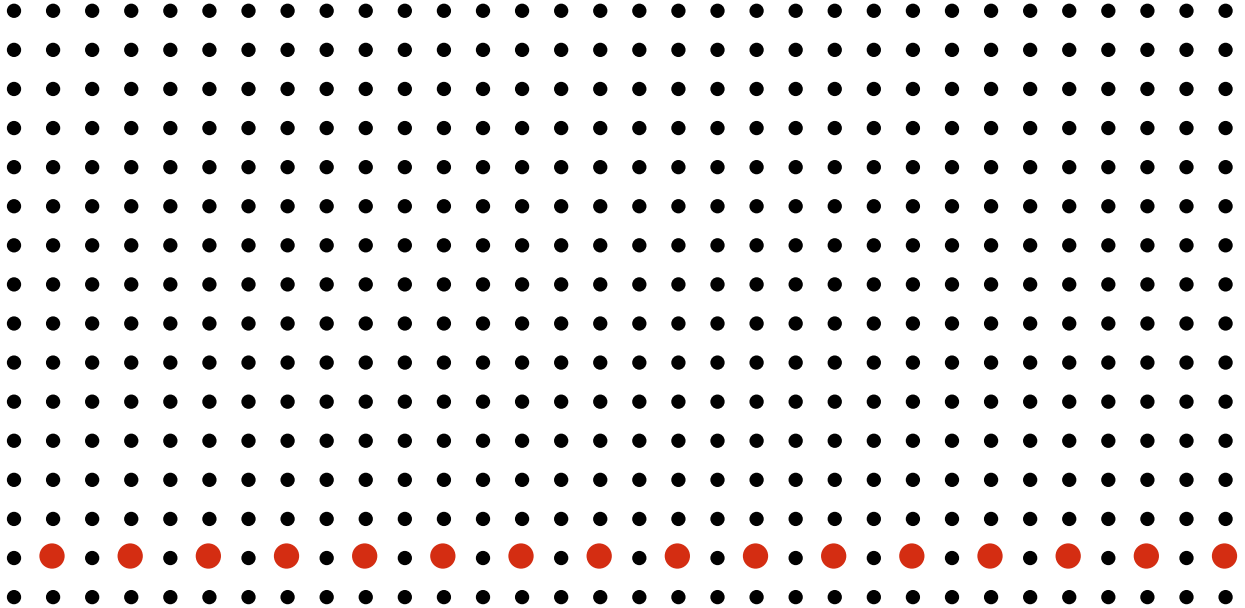

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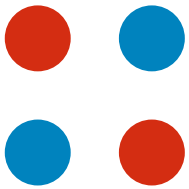

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Vectorizing QCD

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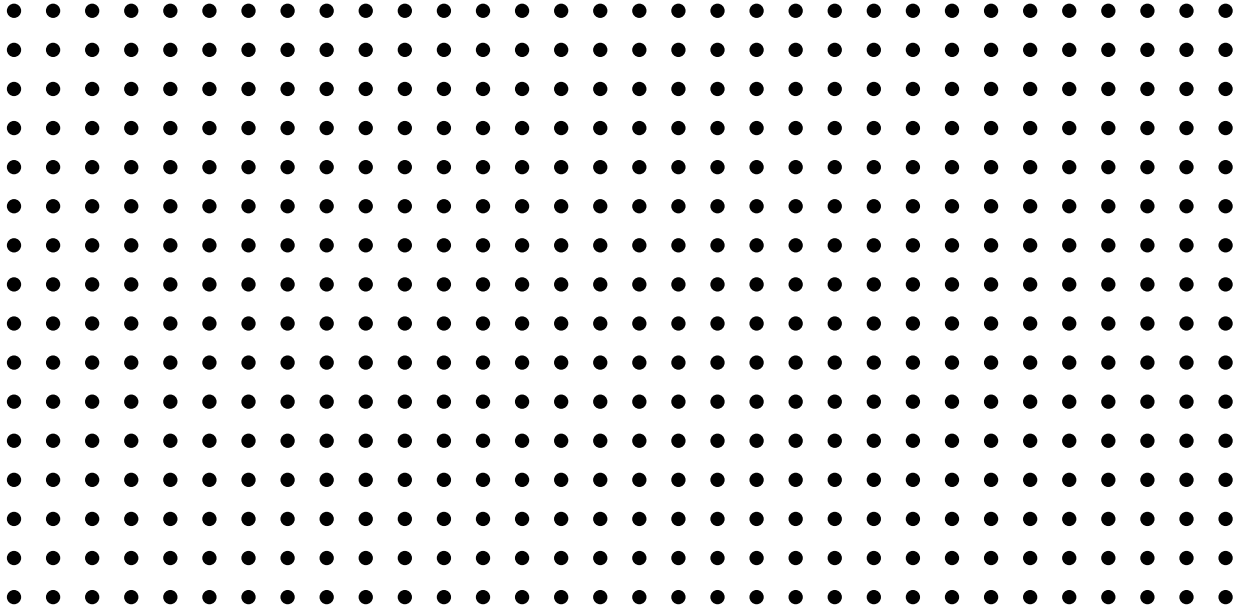
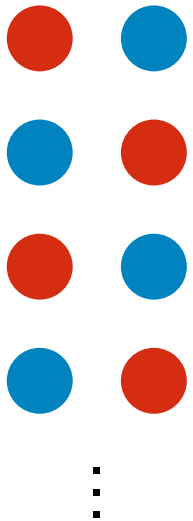
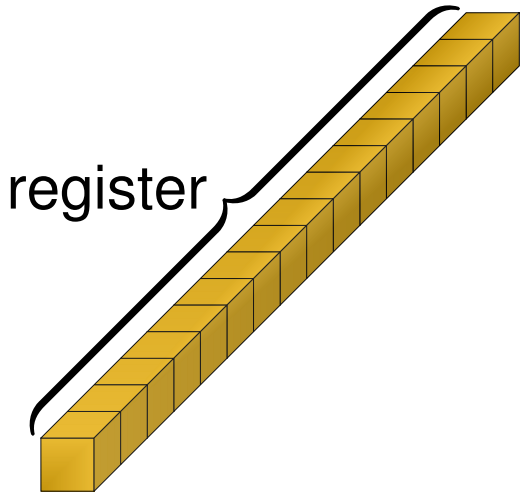


- even-odd preconditioning
  - need to fuse sites of the same parity
- fuse e.g. 16 sites (fp32, AVX512)
  - $32^3 \times 8 \longrightarrow \mathbf{2} \times 32^2 \times 8$
  - constraints on lattice size



Vectorizing QCD

Matrix-vector multiplication



Vectorizing QCD

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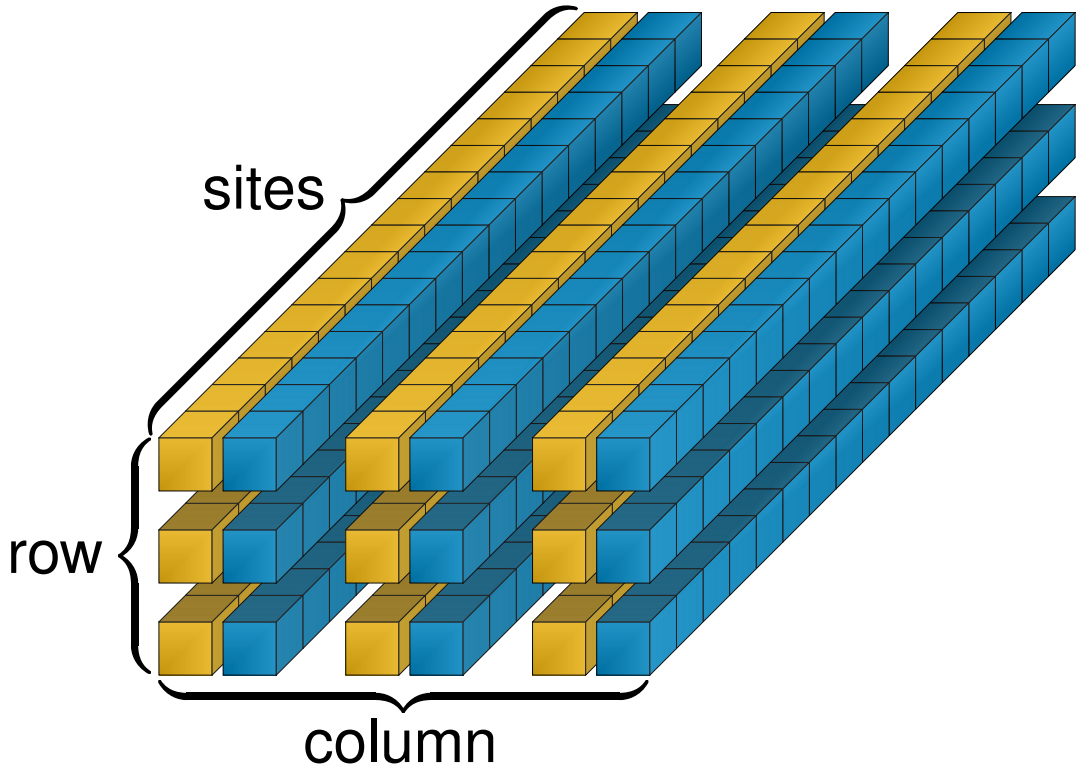

Vectorizing QCD

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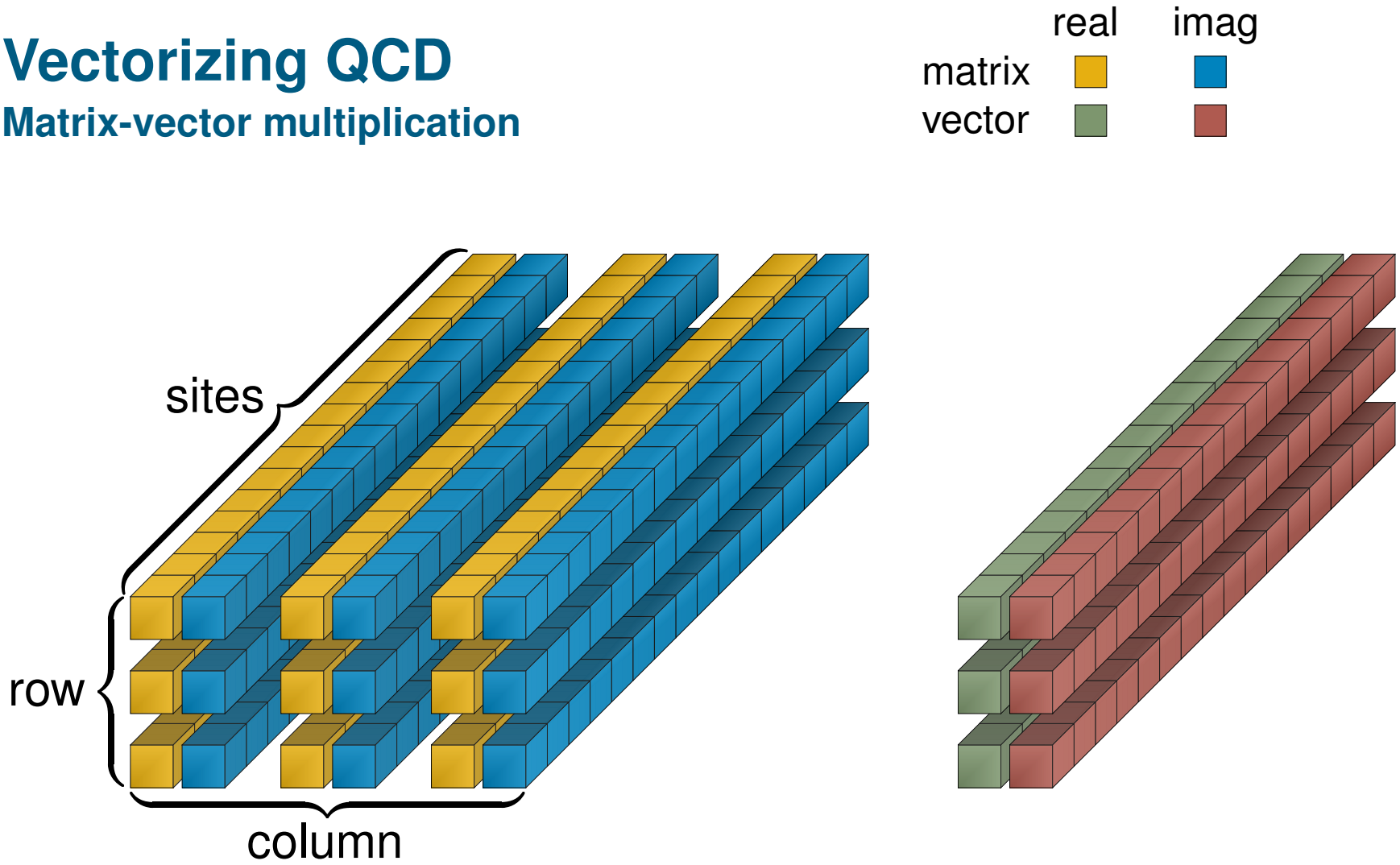

Vectorizing QCD

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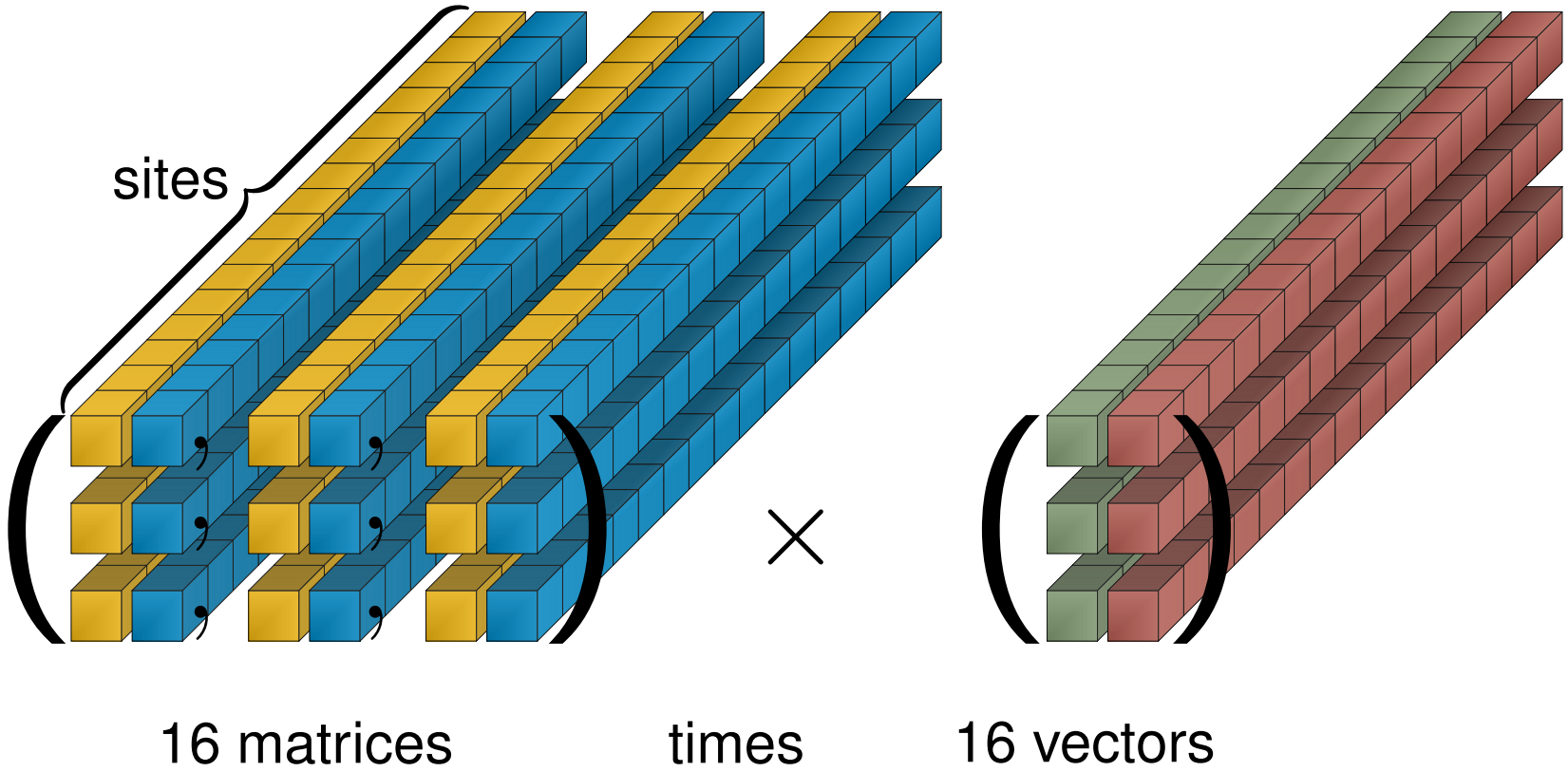
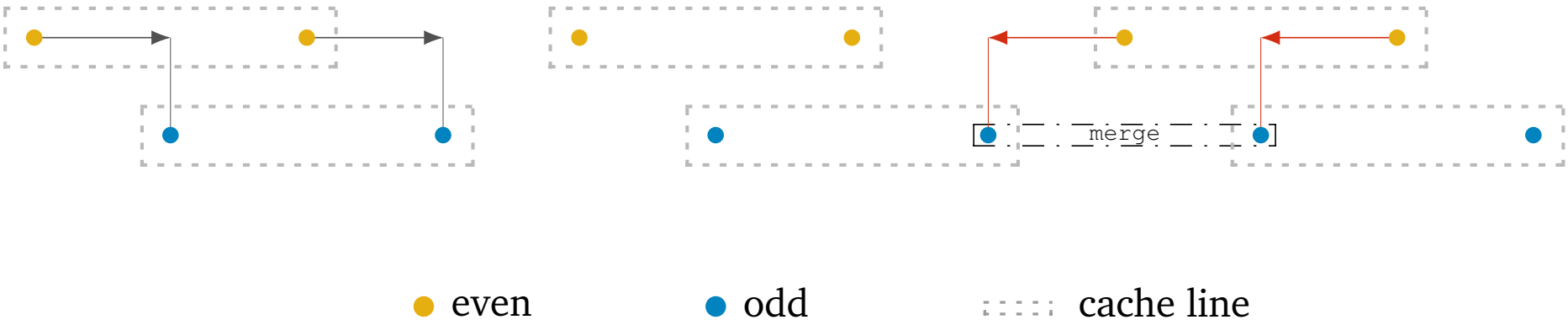
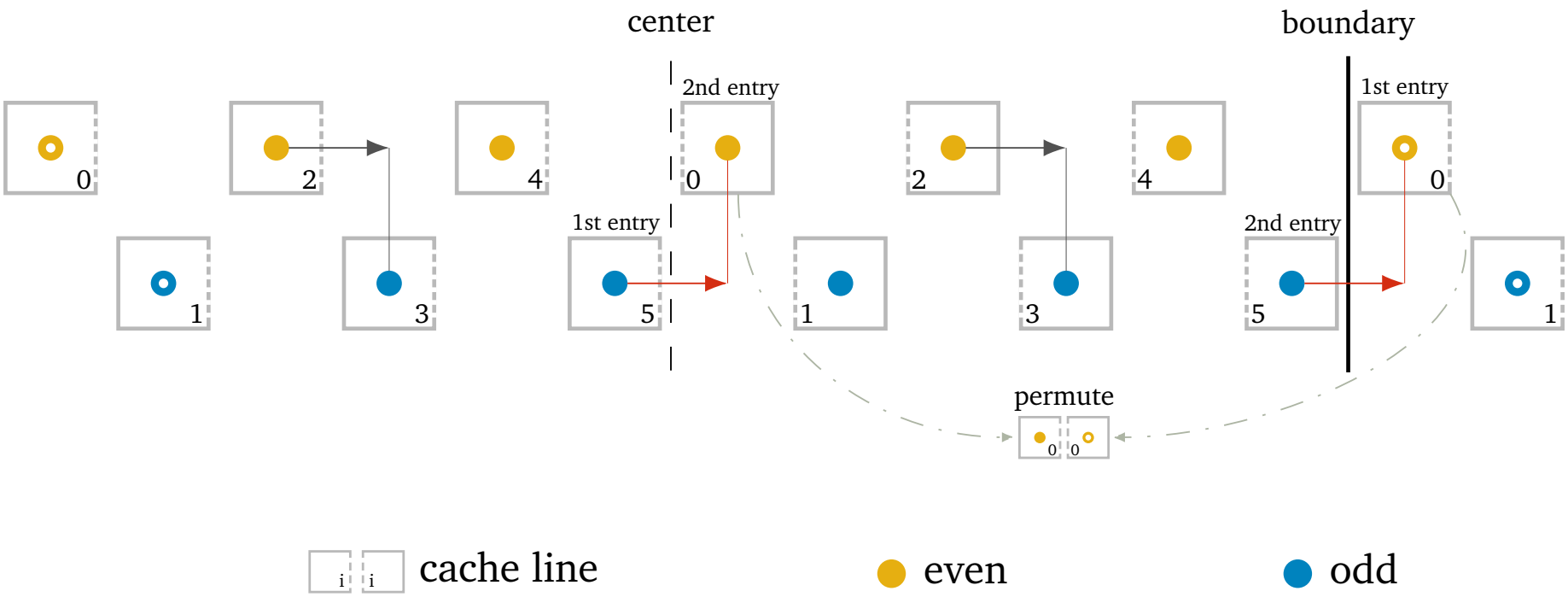


- very natural implementation $\longrightarrow$ use SIMD registers like scalars

Naive site fusion



Efficient site fusion



Performance gains on Haswell

(dual-socket E5-2698V3, 2.3 GHz, 32 cores)

Dslash, $32^3 \times 8$, 16 right-hand sides

optimizations	speedup
1 core, scalar	1x

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Thank you for your attention!

C

```
void add( double *a, double *b,
                     double *c  ) {

  for ( int i = 0; i < 8; ++i ) {

    c[i] = a[i] + b[i];
  }
}
```

Intrinsics

```
void add( double *a, double *b,
                     double *c  ) {

    __m512d a_, b_, c_;

    a_ = _mm512_load_pd( a );
    b_ = _mm512_load_pd( b );

    c_ = _mm512_add_pd( a_, b_);

    _mm512_store_pd( c, c_ );
}
```

Assembly

```
void add( double *a, double *b,
                     double *c  ) {
    __asm {

        mov rdi, a
        mov rsi, b
        mov rdx, c

        vmovapd zmm1, [rdi]
        vmovapd zmm2, [rsi]
        vaddpd zmm3, zmm2, zmm1
        vmovapd [rdx], zmm3
    }
}
```