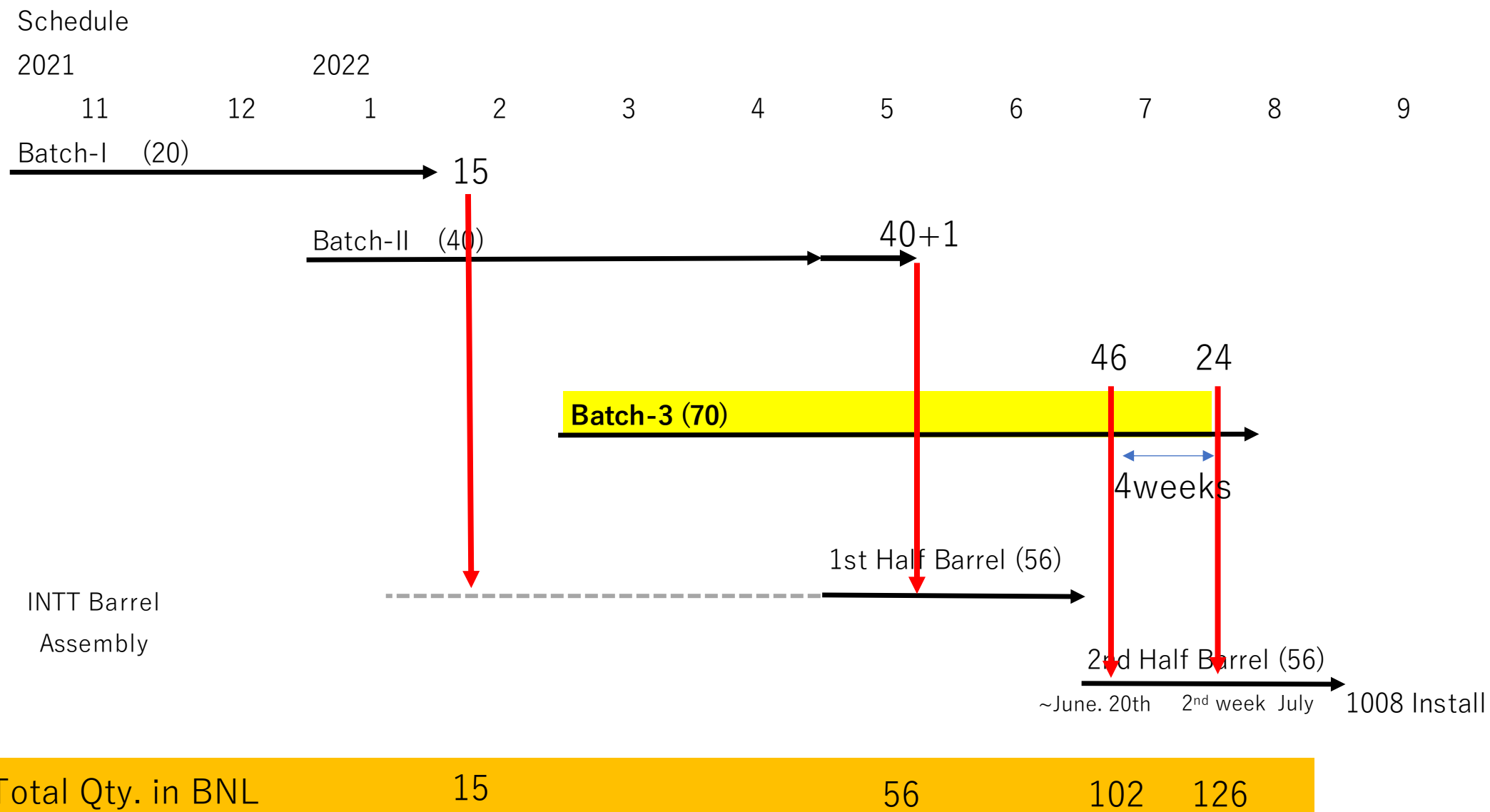


# Production Status

RIKEN/RBRC

Itaru Nakagawa

# Bus Extender Production Batch-II, III



# INTT Production Status

Today

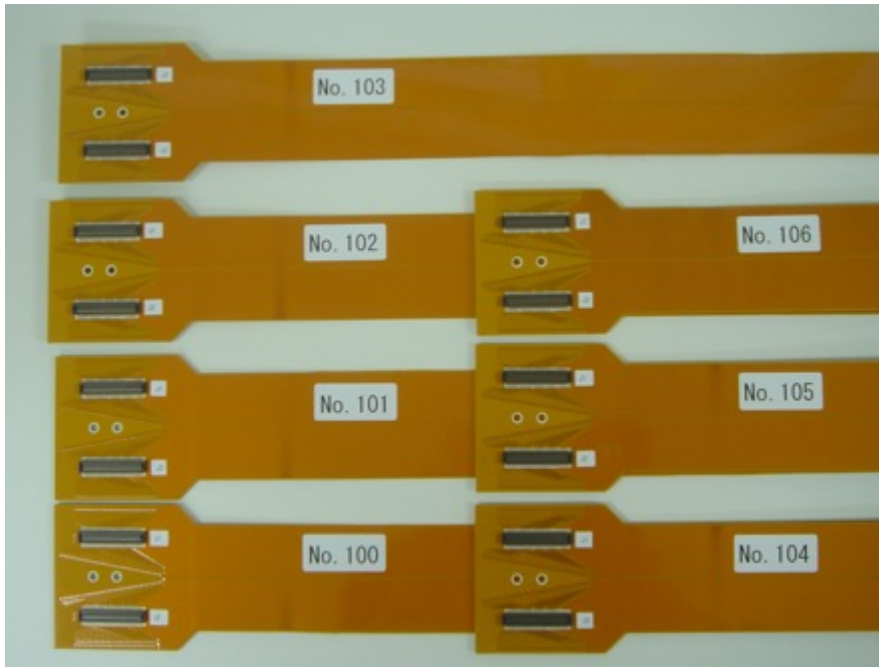
\* Beyond 112 are spares

2022	1	2	3	4	5	6	7	8	Qty*	Status
Silicon									135	Done
HDI									176	Done
Stave									204	Done
Bus Extender	Batch-1(20)								130	Production
	Batch-2(40)									
	Contract								130	Prototype
	Batch-3(70)									
Conversion Cable	Prototype-1								130	Prototype
		Contract								
									20	Prototype
Beam Clock Board	Design		Public bid						20	Prototype
Barrel Assembly										

- 46 BEX are to be delivered in week of June 20th.
- Finalize design of the conversion cable for production.
- To be delivered beam clock board by the end of of June. Cables need to be prepared

# 3<sup>rd</sup> batch bus extender LOT-1

- There are 46 (serial No. 61 ~ 106) good BEX were delivered to RIKEN on June 21<sup>st</sup> and picked up for export on 22<sup>nd</sup> as scheduled.
- Expected delivery to BNL is June 28<sup>th</sup>.



# ROC Boards Testing

- Received 4 ROC boards from BNL.
- Will inspect DF18 connectors or chips if there are any damaged ones. Then these boards are handed to Hayashi-REPC co. for the regulator upgrade and repair (June ~ July).

# Concern towards Production

Partially dropped data observation in D3 port

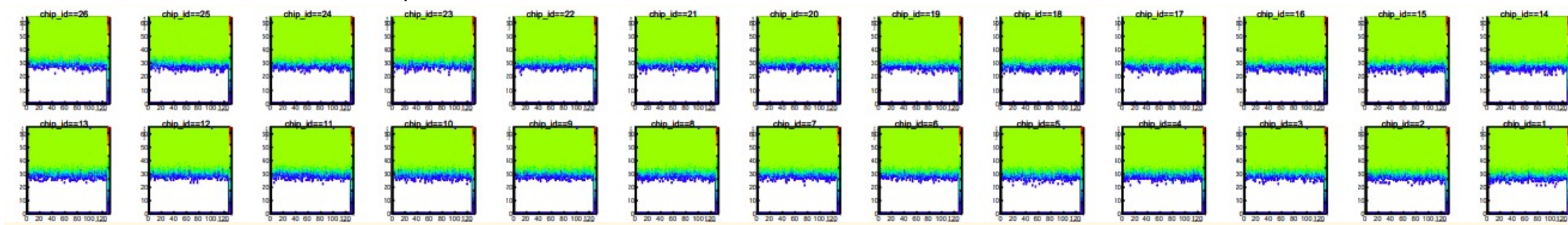


# Partially Dropped Data in Calibration

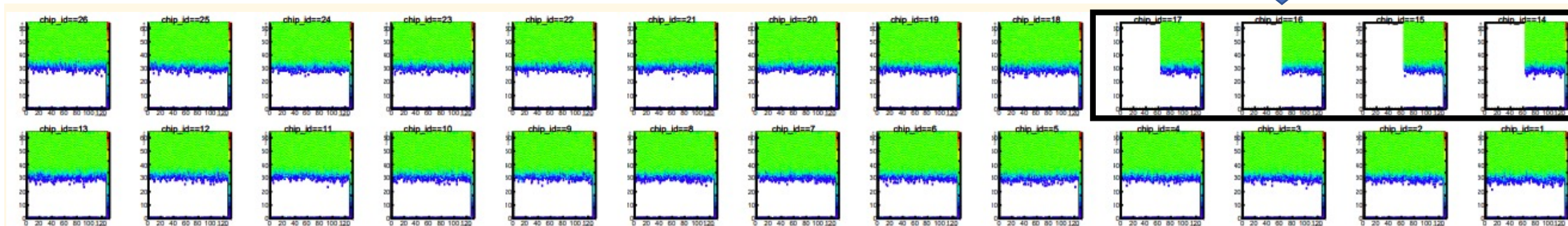


Perfect calibration in B-ports (B1, B2, B3)

Study by Hikaru Imai



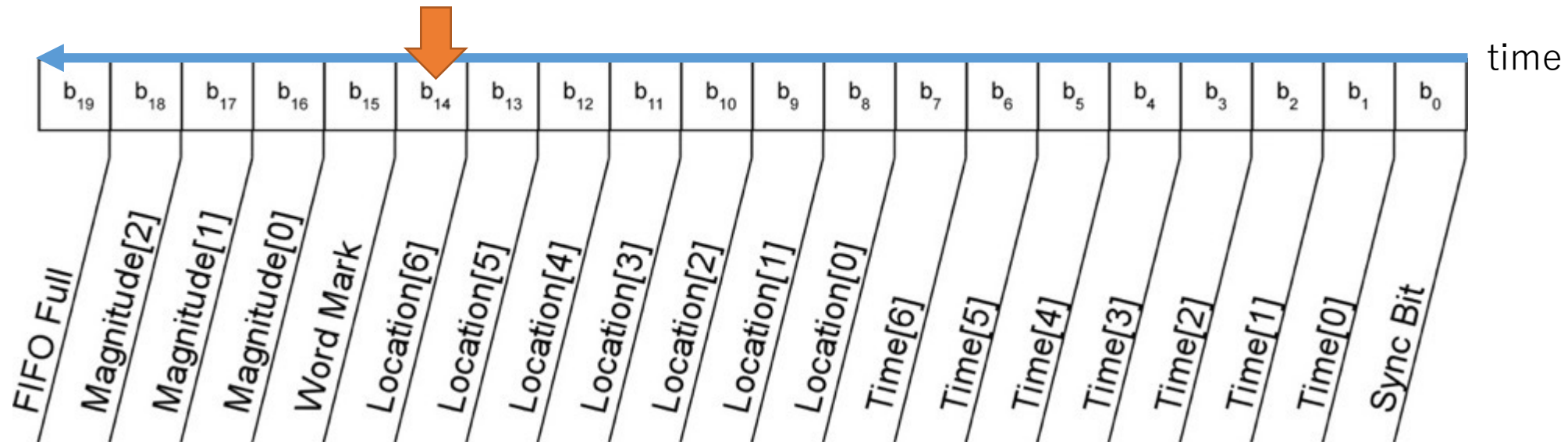
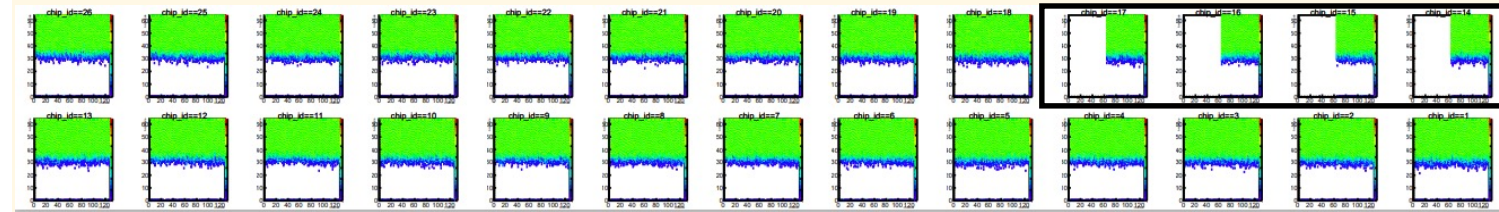
Occurs particularly in D-port of ROC.  
Worst in D3 port.



Typically, missing data strip#0~64 of Chip 14 ~17

# Strategy

1: Strip #64 ~ 127  
0: Strip #0 ~ 63



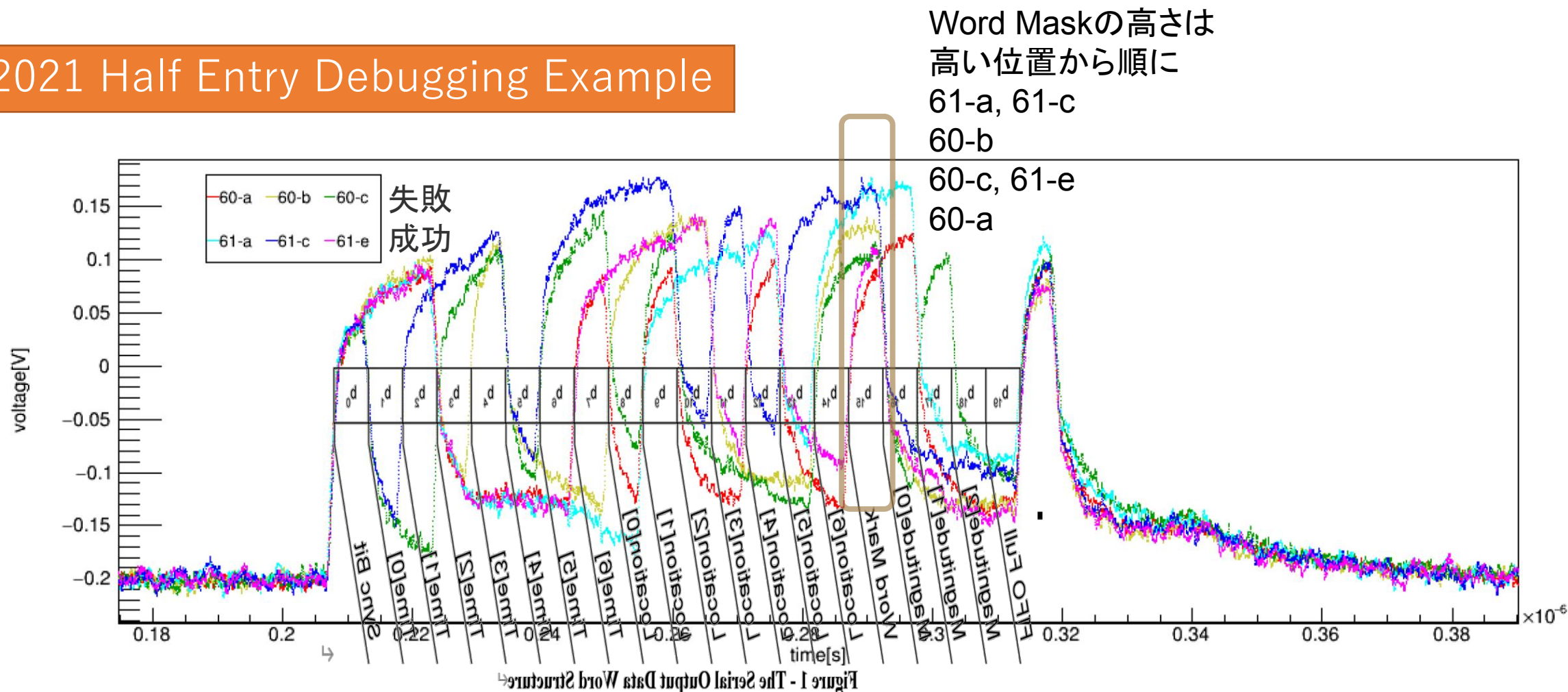
Note that in time order, the Sync bit comes out first and the FIFO full bit comes out last.

- If we observe data pattern  $b_{14} = \text{false}$ , then the problem is in down stream, i.e. data is healthy. The problem is in the ROC.
- If we don't observe data pattern always  $b_{14} = \text{true}$ , then the problem is in upstream. Most likely the initialization failure of FPHX chip. Slow control transmission issue of  $\mu$ -Coax?





## 2021 Half Entry Debugging Example



前回の20bitデータ測定(今回の条件ではこれよりも信号がはっきりしているはず。)

# Signal Observation @ D3 Port (1)

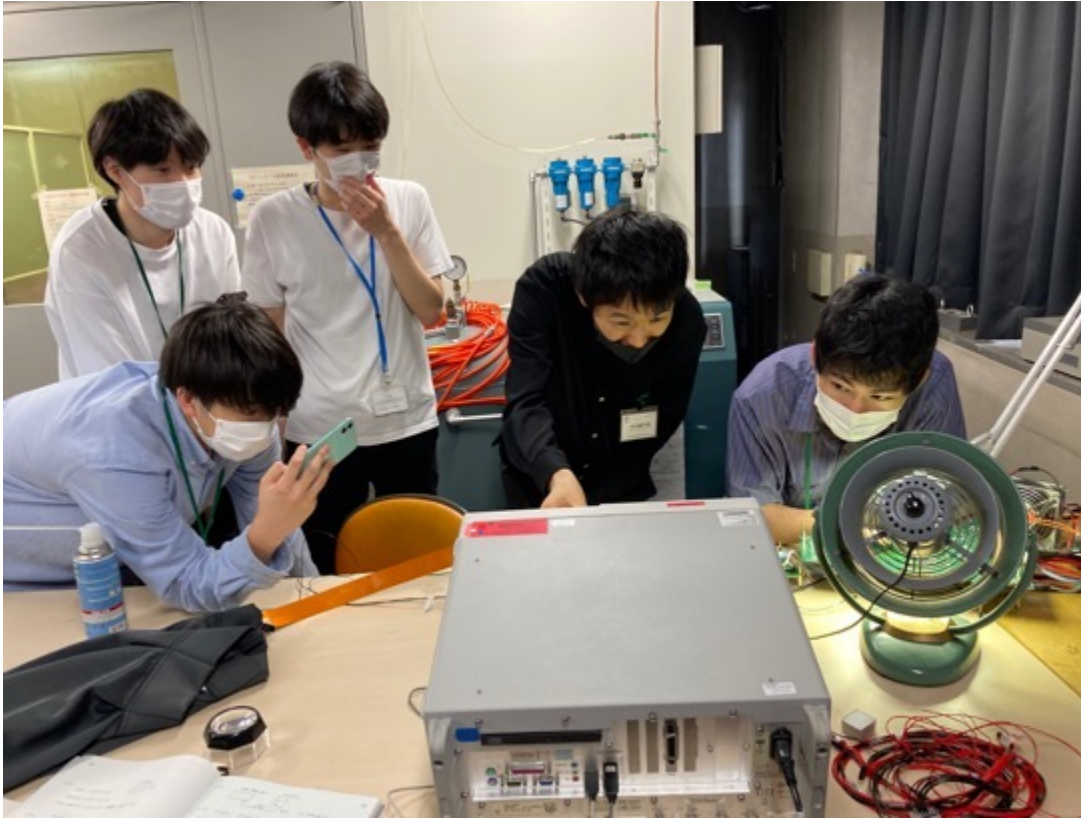
With BEX + 25cm Micro-Coax Conversion Cable



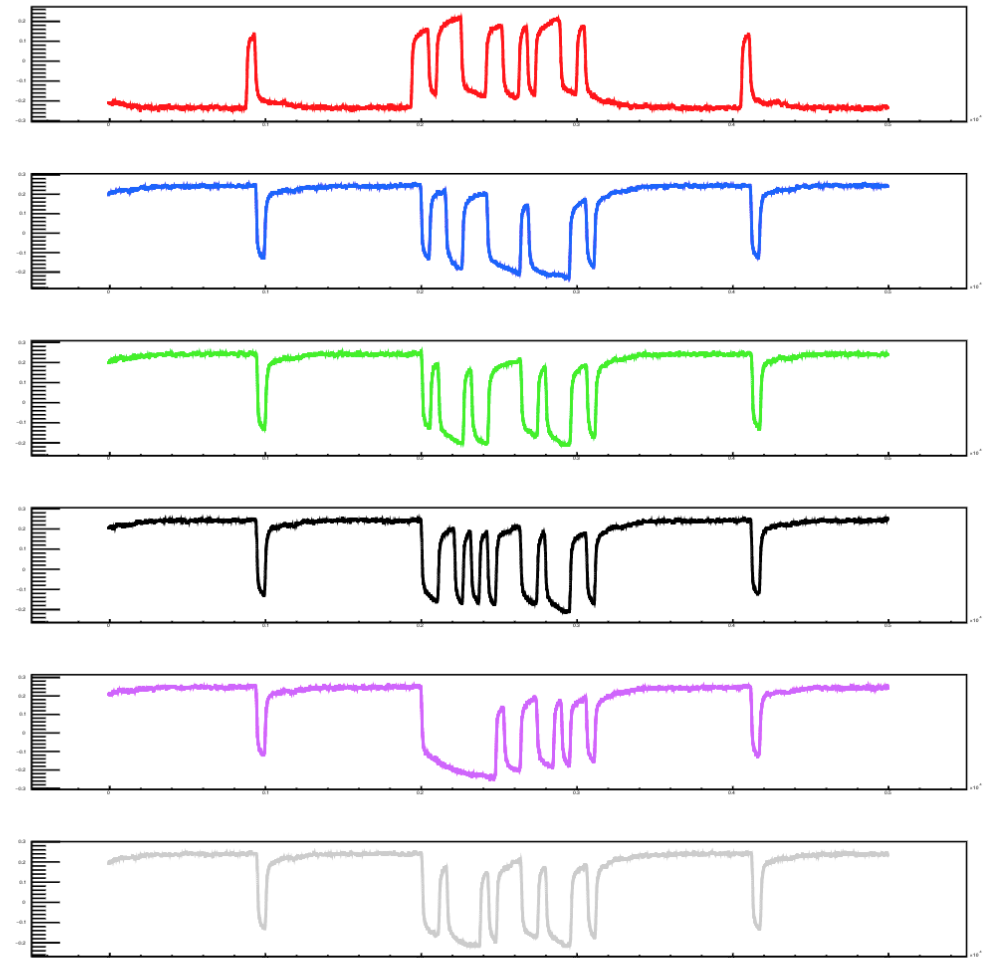
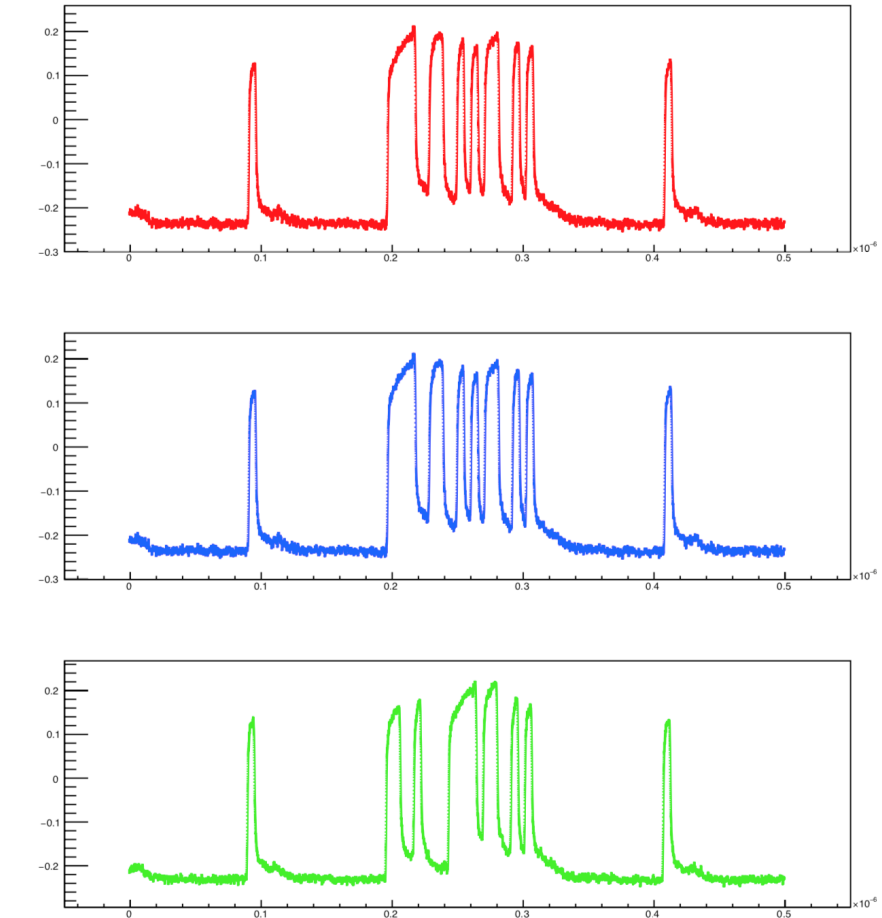


# Signal Observation at D3 port (2)

With BEX + 25cm Micro-Coax Conversion Cable



# Observed Wave Form



Plot by Hikaru Imai

Analyses are underway by Rikkyo undergrads

# INTT Collaboration Meeting



# INTT Collaboration Meeting in BNL

- Many members are going to travel to BNL this Summer.
- I would like to propose a collaboration meeting in August at BNL
- Review activities in each institutes to understand each other's work and figure out if there is anything overlooked.
- Discuss plans and schedules for this Fall and Winter.