



Timing ASIC for LGAD sensors based on a Constant Fraction Discriminator – FCFD0

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eRD112/LGAD Consortium Meeting

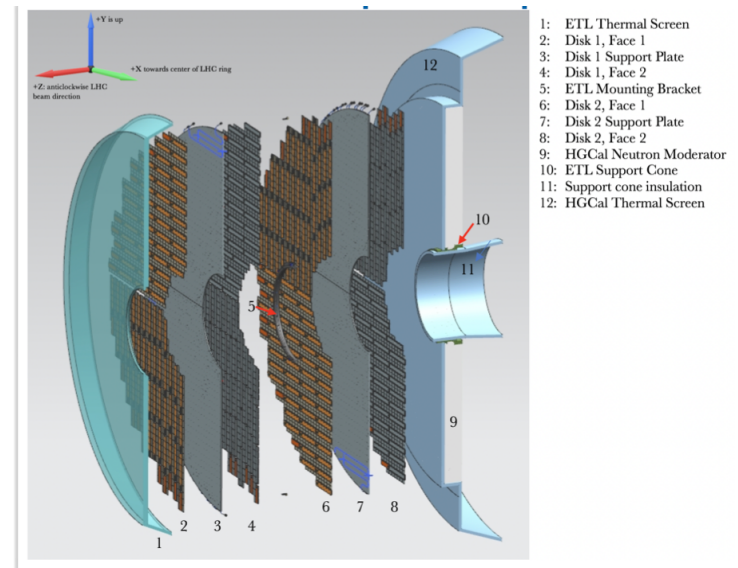
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Motivation

- The 4D-trackers will play a key role at the future machines
 - Reduce backgrounds, track reconstruction, PID, triggering all will need precision timing information, in addition to the precision position
- Next generation detectors will be more sophisticated and replace tracker
 - Development of the technologies need to start now

Measurement	Technical requirement
Tracking for e^+e^-	Granularity: $25 \times 50 \mu\text{m}^2$ pixels
	$5 \mu\text{m}$ single hit resolution
	Per track resolution of 10 ps
Tracking for 100 TeV pp	Generally the same as e^+e^-
	Radiation toleran up to $8 \times 10^{17} \text{ n/cm}^2$
	Per track resolution of 5 ps

Technical requirements for future trackers:
from [DOE's HEP BRN](#)



CMS endcap timing detector

FCFDv0: Fermilab CFD chip v0

- Goals:
 - Develop a robust fast-timing measurement technique for fast detectors
 - 30 ps time resolution or better
 - Easy to use and stable: no corrections, or repeated calibrations and threshold adjustments
 - Dynamic range $\sim 5 - 50$ fC
 - Very low dead-time after a hit (< 25 ns)
- Our approach:
 - Studied both LE and CFD approaches for AC-LGAD: “*A simulation model of front-end electronics for high-precision timing measurements with low-gain avalanche detectors*”, **NIM A 940 (2019), pp 119-124**
 - Adapt the Constant Fraction Discriminator (CFD) principle for a pixel – when paired with a TDC, *one time measurement* gives the final answer
 - Modify the classical CFD approach to eliminate the need for pixel-by-pixel trimming or compensation
 - Tailor the first design to LGAD requirements (serve an existing need)
 - General principle could be useful for other applications (beyond LGAD)

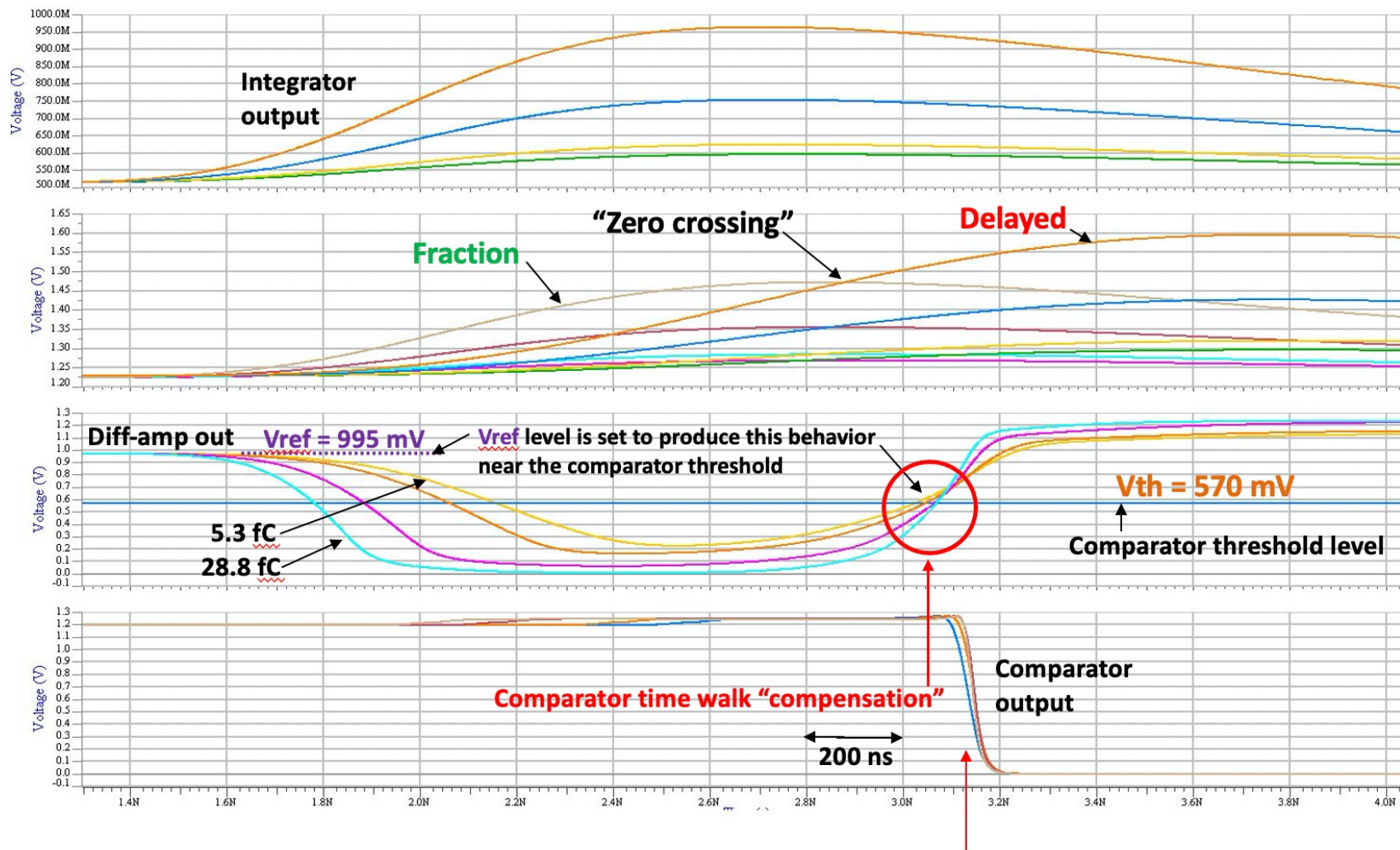
Bench-testing

- Design an on-chip charge injection circuit that can deliver a wide range of charge pulses with well-known shape and amplitude to the FCFD0 input.
 - Implement an on-chip time-to-voltage converter with precision of \sim few pS to enable easy measurement of FCFD0 output delay and jitter.
 - Establish methods to accurately measure all relevant parameters of these test circuits (to $\sim 1\%$ level), and the FCFD0 input capacitance (so we can accurately mimic the LGAD capacitance).
 - These methods should use only readily available basic test equipment (pulse generator, oscilloscope, etc.)
- Detailed report at TWEPP21:
https://indico.cern.ch/event/1019078/contributions/4443948/attachments/2277824/3938152/FCFD0_TWEPP_talk.pdf

Simulation

Apply LGAD-like charge pulse to FCFD0 input.

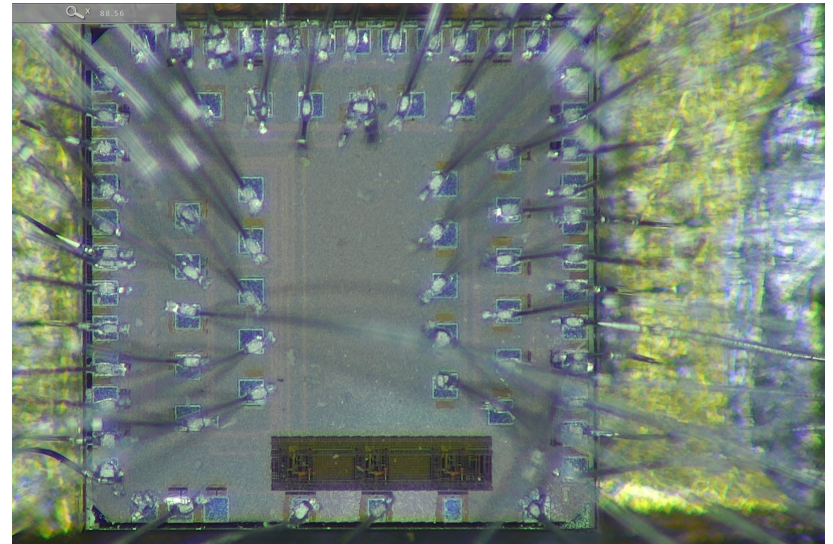
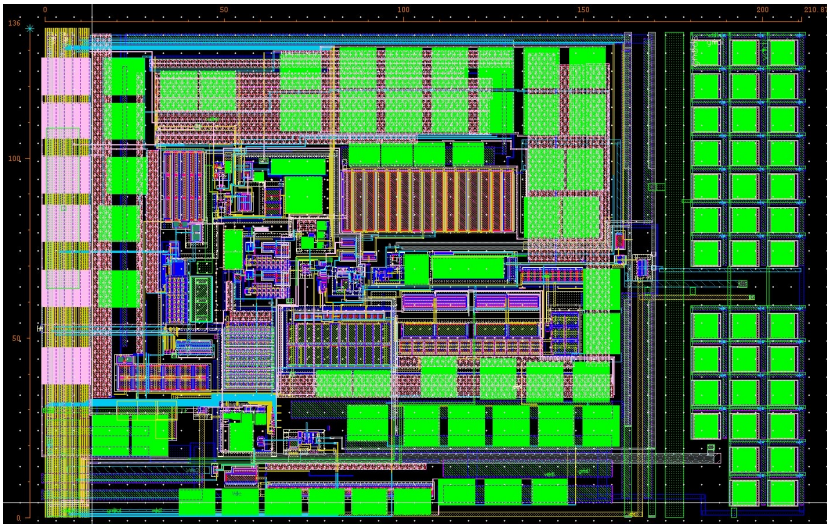
Inject 4 different amplitudes: $Q_{in} = 5.3 \text{ fC}$, 7.0 fC , 15.3 fC , 28.8 fC



Comparator output has same delay for a range of input amplitudes

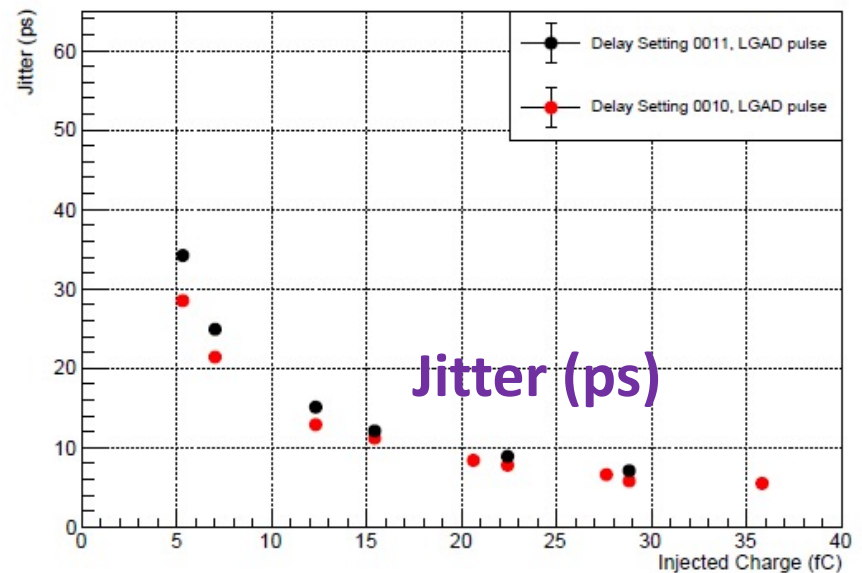
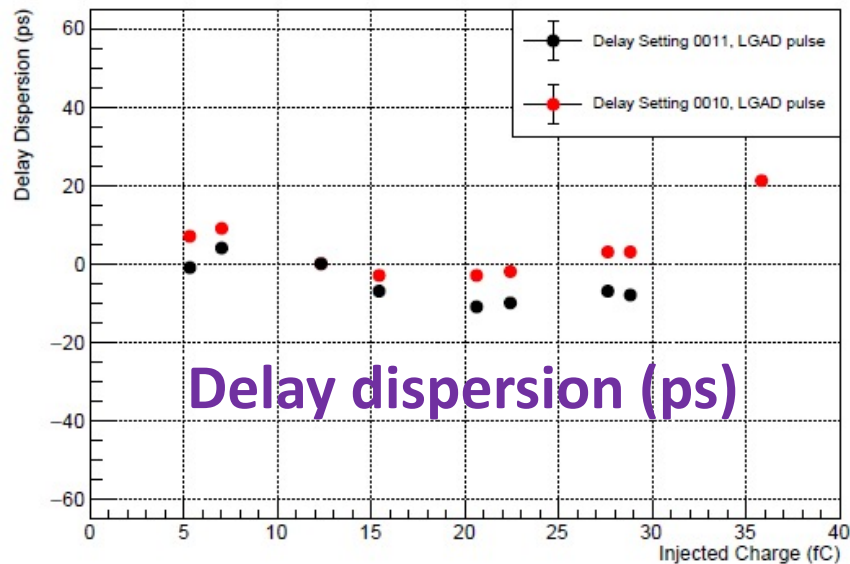
FCFDv0

- First version of the chip to test and study the approach
 - Only analog output to measure the performance of the CFD approach
 - Measurements first performed using the internal charge injection circuit



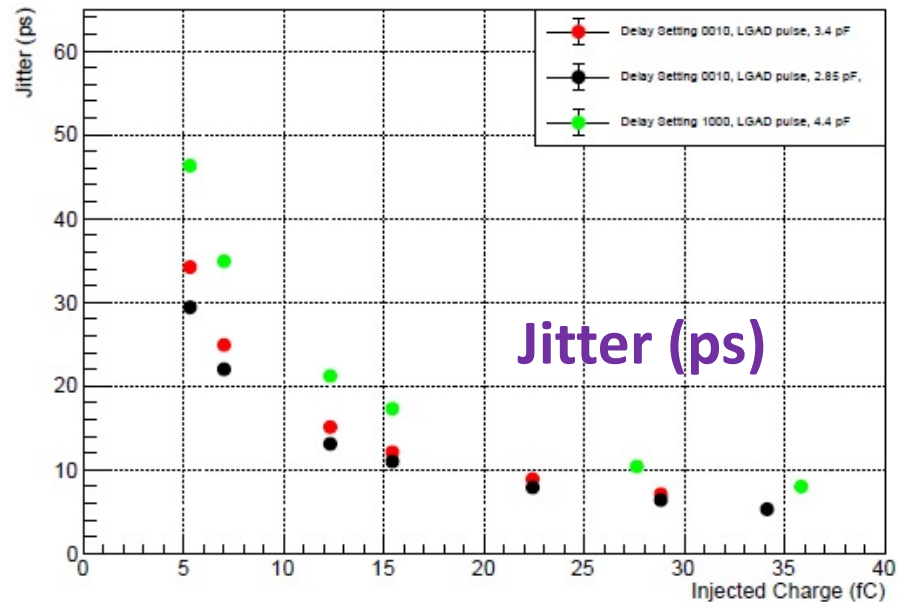
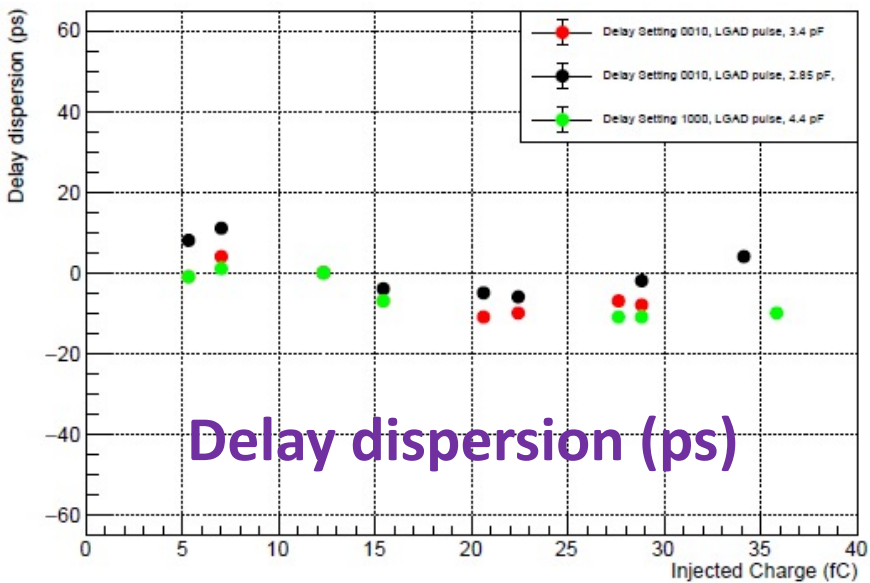
LGAD-shape injected pulse

- Measured delay dispersion and jitter vs. input charge for two different power modes



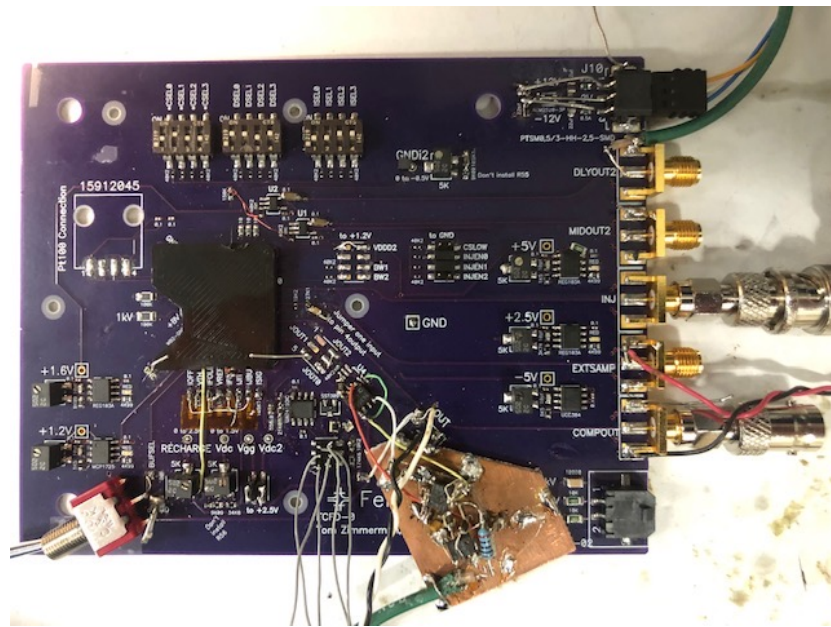
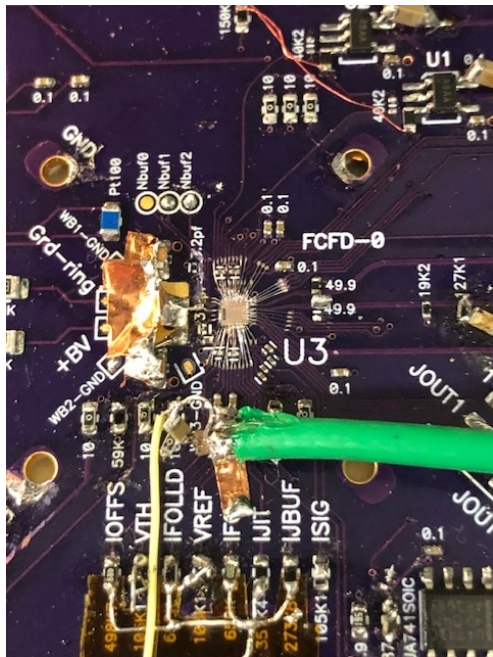
Effect of capacitance

- Vary the input capacitance from 2.850 pF to 4.4 pF



Next steps

- Characterization of FCFDv0 with beta source and test beam
 - Designed dedicated board for measurements with LGADs
 - Measurements during next two months



Next steps

- Simultaneously, working on the design of the next v1 version
 - Focus on AC-LGAD readout which needs both amplitude and timing information from each channel
 - Add measurements of amplitude
 - Multichannel chip for AC-LGAD strip detector, probably around 10 channels
- Preliminary specs from our studies of AC-LGADs

<i>Min Charge</i>	<i>Max Charge</i>	<i>Min MPV Charge</i>	<i>Max MPV Charge</i>	<i>Capacitance</i>	<i>ADC Resolution</i>
2 fC	64 fC	15 fC	25 fC	0.5-10 pF	10%

Summary for FCFDv0

- Good performance for the first generation CFD-chip produced in TSMC 65nm technology node
 - Precise measurements and calibrations of the chip on a bench, stable operations, low dead time
 - Consistent with simulations: ~ 30 ps at 5fC, and < 10 ps at 30 fC, with LGAD-like pulses
- Now moving on to testing with LGAD signals
- Development of the next version is starting, targeting specifically AC-LGAD signals to achieve good timing and position resolutions