ALD review of sPHENIX TPOT Electronics -

Takao Sakaguchi

Jul 20, 2022

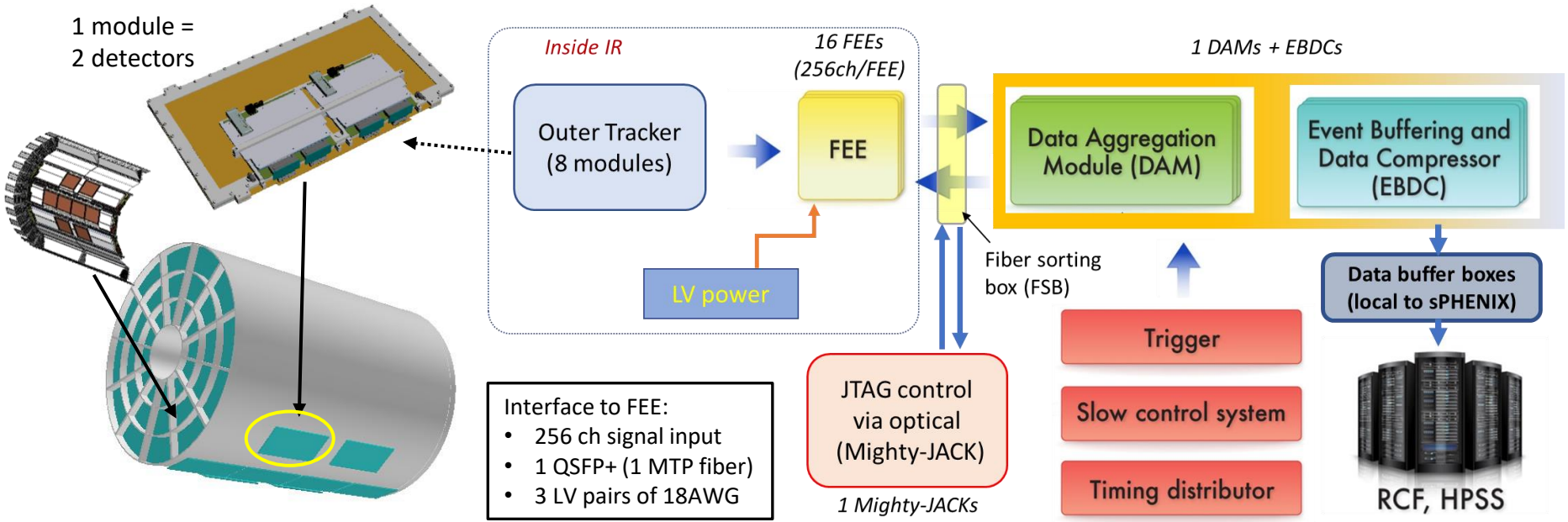
BNL

Topics to be covered in this talk

- Front and back-end electronics for signal readout
  - **Boards: FEE, DAM+EBDC, Mighty-JACK**
- Interface to the detector, optical fiber cabling, and fiber sort-out-box
- Low-voltage (power supplies, cabling), High Voltage
- Cost and Schedule
- Status and Highlight
- Summary

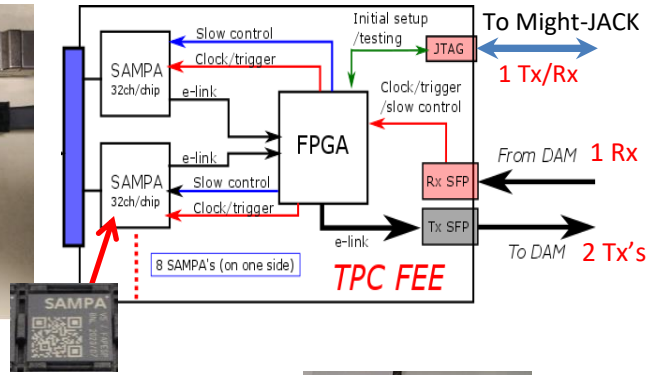
TPOT readout overview

- Readout scheme is the same as the one for TPC
  - Digitize analog signal from the detector, and send them to backend electronics (DAM) via optical cable
  - 2 FEEs (512 channels) per module, 16 FEEs in total (vs 624 FEEs for the TPC), 1 DAM+EBDC
    - **Input capacitance (C_{det}) per channel (or strip): 150-200pF (vs 18pF for the TPC)**
  - 1 JTAG control of FEE over optical cards (Mighty-JACK cards with fiber sort-out-box)



Technical overview of boards

- FEE (256 channels per board, 20W heat)
  - Continuous readout mode
  - 8 SAMPAv5 + 1 FPGA + 1 QSFP (4 Tx/Rx)
    - **SAMPA: 32 of (CSA + Shaper + FADC + DSP)**
    - **Optical: 2 Data links (4+ Gbps/line) + 1 JTAG**
  - 80/160 nsec shaping, 30/20mV/fC gains
  - ADC Sampling: 4.7/9.4/18.8MHz
  - FEE works fine at 1.5T and 100krad

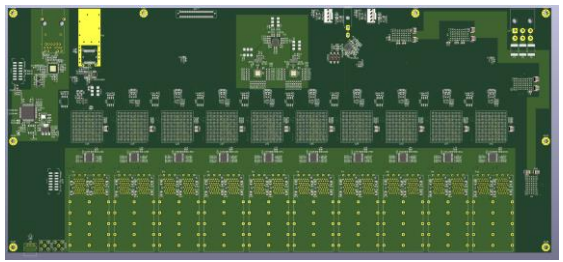


- DAM/EBDC
  - ATLAS FELIX v2.1 card (PCIe Gen3 x16), hosted by a commodity server.
    - **48 Optical Tx/Rx (10+ Gbps/line) and Xilinx Ultrascale FPGA (XCKU115)**
  - Reducing data via triggering and compression

FELIX v2.1 card

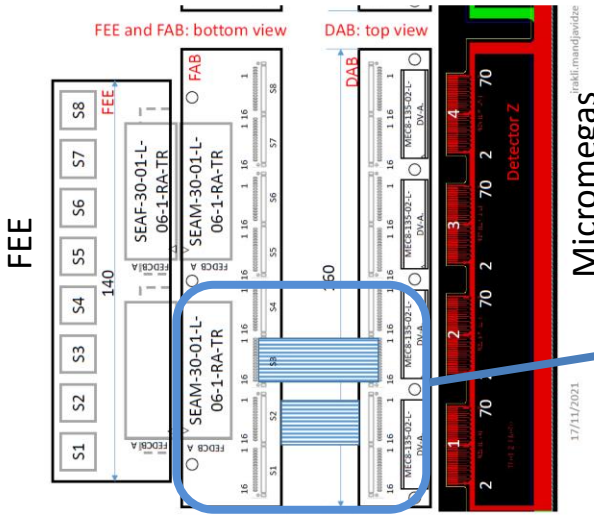
Commodity Server

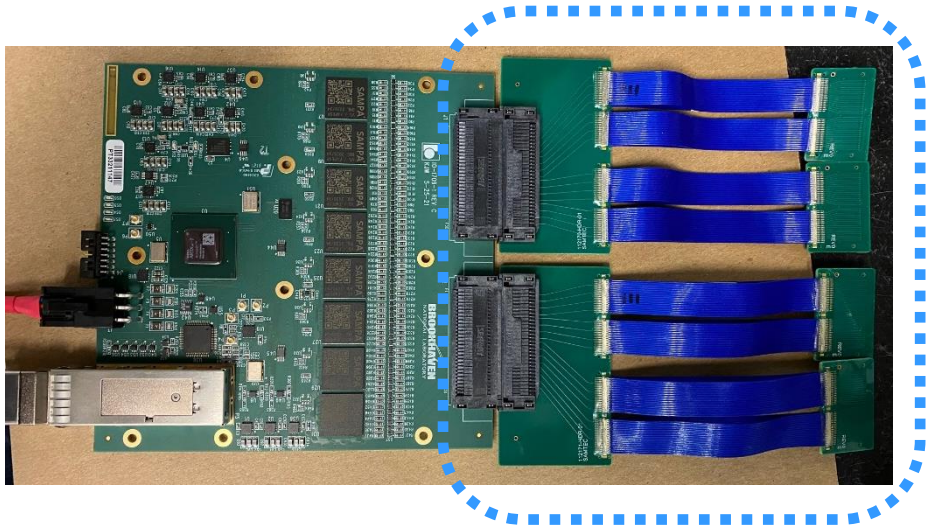
- Mighty-JACK
  - JTAG connection to FEE over optical fiber
    - **10 Xilinx Artix-7 FPGA with 40 Optical Tx/Rx**



Detector interface cable

- To interface with the FEE, an adaptor cable between Micromegas and FEE is necessary
  - MEC8 connector at TPOT side, and SEAM connector at FEE side (both from SAMTEC)
- Designing with a SAMTEC engineer started in Nov 2021
  - The FEE side has two type of boards, mirror of each other.
  - All the cables (25 + 25) have been delivered. All of them have been tested fine.

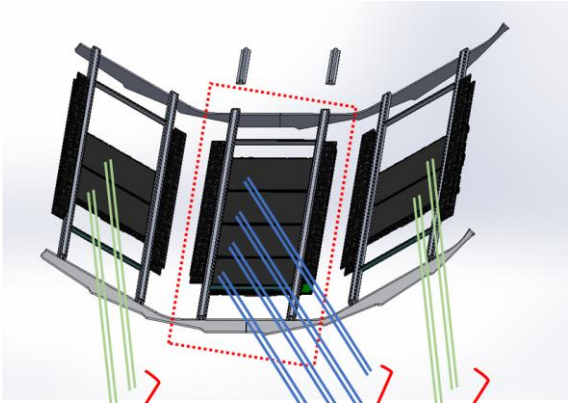


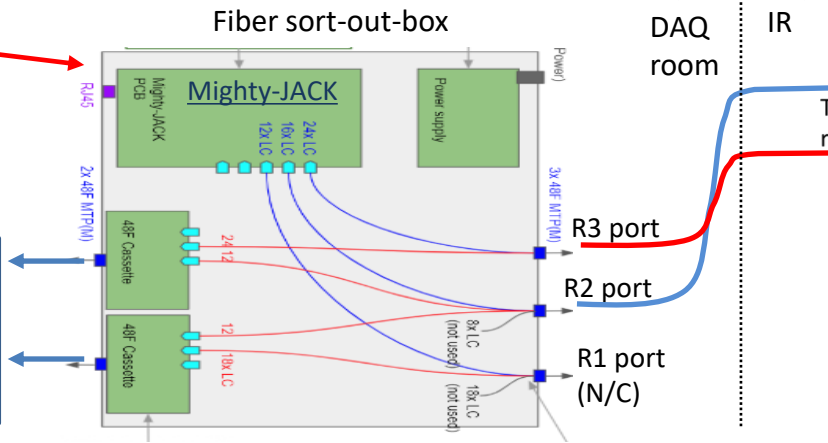


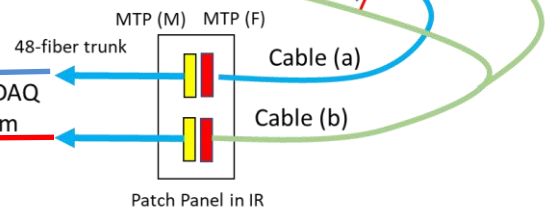
Initial concept by Irakli Mandjavidize

Technical overview (fiber layout)

- QSFP+ fibers from each FEE to the fiber patch panel
  - 10 QSFP+ fibers from North and South each (yet to be ordered)
  - At the patch panel, QSFP+ cables are interconnected to 48-fiber MTP trunk cables using the breakout cables below made for TPC
    - **(a): 1 MTP <-> 8 QSFPs, (b): 1 MTP <-> 12 QSFPs**
  - All the breakout cables have been delivered
- Two 48-fiber MTP trunk cables run from the patch panel to the fiber sort-out-box in the DAQ room





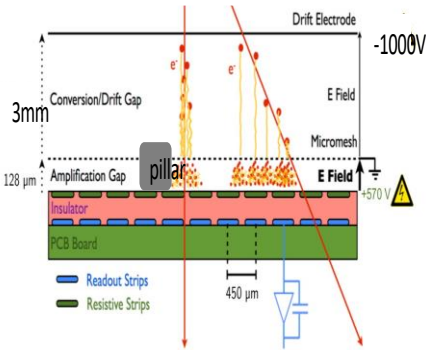


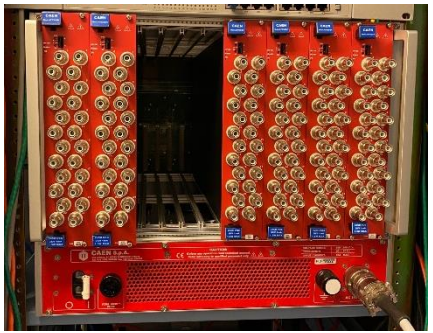
MTP – QSFPs breakout cable

Low/High Voltages

- TPOT uses spare channels of TPC LV system
  - Cable lengths from LV rack to TPOT modules have been fixed. Cable delivery will be completed within a month (together with those for TPC)

- TPOT uses both positive and negative high voltages.
  - 1 negative HV for electron drift per detector
  - 4 positive HVs for amplifications per detector
- 8 modules (= 16 detectors) need 16 neg. and 64 pos. HVs
  - We selected a CAEN HV system (delivered)
    - **One main frame + two 24-ch neg. + four pos. modules (+/-3kV, 1mA in max.)**
  - HV cable lengths and routing are being worked on.
  - HTML-based control software already exists.
  - Interface to sPHENIX OPC server is in progress





Schedule Drivers

- TPOT electronics relies on surplus from TPC production
  - 700 FEEs have been fabricated and are under testing. 624 FEEs will be used for TPC
  - All the FELIX boards have been produced. They are under testing
    - **Leftover from TPC will be 76 FEEs and 6 FELIXs.**

- Current initial test of the FEEs tells that the yield is 90-95%
  - All the failed boards have same symptom. They are related to the SAMPA power-on procedure.
  - We are working on solving the issue mainly by updating the FEE FPGA firmware.
    - **Once successful, the end yield will be very close to 100%**

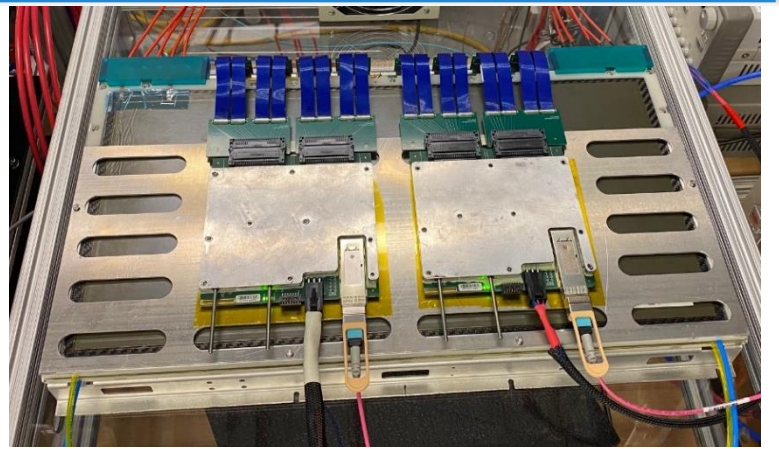
- Items subject to schedule drivers include:
  - Engineering of HV cables, and optical fibers (to be finished in ~2 weeks).

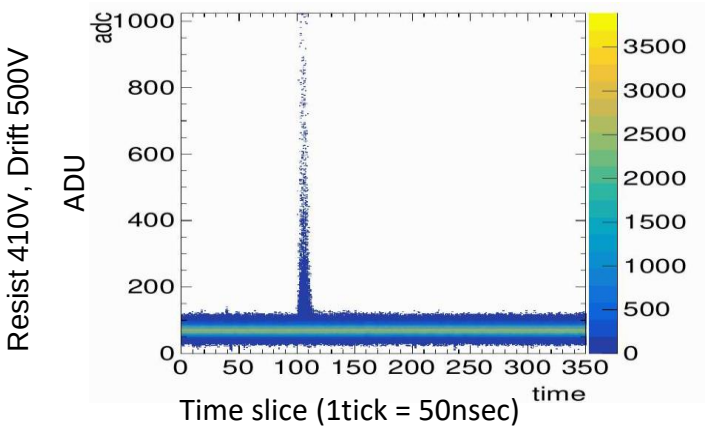
Cost Drivers

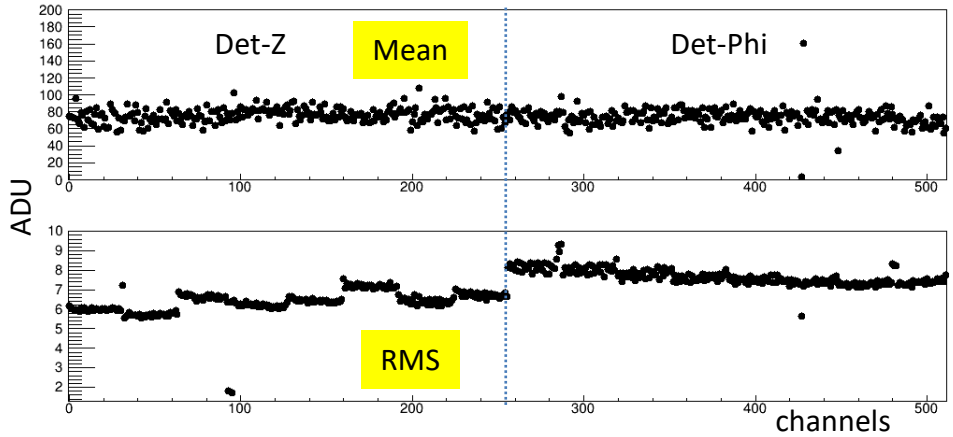
Item	Estimated	Actual	comments
FEE boards (16 FEEs)	$7k	$0	Use surplus from TPC
One set of FELIX+EBDC	$14k	$0	Use surplus from TPC
Mighty-JACK board	$2k	$0	Use surplus from TPC
Fiber sort-out-box	$3k	$0	Use surplus from TPC
Signal interface cable	$21k	$21k	Delivered
HV modules and mainframe	$37k	$37k	Delivered
HV cables (100, SHV)	$17k	$17k	To be delivered
LV power system	$2k	$0	Use surplus from TPC
Optical fibers	$3k	$3k	To be delivered
Total	$106k	$78k	

Status and Highlights

- First production detector has been assembled with a frame, FEE, and transition cables.
- Pedestal of all the channels have been measured with this setup
  - Noise at 160nsec, 20mV/fC is ~7 ADU (= ~4500 e).
  - Only ~3 out of 512 channels have issue (0.6%)
- We confirmed that there is no oscillation from a comic ray test.







Issues and Concerns

- Most of the items have been procured, but there are few items yet to be procured
  - **Given the global supply chain issue, we will order as soon as possible, and keep watching the situation**

- FEE production yield should be more than 92% to cover needs of both TPC and TPOT (624 + 16 = 640, out of 700 assembled in total)

Summary

- Technical designs are all fixed.
  - **Most of the items have been procured.**
  - **Cost: $78K**

- Prototype Micromegas has been connected to FEE and is under testing
  - **Noise has been measured for fully-assembled TPOT setup.**
  - **Cosmic signals have also been observed**
  - **No worrisome oscillation is seen despite 10x higher capacitance compared to TPC.**

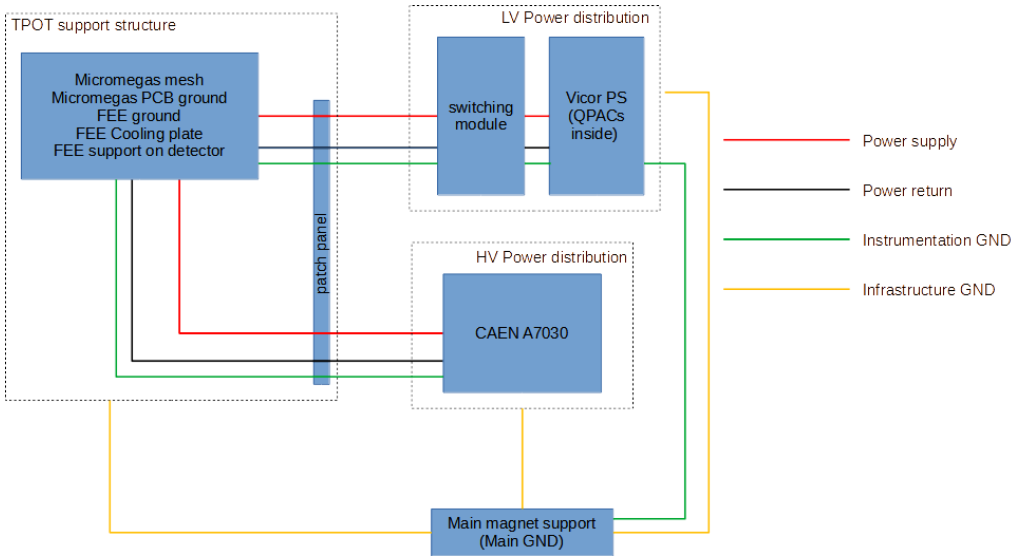
- All the FEEs will be tested ready for TPC by mid-Aug 2022
  - **Current yield of the FEEs is 90-95%. The symptom are same for all failed boards and are related to SAMPA power-on procedure.**
    - **We are working on solving this issue mainly by updating the FEE FPGA firmware.**
  - **No issue in terms of schedule**

Back Up

Technical overview (Grounding)

Hugo Pereira Da Costa

- TPOT support structure and racks are connected to infrastructure ground
- Instrumentation ground is brought to the detector via LV power return.
- HV power lines are floating. Power return is connected to the instrumentation ground at detector.
- FEE PCB, FEE cooling plates, FEE support, Micromegas mesh and PCB ground are all connected to the instrumentation ground at detector
- Detector ground (= instrumentation GND) isolated from support structure (= infrastructure GND)



FEE Technical Overview

- **Continuous readout mode**

- Use of 8 SAMPA chips per FEE (256ch/FEE)
  - **SAMPA = CSA + Shaper + FADC + DSP**

- Use of newly developed SAMPA v5 that has 80nsec shaping time option.
  - **160nsec is also available**
  - **SAMPA v5 chip production is finished.**

- FPGA receives data from SAMPA and sends to optical link, and processes clock and slow control data from DAM.
  - **JTAG is now implemented over optical link.**
  - **Two data links are available**

- ADC clock will be 4.7, 9.4 or 18.8 MHz, as we base on the RHIC beam-crossing clock.

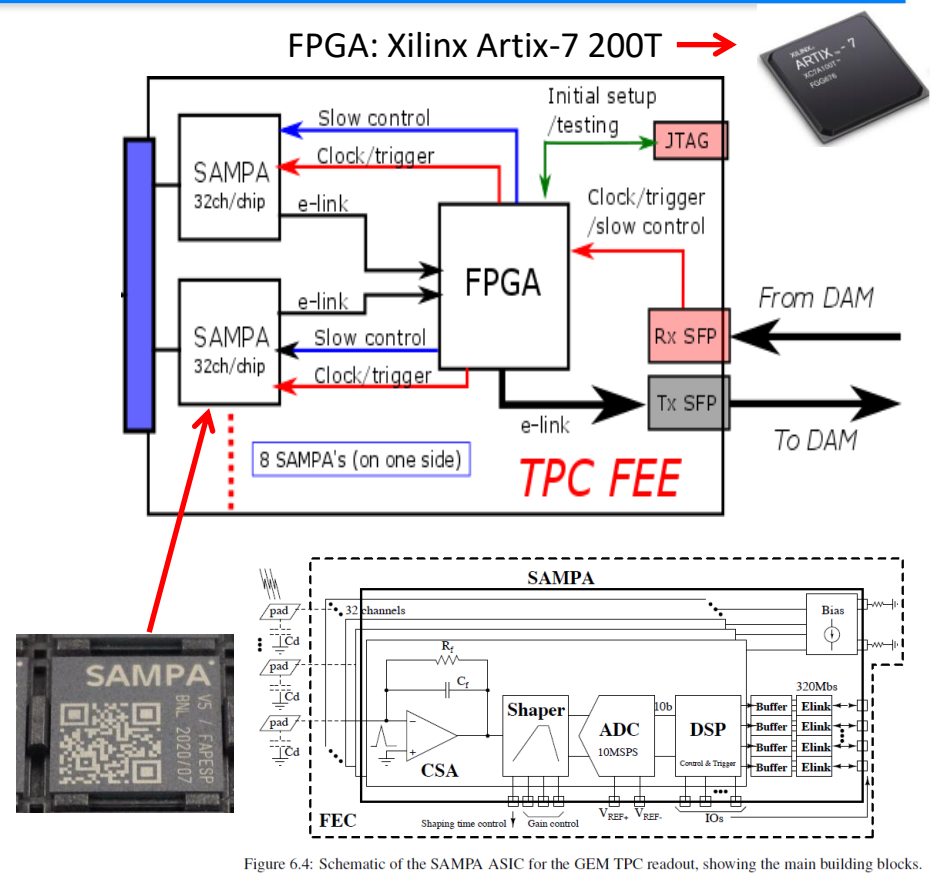


Figure 6.4: Schematic of the SAMPA ASIC for the GEM TPC readout, showing the main building blocks.

Single event effect on FPGA

- Xilinx Artix-7 7A200T FPGA
- Assuming all CRAM bits are significant
- Used AMPT event generator (Au+Au 200GeV @100KHz) to estimate charged hardron rate at particular positions.
- Triple modular redundancy (TMR), memory scrubbing is implemented

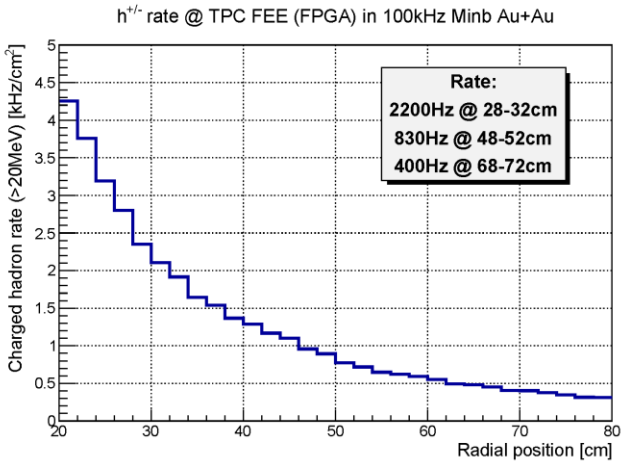


Table 2.7: Soft error for sPHENIX TPC FEE case (using Artix-7 7A200T).

R-position	# of FEE	flux [Hz/cm^2]	error/FEE [s^{-1}]	error/sector [s^{-1}]
28-32cm	120	2200	1.6×10^{-6}	1.9×10^{-4}
48-52cm	192	800	5.8×10^{-7}	1.1×10^{-4}
68-72cm	288	400	2.9×10^{-7}	8.6×10^{-5}

One error in 45 minutes as whole TPC

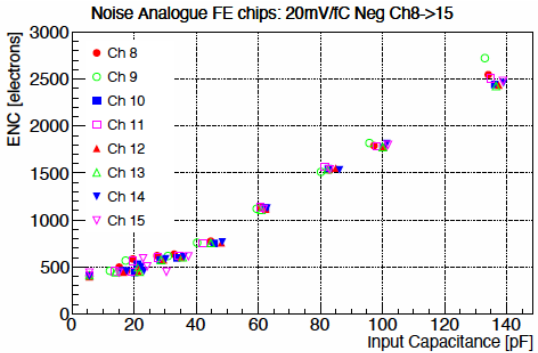
25kRad TID for 5 years.
1.2 10^{12} 1MeV-eq n/cm^2

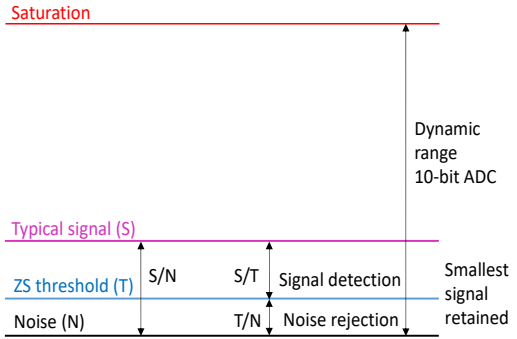
Expected signal and efficiency

Irakli Mandjavidize

- Mean E_{dep} is 500 eV. (initial N_e is 18.6)
  - **Highest input signal is 11 [fC]**
  - **Primary shaping time and gain choice: 160nsec and 20mV/fC**
  - **Saturation possibility due to a long tail of E_{dep} distribution:**
    - **3.7% cases @ 8 000 detector gain**
    - **5.8% cases @ 10 000 detector gain**
- Capacitance per strip: 150-200pF
  - **10x of that of the TPC**
  - **Measurement of noise exists at 140pF**
    - **→ ~ 3500 e@200pF = 0.56 fC**
  - **Need to confirm that FEE works at this capacitance**
- Zero-suppression threshold (T) to noise ratio determines minimum detectable E_{dep}
  - **Noise is independent of MM gain.**
  - **Working point has been identified in terms of MM gain, T and N.**

TWEPP16





Signal detection efficiency for a given detector gain

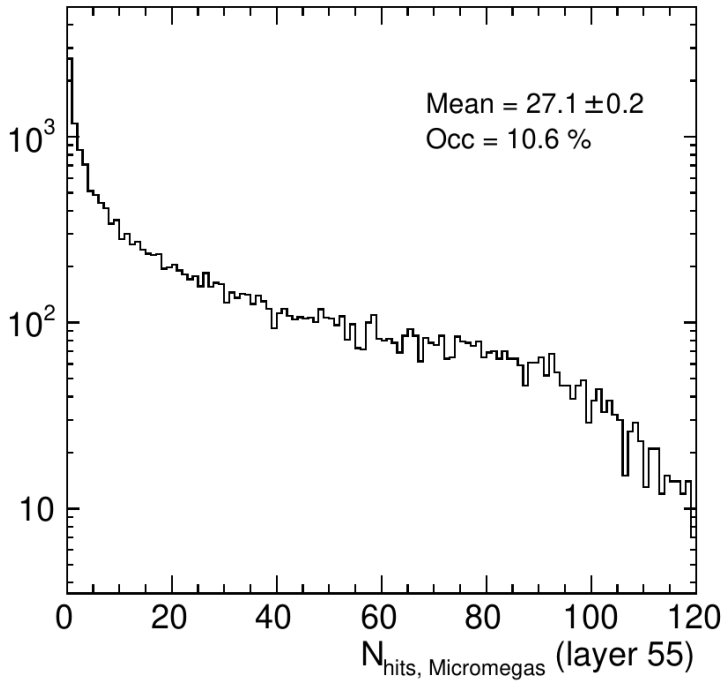
Red: uncomfortable

Gain0	S / N	T / N	Min energy eV	Min detectable energy / full energy %
8 000	19.6	3	50	9.9
		4	66	13.3
		5	83	16.6
10 000	24.5	3	40	8.0
		4	53	10.6
		5	66	13.3

Expected data rate

- Data rate assumption: 160nsec shaping, 10MHz sampling
  - **Resistive strips would make charge collection slow, which prefers 160nsec shaping**
- One strip signal = 5 hits (in timing direction) * 10 bits (ADC).
- # of total channel: 256 *3*8 = ~6k
- Per event data rate: 6k * 0.1 (occupancy) * 50 (bits) * 1.4 (overhead factor) = 42k bits/event
- At 100kHz: 4.2Gbits/s → < 0.5% of TPC data volume

Hugo Pereira Da Costa



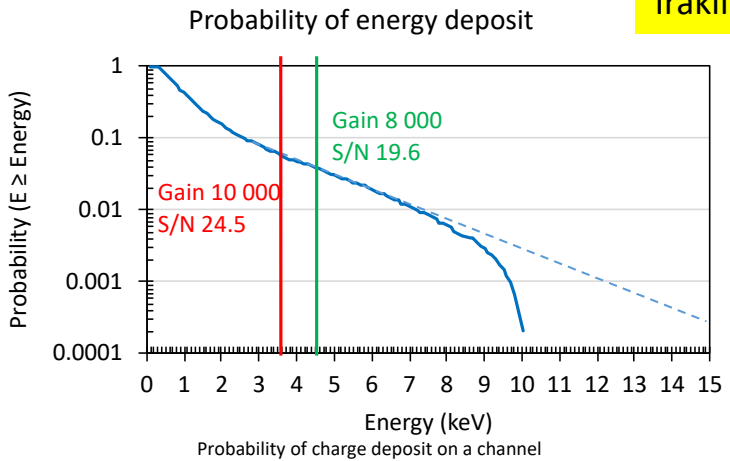
Expected signals

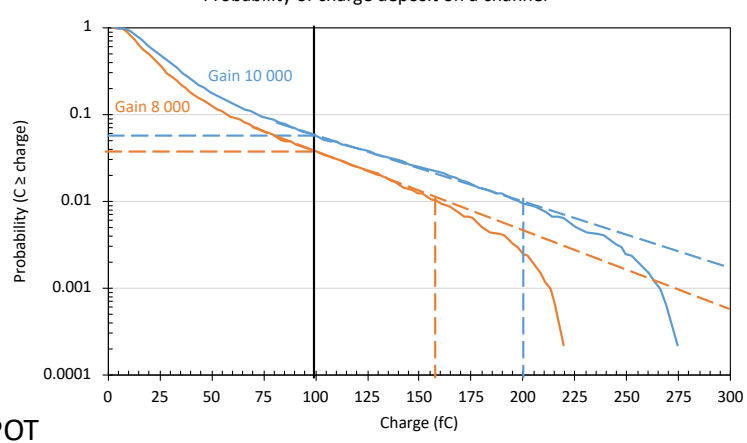
- Mean E_{dep} is 500 eV, mean initial N_e is 18.6C
  - **Charge per hit: 18.6 * 8000 (gain) * 1.6×10^{-19} = 23.8 [fC]**
  - **One hit spreads over a "cluster" of ~5 strips**
  - **Strip with max amplitude gets ~65% of cluster charge**
  - **About 71% of the charge reaches to SAMPA**
  - **→ Highest input signal is 11 [fC]**
    - **Max input: 67 fC@30mV/fC, 100 fC@20mV/fC gain**
  - **Primary gain choice: 20mV/fC**

- Because of a long tail of E_{dep} distribution, SAMPA might be overrun in:
  - **3.7% cases @ 8 000 detector gain**
  - **5.8% cases @ 10 000 detector gain**

- Three saturation scenarios
  - **Signal hitting max of dynamic range of ADC**
  - **Pulse pile-up hits CSA ceiling (30nA) at high rate**
  - **If a strip is shared by multiple clusters, charges are added up, resulting in saturation.**
    - **Last two are negligible, but it needs confirmation**

Irakli





Cost Drivers

- FEE board production (16 FEEs): $7K (zero for now)
  - PCB production ($2k) + partial turnkey assembly ($5k, including RC-parts to be procured by vendor).
  - Enough non-RC parts are already in hands to cover production for TPOT.

- 1 FELIX card + 1 EBDC: $14k (zero for now)
- 1 Mighty-JACK board: $2k (zero for now)
- 1 fiber sort-out-box: $3k (zero for now)

- Signal interface cable: $21k (SAMTEC)
- HV modules and mainframe: $37k (CAEN)
- HV cables (SHV): $2k
- LV power distribution (Only cables): $2k (zero for now)
  - Cable/connector purchase and cable production (harness) at a vendor

- Optical fibers: $2k

- Total net cost at this moment: $62K