INTT Software: tasks for Day1 & Hardware related things

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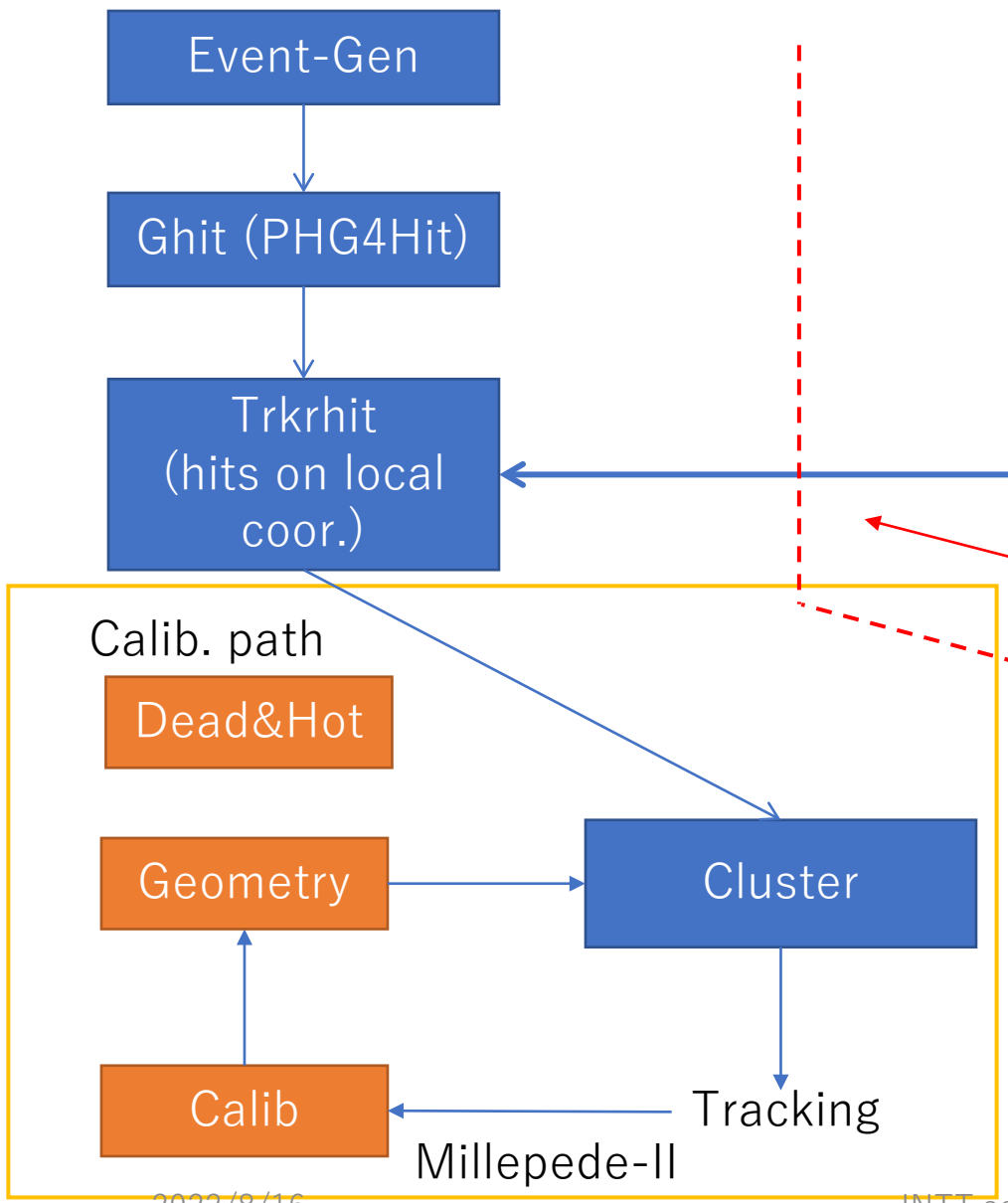
Software tasks

	person	Status
QA with ladders at barrels [Assembly]	Genki, Misaki	Testing ladder with actual Bias/LV system. Using Win7 DAQ
Unpacker	Joseph, Milan, Cheng-Wei, Wei	Need to define INTT rawdata with Raul and Martin's help.
Online monitor	Milan, Joseph, Cheng-Wei, Wei	Plots for monitoring INTT status are listed and started coding
INTT Event Display	Runa	
Expert GUI for sPHENIX	Hikaru	
Standalone DAQ with FELIX	Itaru,	Need Martin and Raul's help
LV/Bias GUI	Wei-che, Maki, Mai, Maya	CUI based control, move to GUI
Temperature monitor	Mai	
Offline code (rawhit and I/F)		
Geometry calibration – millepede	Yumika	Not started yet.s
Cosmic ray data analysis	Yumika	See her talk
Noise study	Yuka	

Data Flow for INTT clustering in real data



- **Basic software needed**
  1. Unpacker (iValue()) for INTT
  2. RawData structure
  3. Address conversion from hardware ch. to reco-software ch.

Status

- Unpacker
  - Need to define INTT rawdata with Raul and Martin's help.
  - A meeting is scheduled on Wed. 4:00pm to discuss about the raw data format and FELIX readout status
- INTT RawData
  - INTT internal module to keep ch-by-ch hit information
  - Not defined yet.
- Address Module
  - Convert hardware ch. To offline software ch.
  - Joseph is working on to compile the information from both hardware side and offline software side

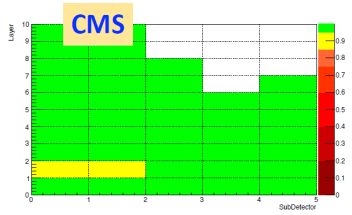
Online monitoring

- Thanks, Milan, Joseph, ChengWei, Wei for gathering information about FVTX and CMS SSD.
  - Monitoring items are listed
    - Hardware status monitoring (hit multiplicity, ADC, FED error, etc)
    - Advanced status monitoring using reco-information (#cluster, #cluster w/ track)

Milan's slide

Summary

CMS



FVTX

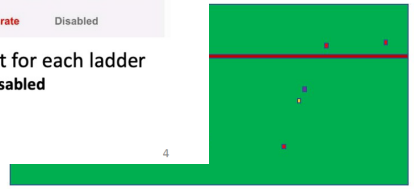
- The fraction of modules which do not pass the Quality Test
- Legend:
  - **green** : status = [95-100]% - GOOD
  - **yellow** : status = [85-95]% - (probably) BAD
  - **red** : status = [0-85]% - BAD
  - **white** : not read out

- Hit multiplicity per event for each ladder
  - **Condition**: **good**, **low**, **disabled**

Milan Stojanovic, INTT Meeting 4

Milan's slide

Chip/Channel monitoring

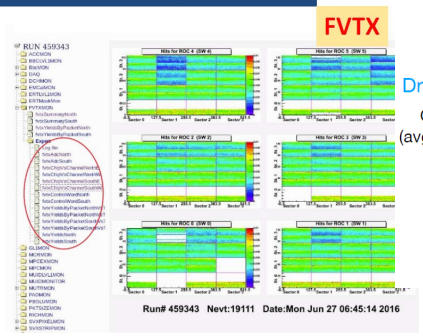


APV

The Subdetector Map, filled with a color code depending on the outcome of Quality Tests.

- **Green** Good
- **White** Missing
- **Dark Red** FED Errors.
- **Pink** Too high (or too low) number of Clusters
- **Orange** Too high (or too low) number of Digis
- **Red** Both high (or low) #Digis and #Clusters
- **Purple** are modules with wrong Volt.

FVTX



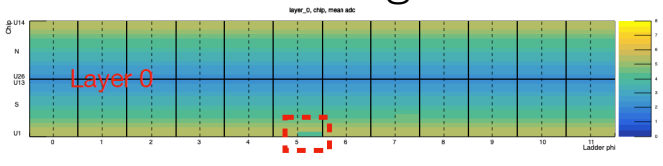
- Hit multiplicity for each channel

Milan Stojanovic, INTT Meeting 5

ChengWei's slide

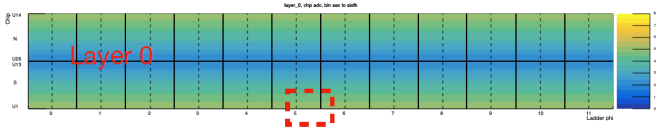
Draw_adc_overall (0)

Overall - adc value
(avg value from stats box)



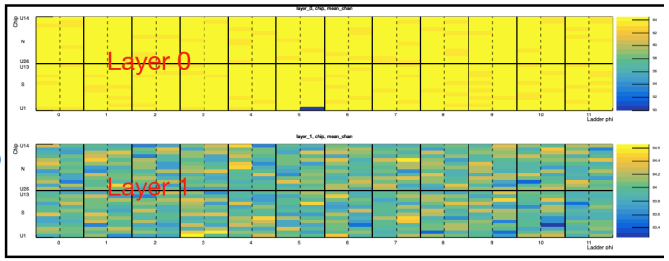
Draw_adc_overall (5)

Overall - adc value
(energy weighted method)
(bin 2nd ~ bin 6th)



Draw_adc_overall (1)

Overall - mean chan
(avg value from stats box)



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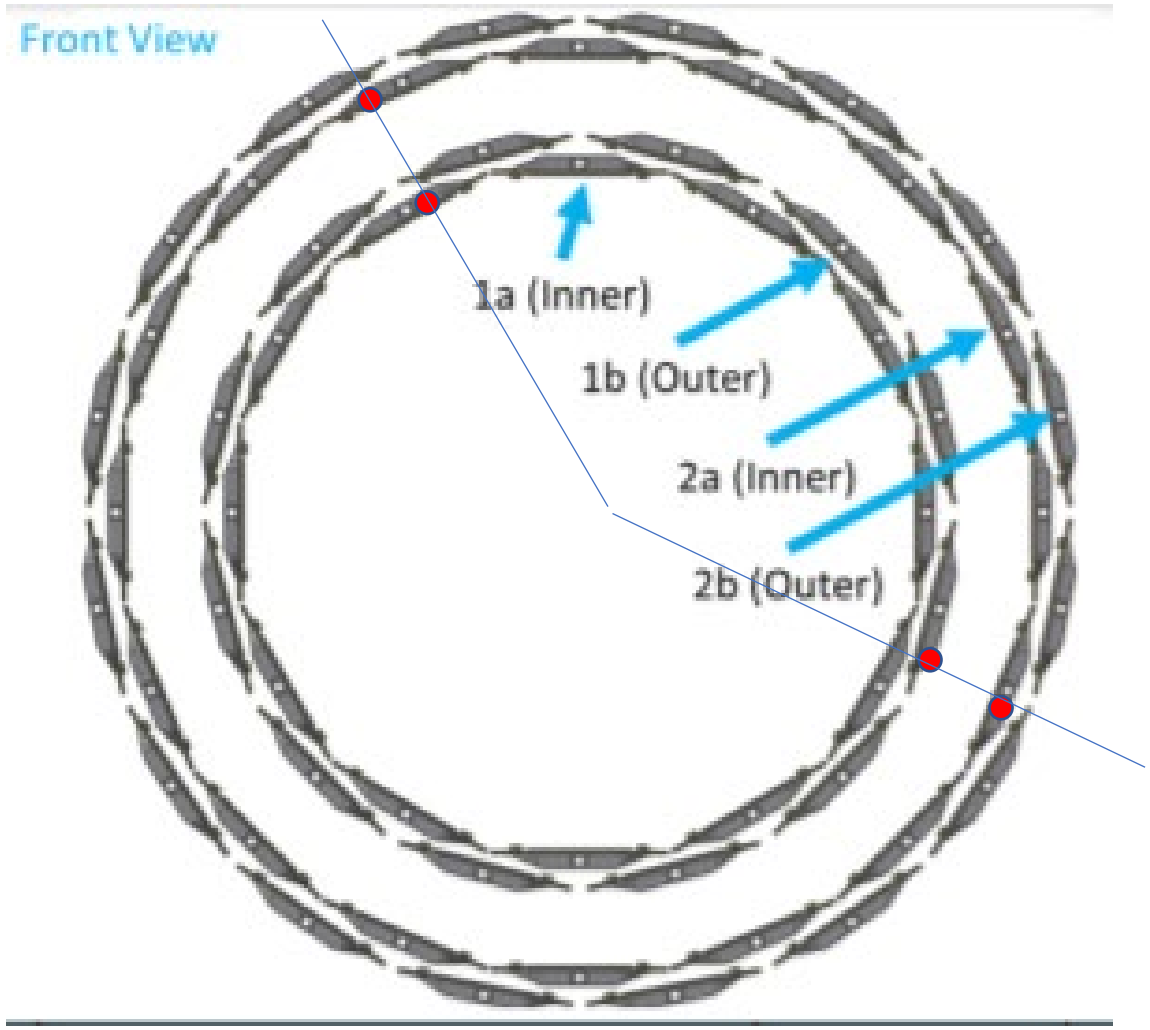
INTT Event Display

- INTT event display is under development to see INTT hits event-by-event basis for QA purpose.

- ED consists of 2 parts
  - Cluster position from offline reco.
  - Display INTT ladders and hits as above.
    - Ladders are displayed via TGeo

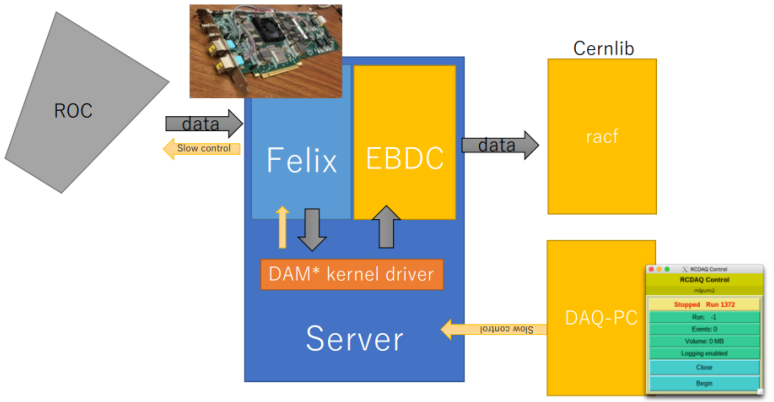
- Now gathering information to access Cluster info in reco code.



INTT DAQ with FELIX

- Standalone DAQ with FELIX
  - FELIX readout
  - Data format is not defined yet
  - Itaru consider a setup of FELIX DAQ at 510 Si-Lab

1008 DAQ Confguration



- LV/Bias control
  - CUI command prepared by Maki, WeiChe
    - Mai just joined to the team
  - GUI development started by Mai, Maya

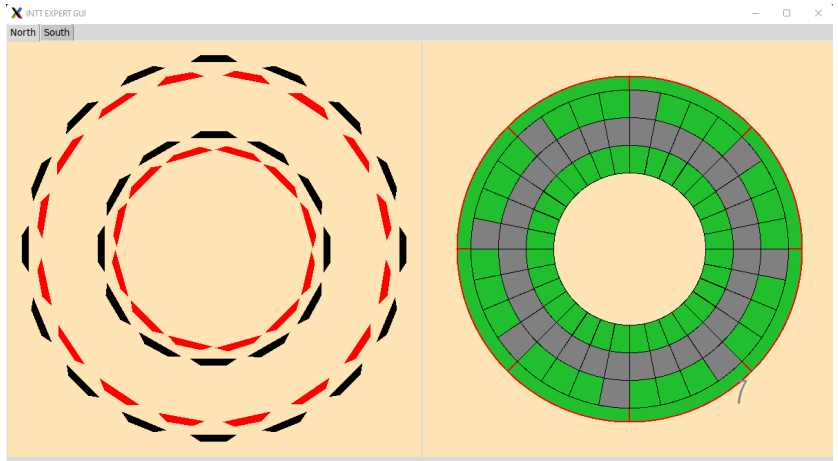
```
maki@DESKTOP-NFJ2CLG:/mnt/c/snmp$ python3 main.py
OK
<COMMANDS>
GetCrate -> Get crate status: on/off
Crateon  -> Turn on crate
```

Perl ~/power/FVTX_Dist_weiche_stable.pl on/off/enable/disable north

These are two parameters need to deliver to script

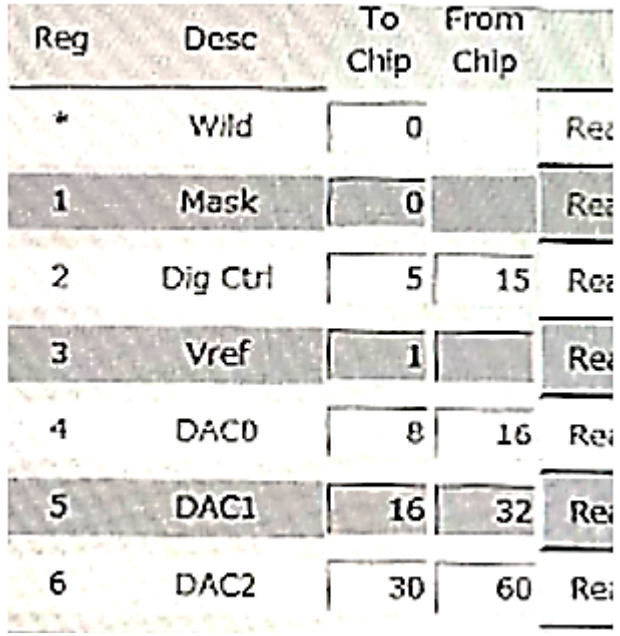
```
intt@inttpower:~$ perl ./power/FVTX_Dist_weiche.pl on north
```

- Expert GUI
  - Hikaru made nice progress on Expert GUI.
    - GUI shows all the register values. These are also saved in DB
    - See his talk
  - Readback from ladder is not successful



Issue on readback from ladders

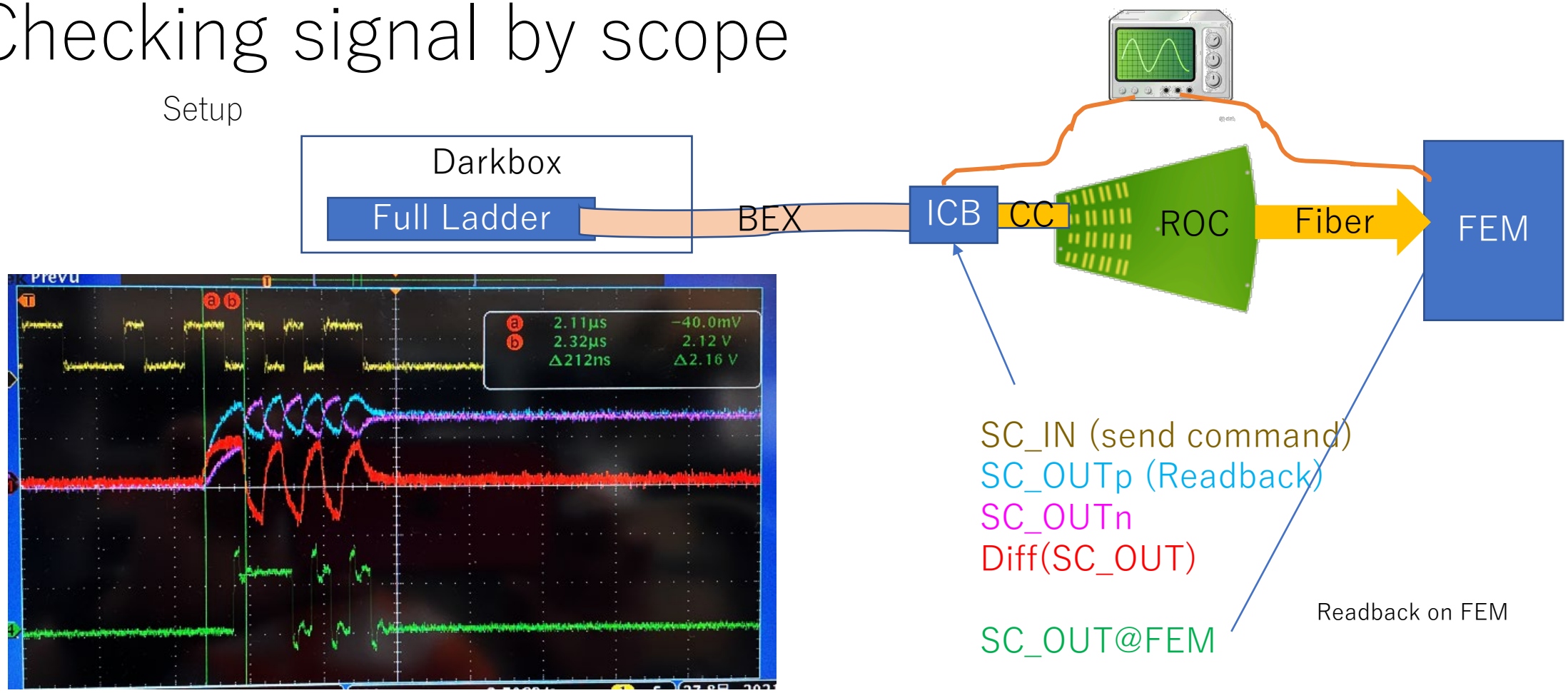
- Readback from ladders with bus-extender is not successful
  - Readback w/o bus extender is successful
- This issue was found some time ago and I investigated what actually happen and why the readback didn't work.
- Actual symptoms
  - Readback data from ladder is 8 bit-word.
  - Readback data w/ BEX show 7bit correctly but missing MSB which comes last.



Reg	Desc	To Chip	From Chip	
*	Wild	0		Rea
1	Mask	0		Rea
2	Dig Ctrl	5	15	Rea
3	Vref	1		Rea
4	DAC0	8	16	Rea
5	DAC1	16	32	Rea
6	DAC2	30	60	Rea

Checking signal by scope

Setup



- SC_IN: 10101011
- SC_OUT: 11010101 (agree w/ SC_IN)
- SC_OUT@FEM : 11101010 (different.1 last bit missing)
- GUI:87 (01010111)

Readback is little endian

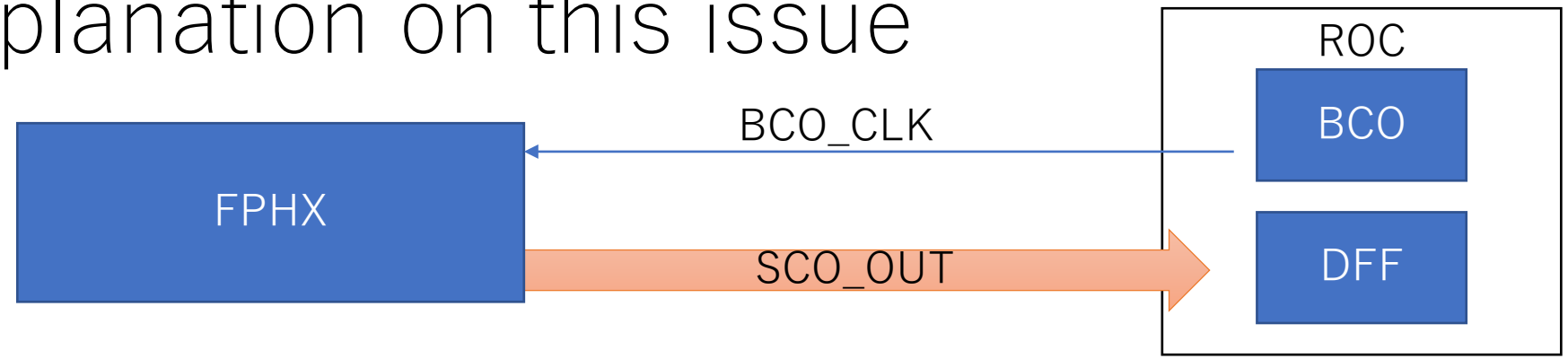
SC_IN＝SC_OUT at ICB
1 bit missing at FEM
→ The problem can happen at ROC

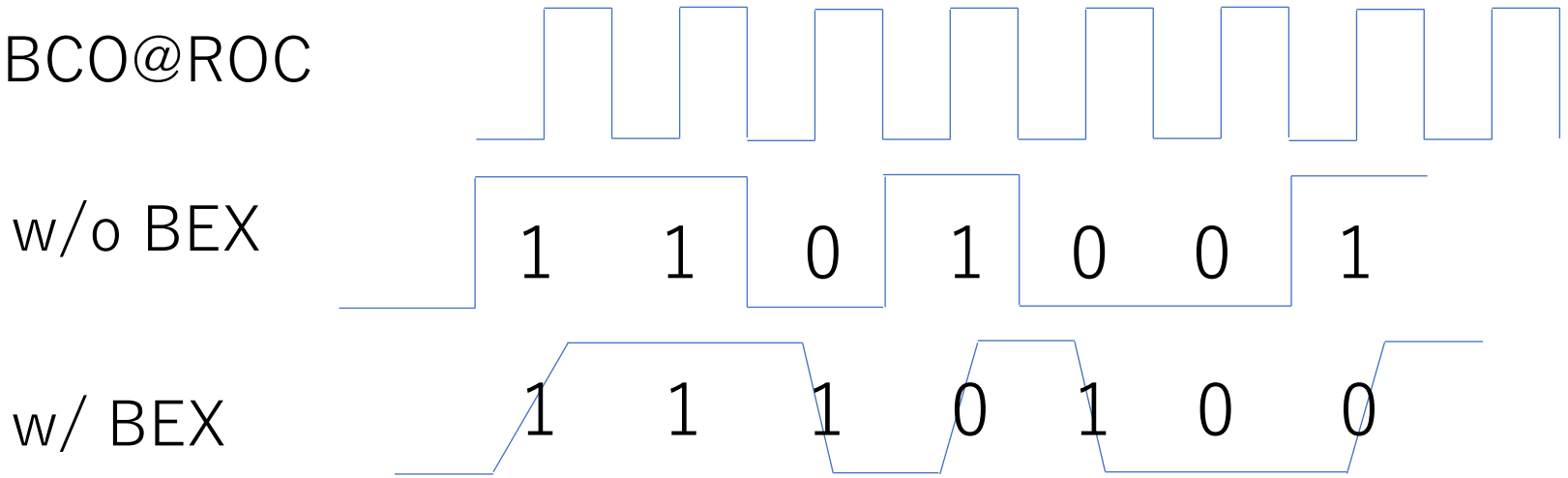
Summary of the readback data

GUI INPUT	SC_OUT(ICB)	SC_OUT(FEM)	GUI ReadBack
171 (10101011)	11010101	11101010 (87)	87 (01010111)
170 (10101010)	01010101	00101010 (84)	84 (01010100)
172 (10101100)	00110101	00011010 (88)	0
173 (10101101)	10110101	11011010 (91)	91
174 (10101110)	01110101	00111010 (92)	92
138 (10001000)	01010001	00101000 (20)	20 (00010100)
122 (01111010)	01011110	00101111 (244)	244 (11110100)
20 (00010100)	00101000	00010100 (40)	40 (00101000)
40 (00101000)	00010100	00001010 (80)	80
25 (00011001)	10011000	11001100 (51)	51
30 (00011110)	01111000	00111100 (60)	60
35 (00100011)	11000100	11100010 (71)	71

All the data shows INPUT=Readback at ICB but different at FEM w/. 1 bit shift.

A possible explanation on this issue





- With bus-extender, the data timing is delayed ~20ns. The delay can cause the 1 bit shift issue.

Proposal of updating SC FPGA on ROC

Readback module (Status_serial_output)

```
    elsif falling_edge(BCO_CLK) then

--Create an FPHX send_command trigger, and upon this trigger start a counter which will
--tell us when to extract the status word from the FPHX SC line:
SEND_COMMAND_BUF <= SEND_COMMAND;
          SEND_COMMAND_2BUF <= SEND_COMMAND_BUF;
          SEND_COMMAND_TRIG <= SEND_COMMAND_BUF and (not SEND_COMMAND_2BUF);

          if SEND_COMMAND_TRIG = '1'  then
                CE <= '1';
          end if;

--After 24 clocks, read the 8-bit FPHX status word:
          if ADDR = "010010" then
                READ_DATA_FPHX <= '1';
          end if;
          if ADDR = "011010" then
                READ_DATA_FPHX <= '0';
                CE <= '0';
          end if;

          if (READ_DATA_FPHX = '1')  then
             STATUS_DATA <= SC_FROM_FPHX_int;
             CS_DATA <= '1';
          else
             STATUS_DATA <= '0';
             CS_DATA <= '0';
end if;
```

After sending the command, the readback data is received with a fixed delay (24-32 clocks, 8bits)

A Possible solution：

- Delay 1 clock
  - Simple but not good for w/ BEX
- take 9 bit data instead of 8 bits.
  - First 8bits are good for BEX,
  - Last 8bits are good for BEX

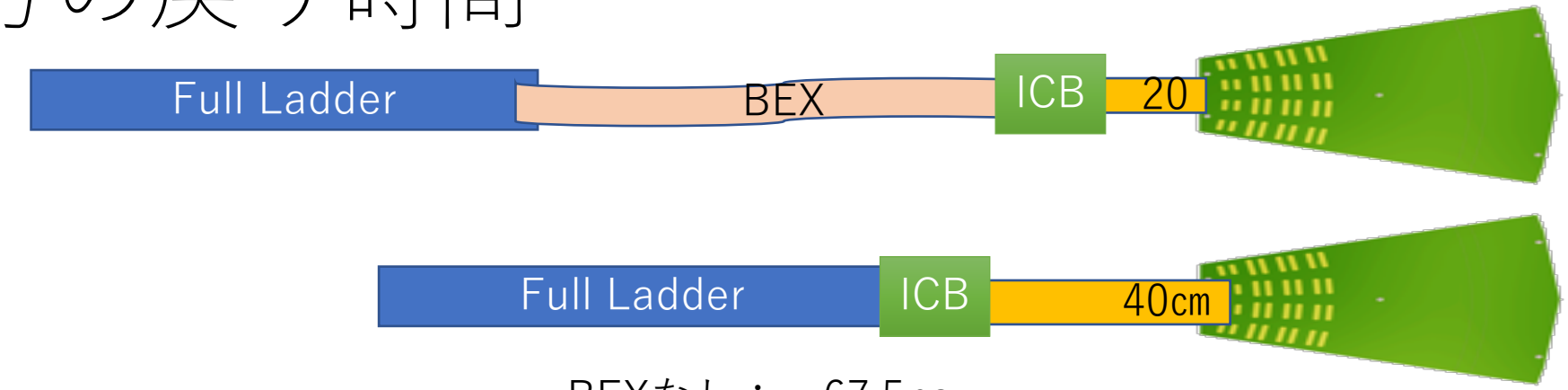
- I would like to test this solution using a ROC for play

Summary

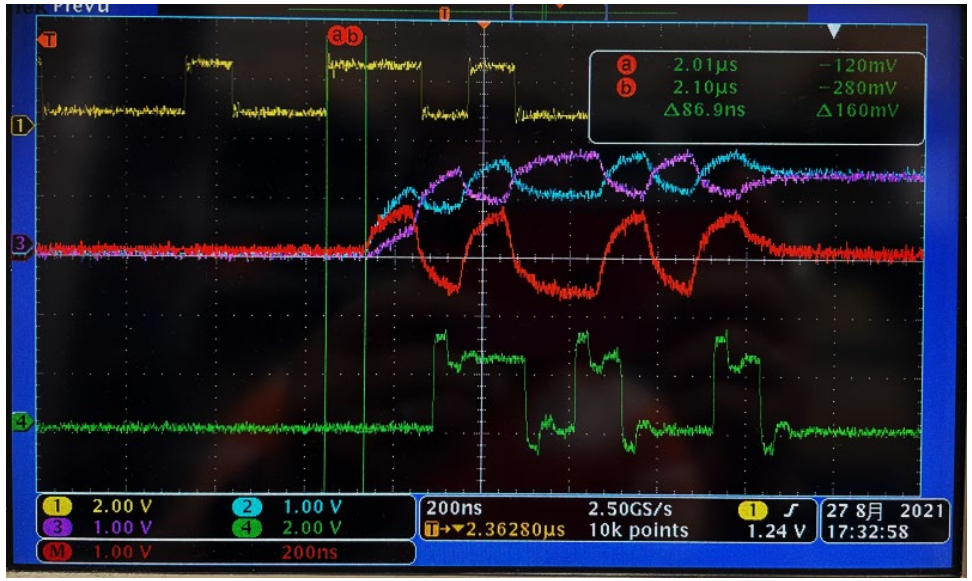
- Software development is on going
  - Online monitoring, LV/HV monitor, Expert GUI are in good shape
  - Other projects just started.

- Readback issue
  - 1 bit missing
  - I plan to play with a ROC

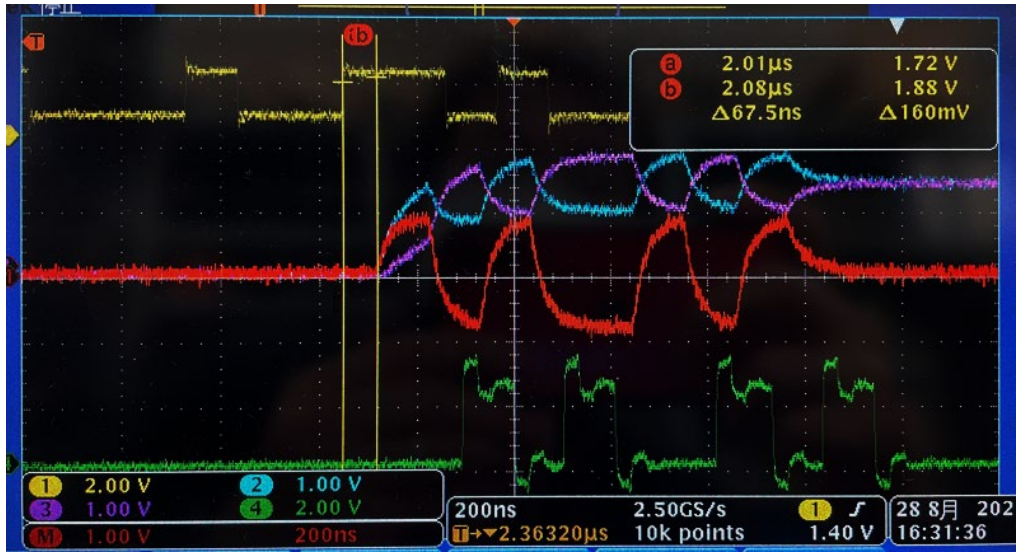
Readback信号の戻り時間



BEXあり：　86.9ns

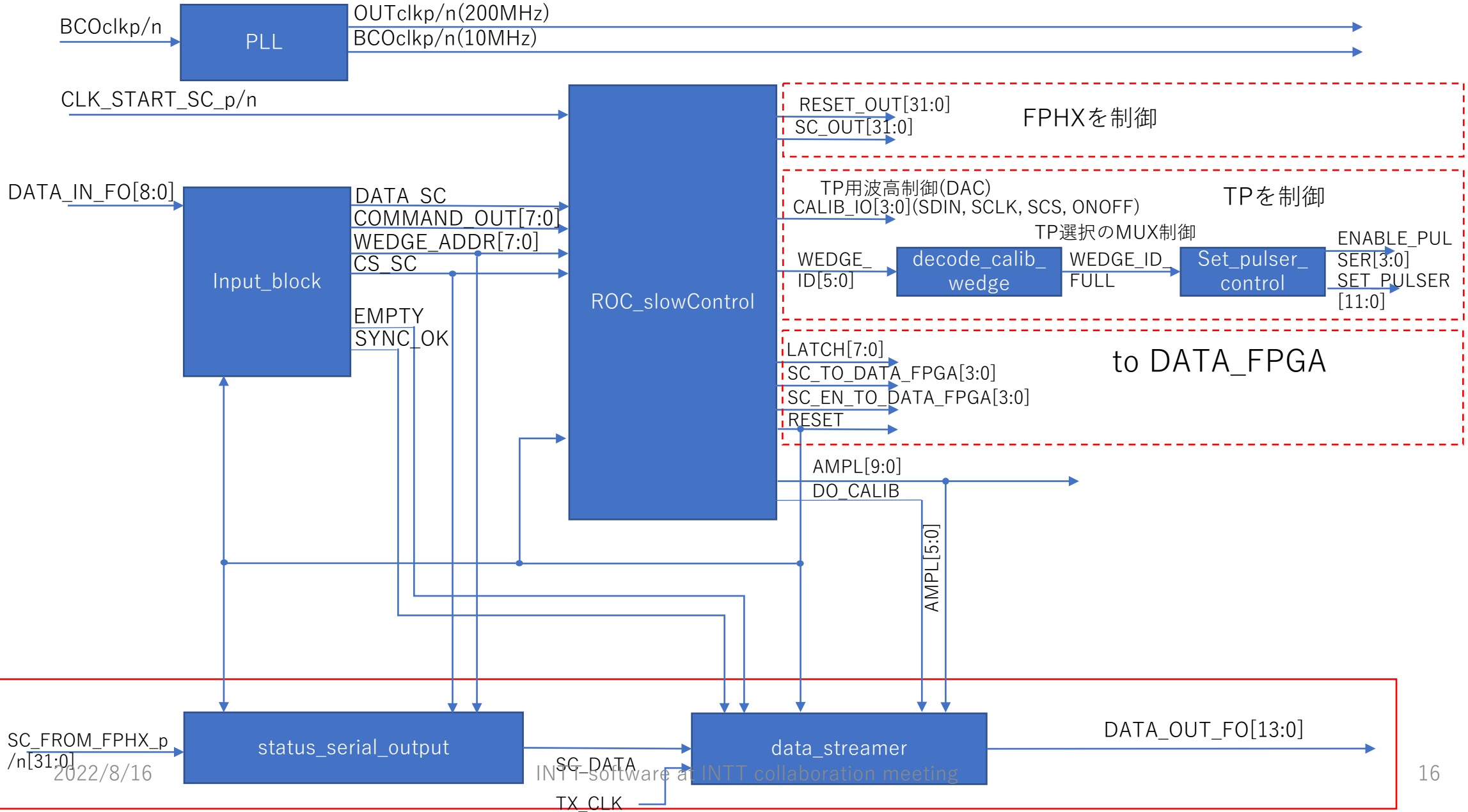


BEXなし：　67.5ns

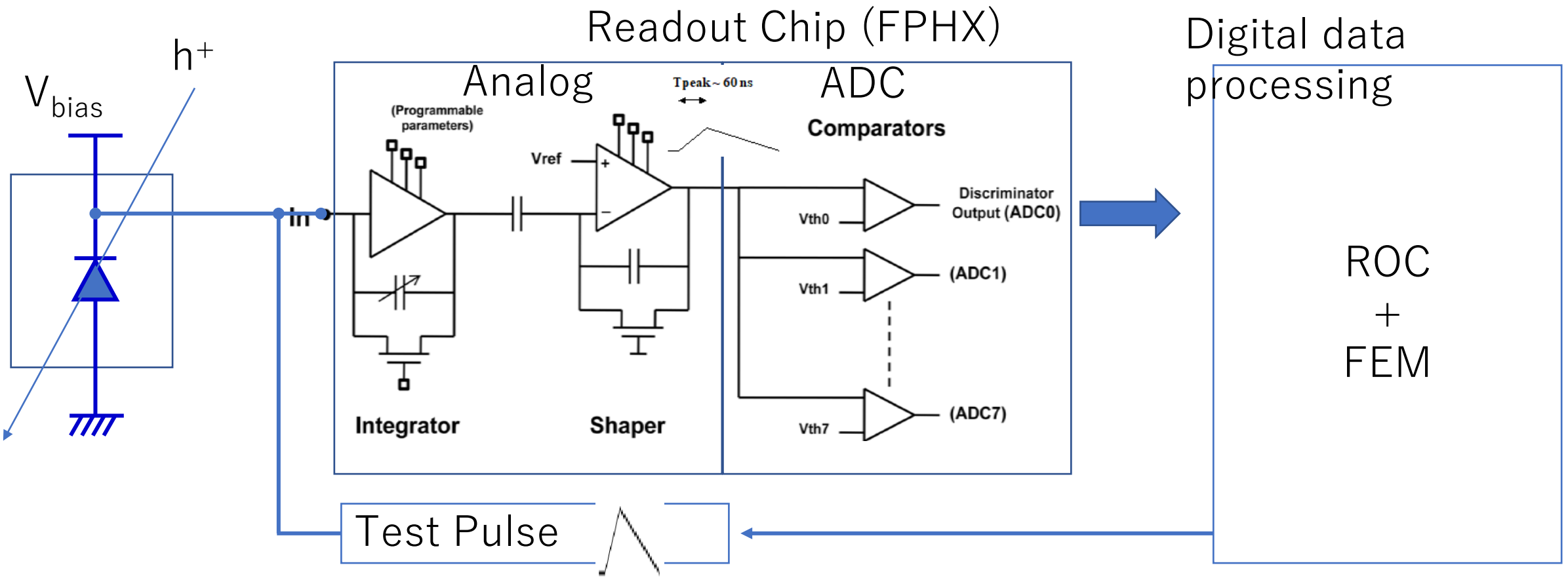


- 時間差：　86.9 – 67.5 = 19.4ns @ 130cm BEX
  - 130cm の往復でかかる時間：　13ns (20cm/1nsで換算)
  - BCOの鈍りで遅れていることも考えられる。

ROC_Slow_control_top

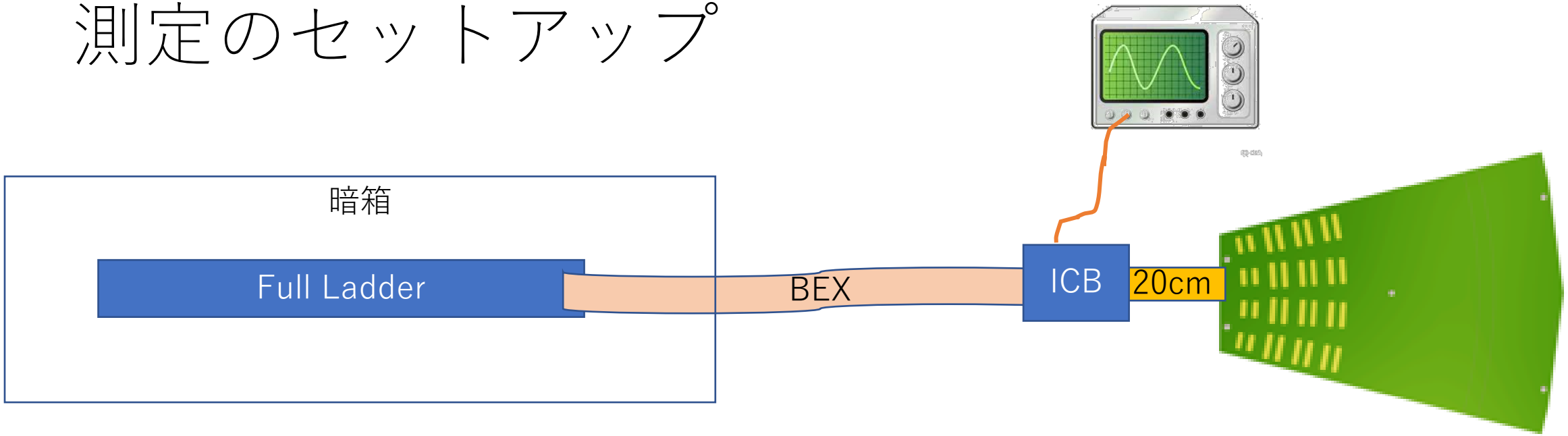


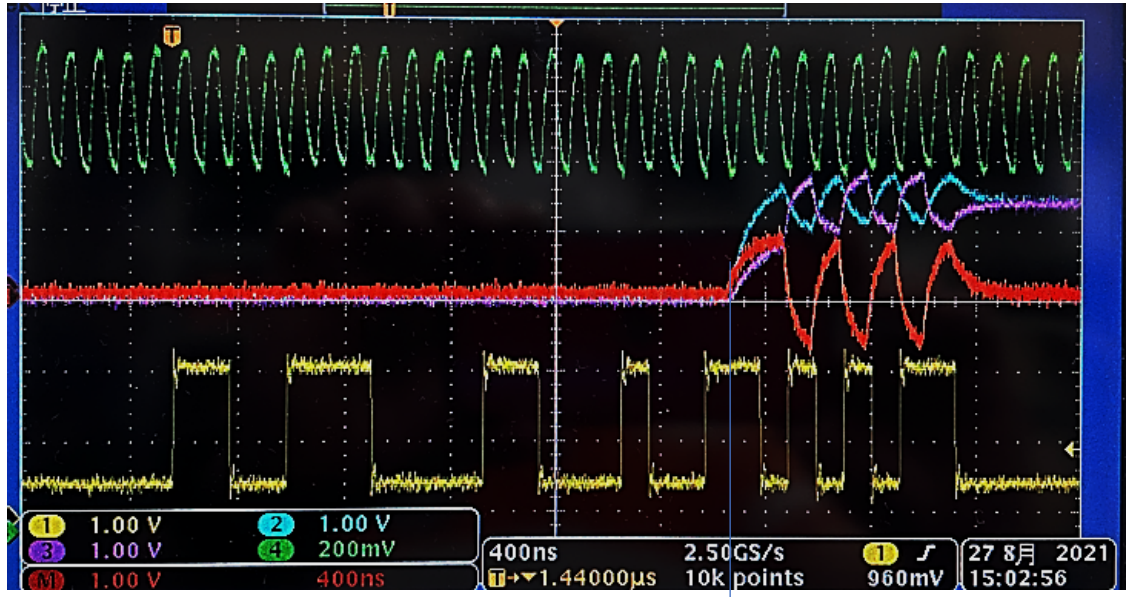
Sensor + Readout Schematics



- Performance is studied using:
  - Charged particle by beam test, cosmic ray and RI sources
  - Test pulse for Readout electronics

測定のセットアップ



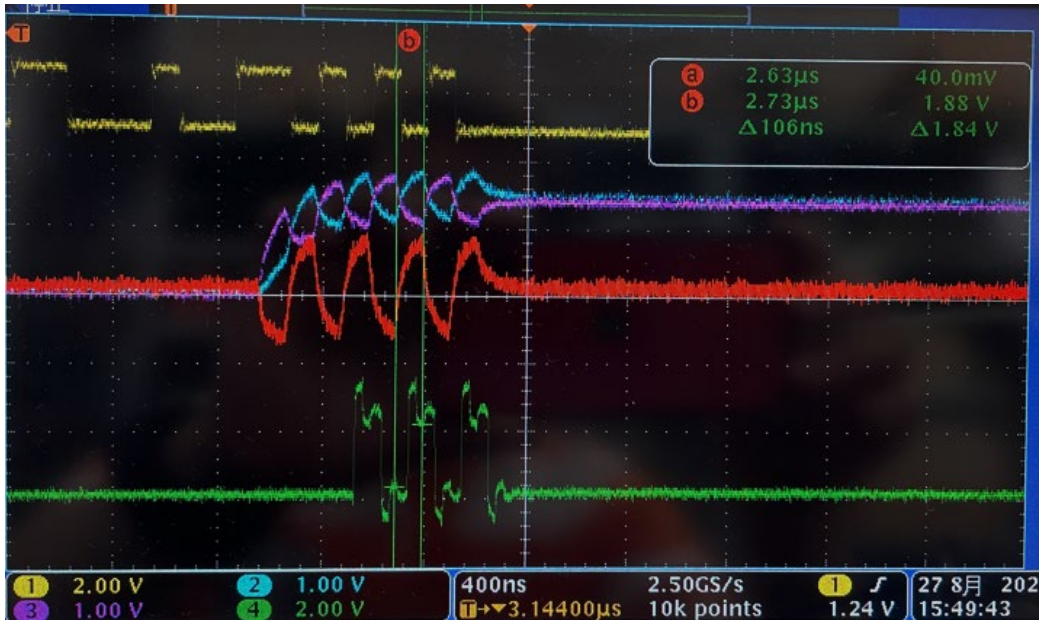


BCO(10MHz)
SC_OUTp
SC_OUTn
Diff(SC_OUT)

SC_IN

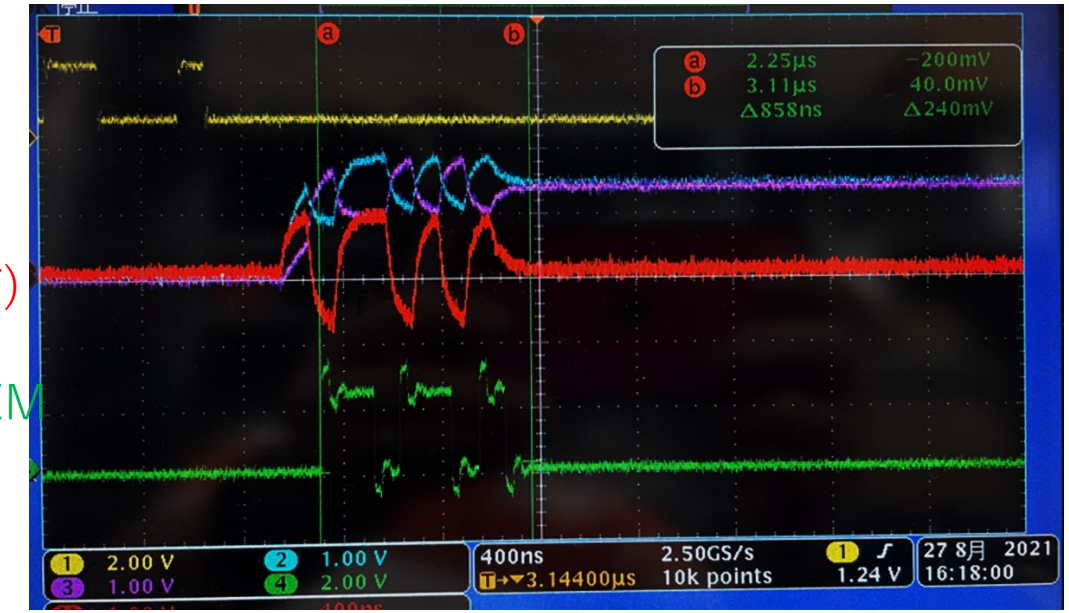
- 入力：10101011
- 出力：11010101
  - 反転してでてくる。
- 入力と出力が一致している。

読み出しデータ



SC_IN
SC_OUTp
SC_OUTn
Diff(SC_OUT)

SC_OUT@FEM



- SC_IN: 10101010
- SC_OUT: 01010101 (SC_INに一致)
- SC_OUT@FEM : 00101010
  - (違う。1ビットずれ＋最初のビットが違う)
- GUI:84 (00101010)

- SC_IN: 173
- SC_OUT: 10110101 (SC_INに一致)
- SC_OUT@FEM : 11011010
  - (違う。1ビットずれ＋最初のビットが違う)
- GUI:91 (00101010)

読み出しデータの1ビット目は、2ビット目といつも同じ

ありえる原因

- ROC上で、FPHXデータの受信失敗
  - (距離が長い？ため、)データが遅れ、受信タイミングがずれてしまう
    - 典型的には1クロックおくれる
  - 観測結果からこれが推測される
    - バスエクステンダを使ったときに起きる。
      - より下流(FEMなど）が原因とは考えにくい。
    - Readback波形の遅れ＋なまりが原因と推測