ROC Test Status

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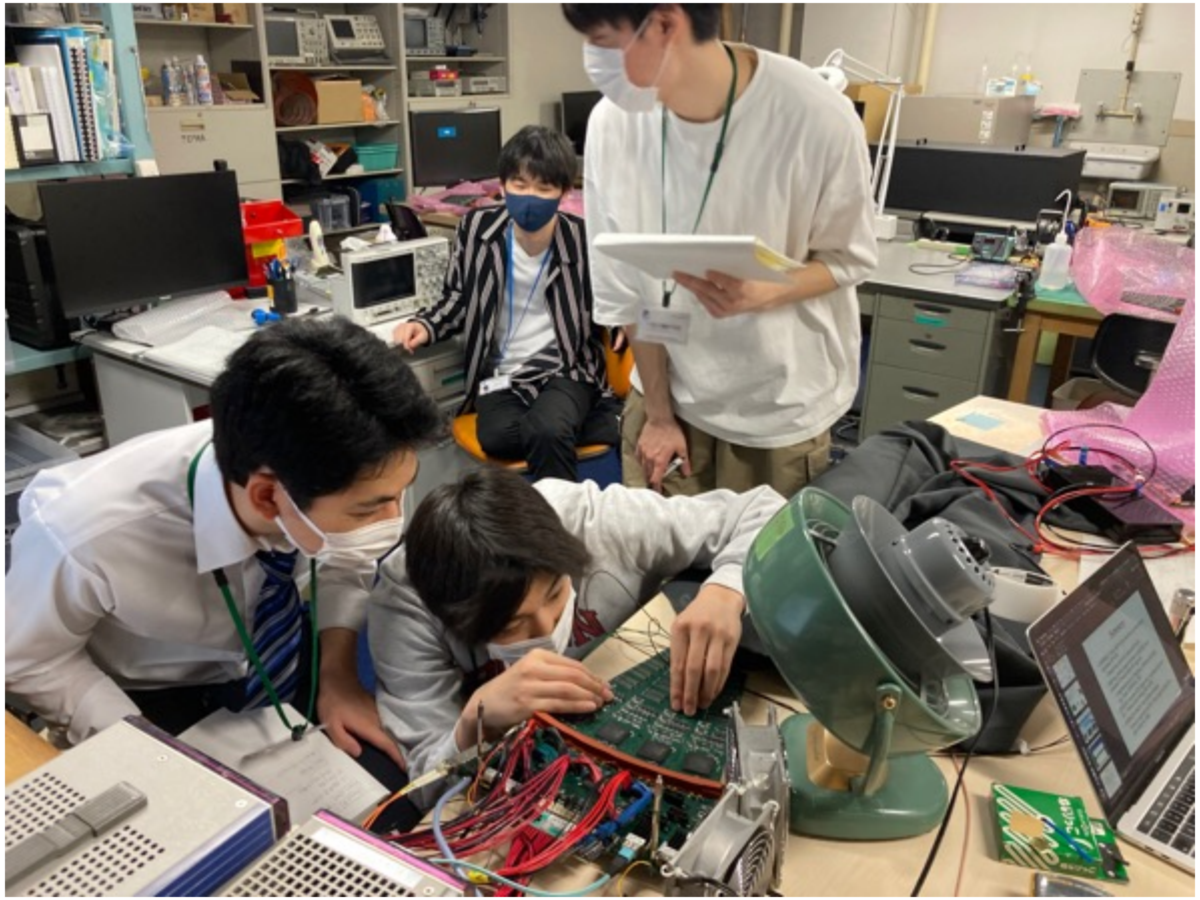
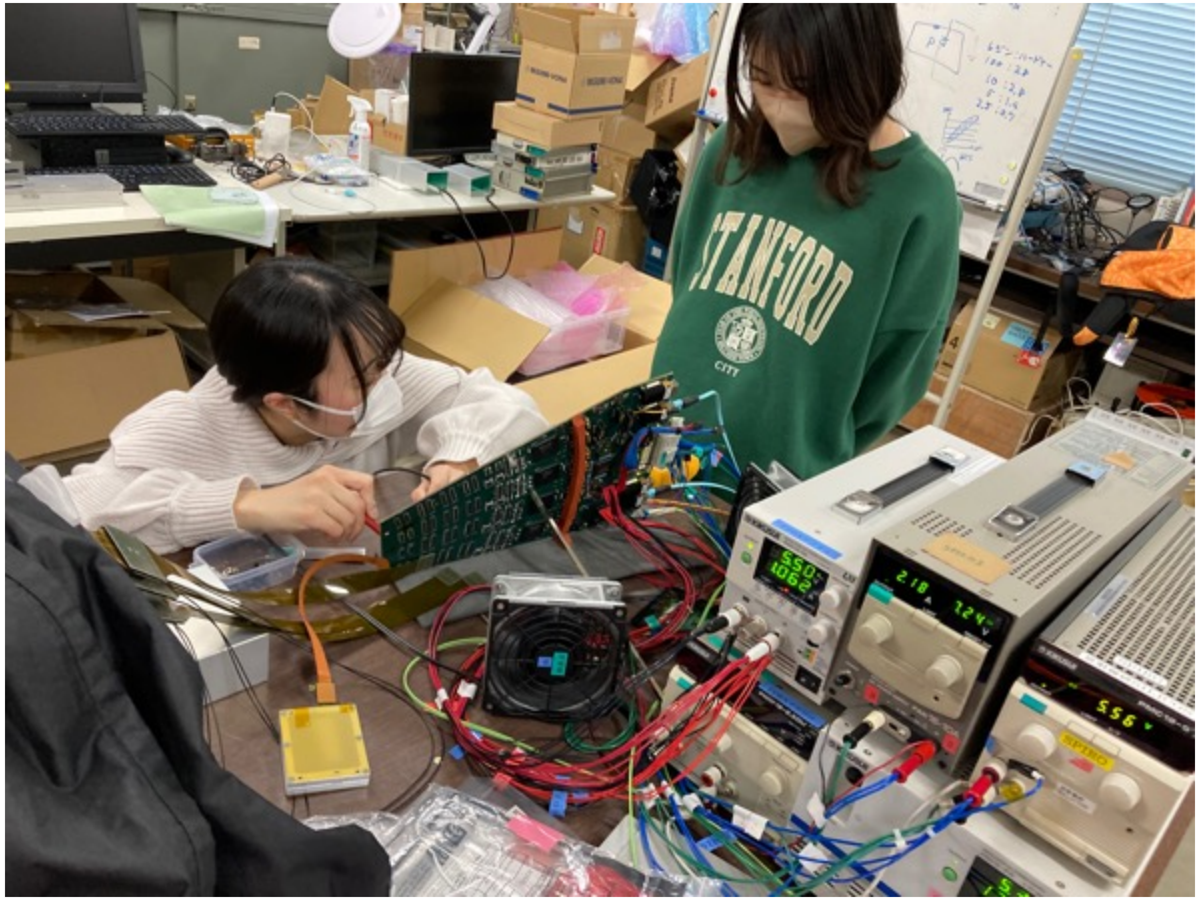
Itaru Nakagawa
On behalf of ROC Test Team




STANFORD

ROC QA Class Definition

Class	Criteria
1	FPHX regulator response as expected. Confirmed healthy calibration data 3 times for all ports.
2	FPHX regulator response as expected. Confirmed healthy calibration data 3 times for all ports, but occasional failure in data taking.
3	FPHX regulator response as expected. There is at least one always unsuccessful calibration data taking port.
	Untested or before regulator upgrade

1008 ROC Test Status at a Glance

Index	ROC #	FVTX	Regulator Upgrade	Location	Class	A1	A2	A3	B1	B2	B3	C1	C2	C3	D1	D2	D3	Issue	Status
1	6	NW2	✓	BNL	1														
2	13	NE4	✓	BNL	1														
3	18	NE1	✓	BNL	1														
4	26	SE3	✓	BNL	1														
5	28	SE0	✓	BNL	1														
6	29	-	✓	BNL	1														
7	20	SW5	✓	BNL	1														
8	22	SE2	✓	BNL	1														
9	23	SE1	✓	BNL	1														
10	31	NW1	✓	BNL	1														
11	32	NE2	✓	BNL	1														
12	19	NE5	✓	BNL	3										F			Fiber Sync	Debug w/ John K.
13	9	-	✓	RKN	2			F										Fiber Sync	Waiting for NE5 debug
14	15	NE0	✓	RKN	2	F									F			Fiber Sync	Waiting for NE5 debug
15	17	NW3	✓	RKN	2			F							F			Fiber Sync	Waiting for NE5 debug
16	24	SE4	✓	RKN	2			F							F			Fiber Sync	Waiting for NE5 debug
17	16	NE3	✓	RKN	3				C	C	C							Calib Pulse	Waiting for SC-FPGA downlaod
18	2	NW4	✓	RKN	3														
19	17	NW3	✓	RKN	3													LV Issue	LV cable might have damaged
20	21	-	✓	RKN	3													LV Issue	LV cable might have damaged
21	10	-	✓	RKN	3													LV Issue	LV cable might have damaged
22	7	-	✓	RKN	3													Fiber Sync	
23	3	NW5		RKN		F		D				F							
24	27	SE5		RKN															
25	14	NE1		RKN							C	C	C		P	P	P	Calib Pulse	

- Good
- Good, but occasional failure
- No data at all

C : Problem in calibration pulse
F : Problem in data fiber sync
P : Problem in power supply
R : Recovered

Statistics

Class	Quantity
1	12
2	3
3	7
	3

Total 25 ROCs

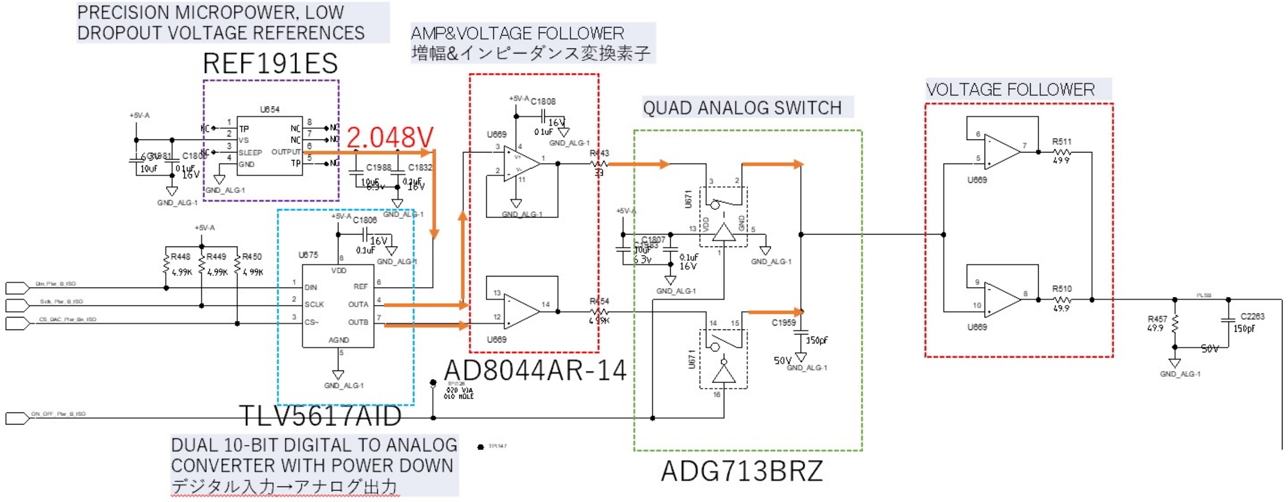
Err or	ROC	Port
C	2	6
F	6	12
P	4	21
	2	15

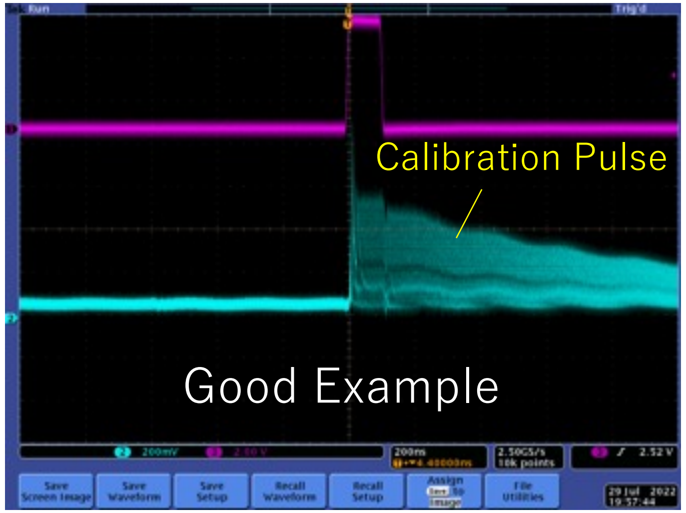
Total 15 ROC

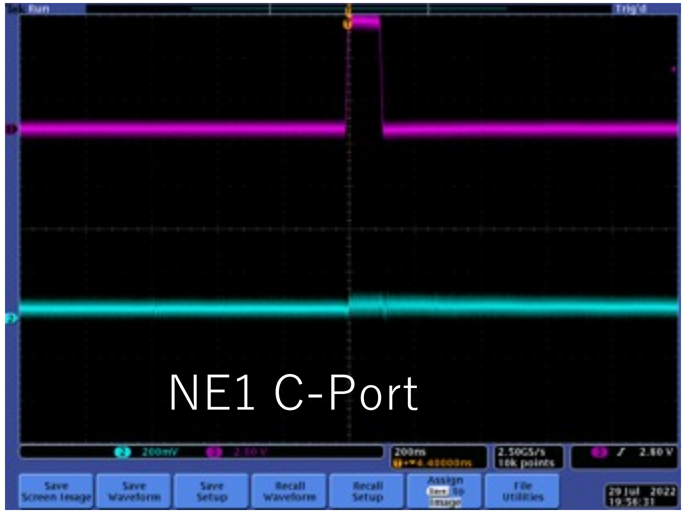
Class	Recovered
ROC	4
Port	10

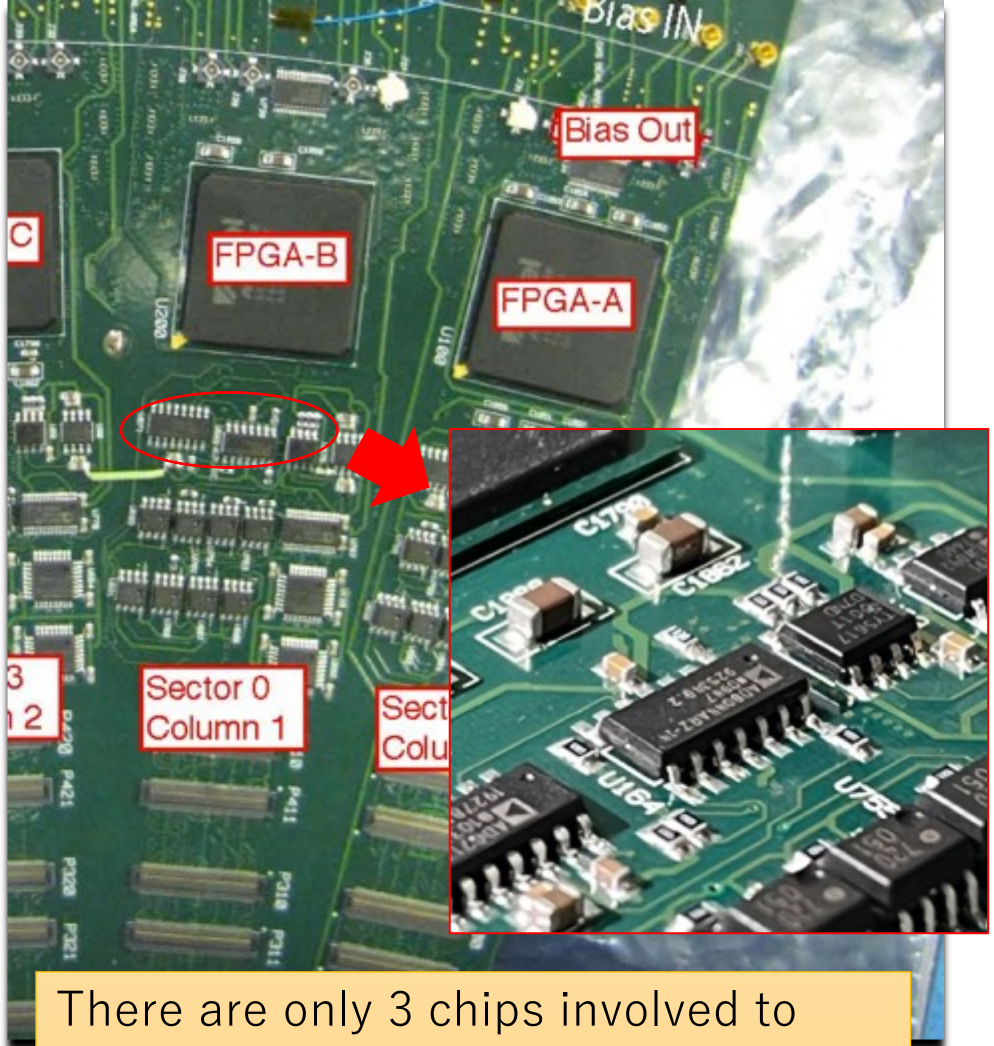
Calibration Pulse Issue

Calibration Pulse Generator Circuit







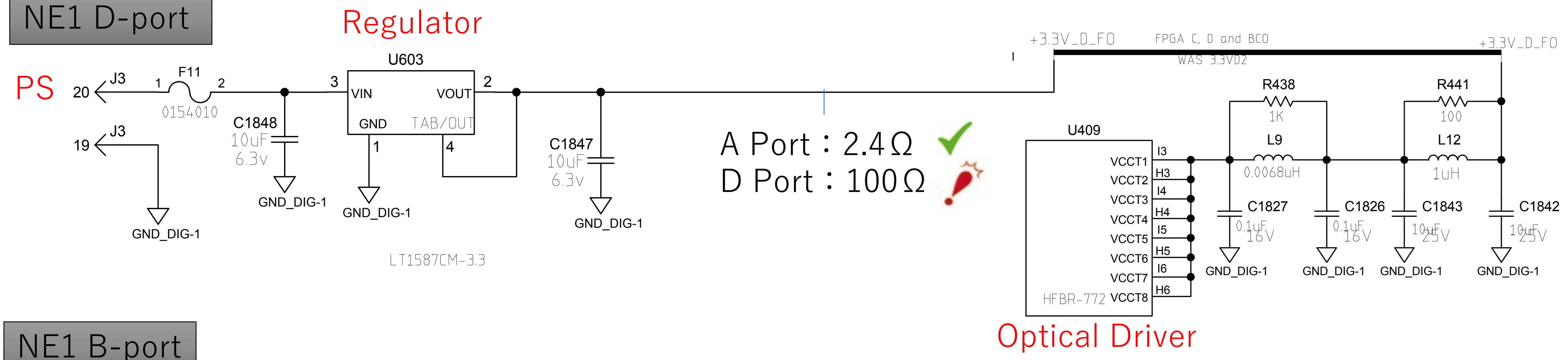


There are only 3 chips involved to generate calibration pulse. So far, we are always able to identify the unfunctioning chip. They are repairable unless signal comes from slow control FPGA is not collapsed.

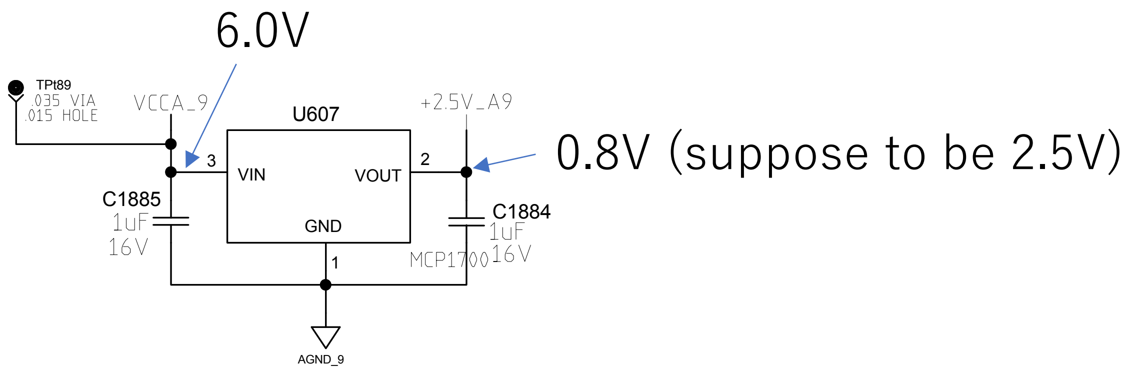
Power Supply Issue

Problem in regulator input/output or extra resistance in power supply line.

NE1 D-port

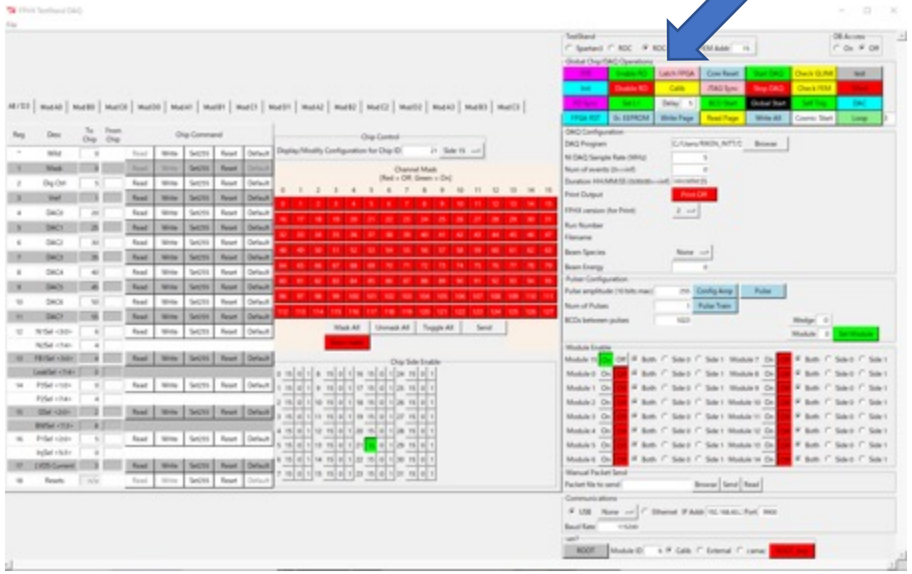


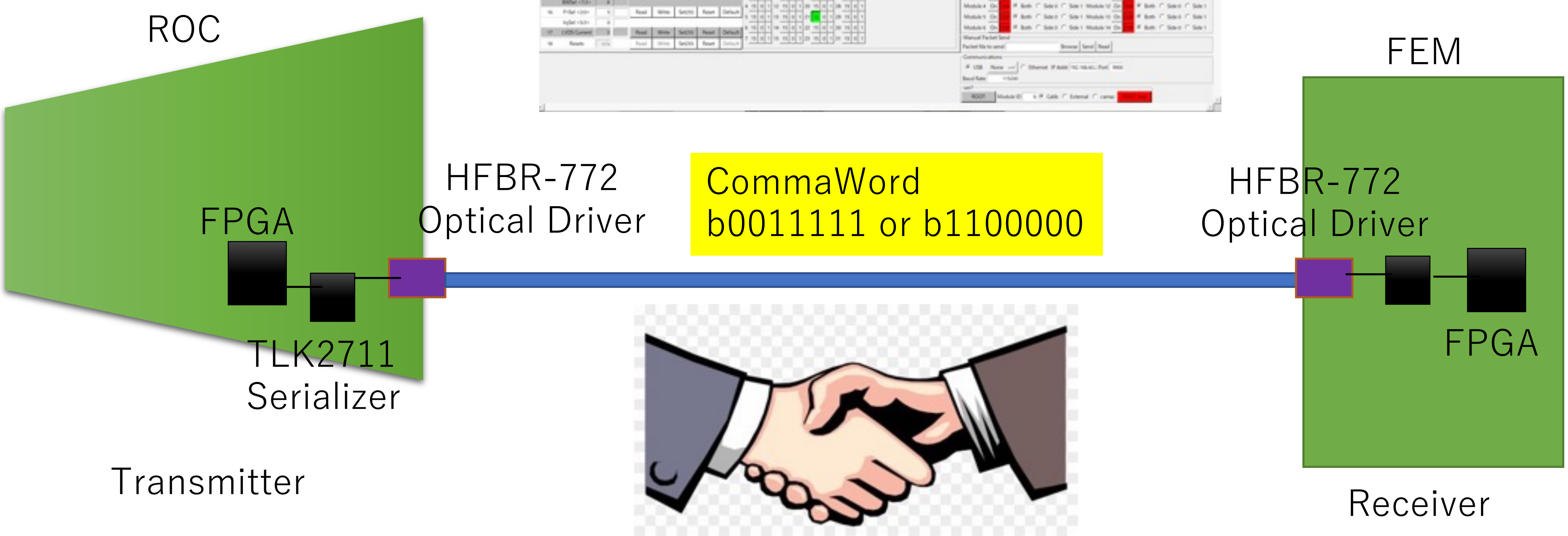
NE1 B-port



Most likely, the cause of the power problem can be identified and good chance to be repaired.

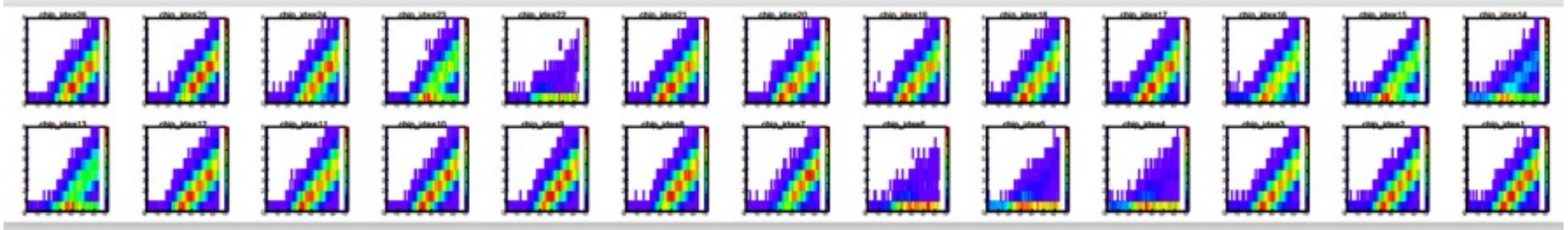
Fiber Synchronization Error

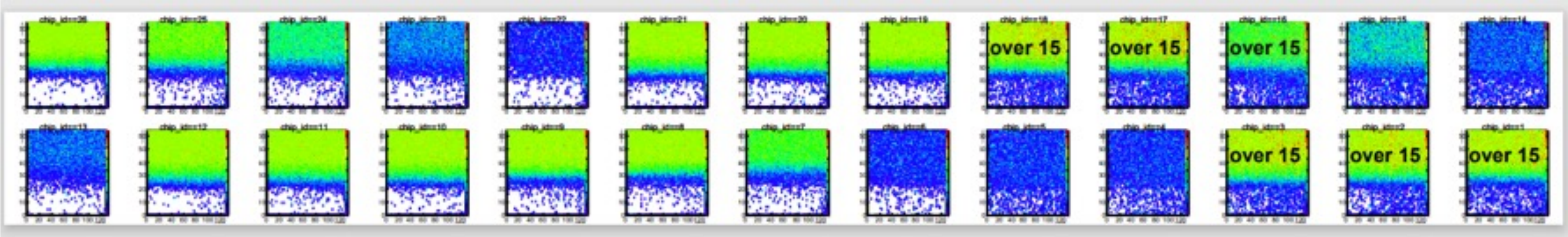




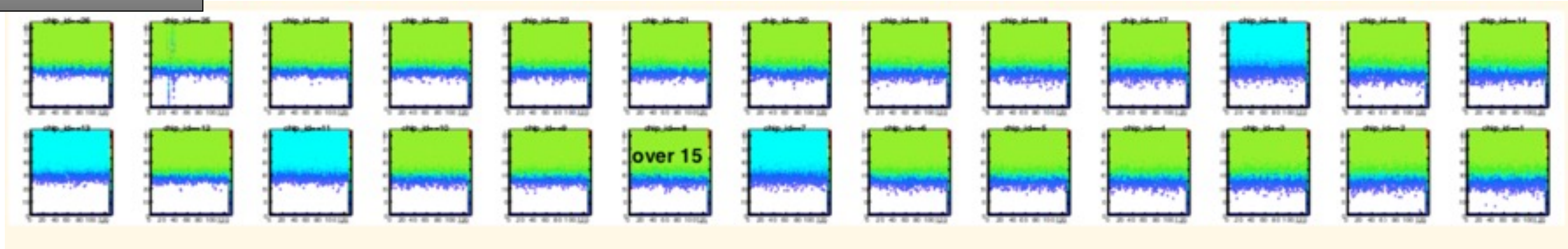
Unclassified Symptoms

NW3 C3-port





NW4 B2-port



Difficulty to pin down the cause. Not yet developed firm way to debug.

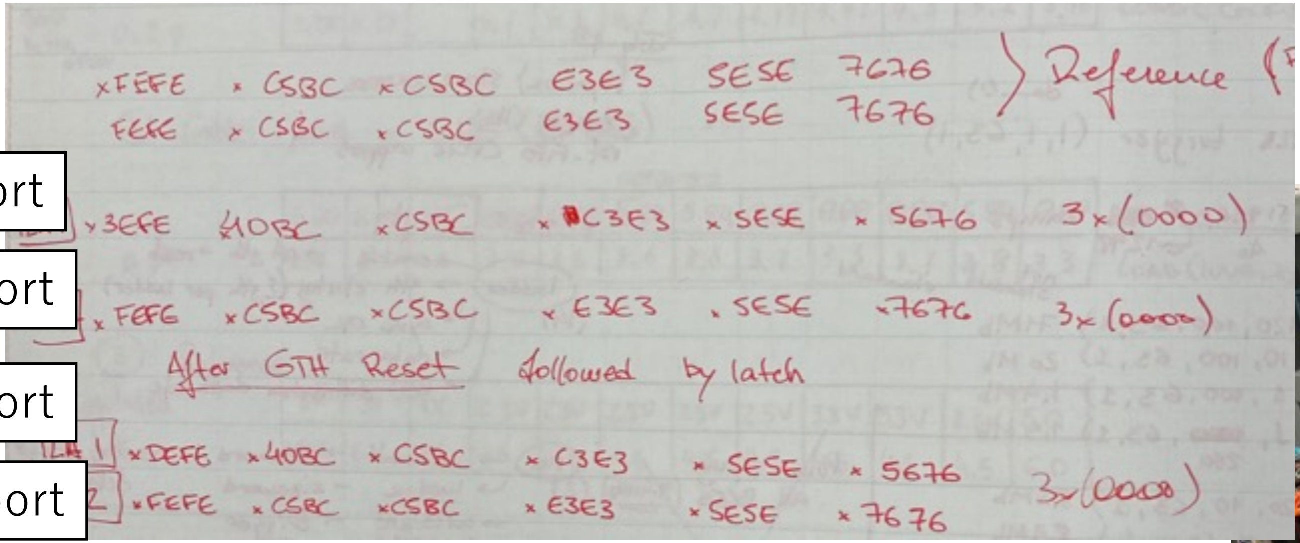
Fiber Sync Error Debugging with John K.

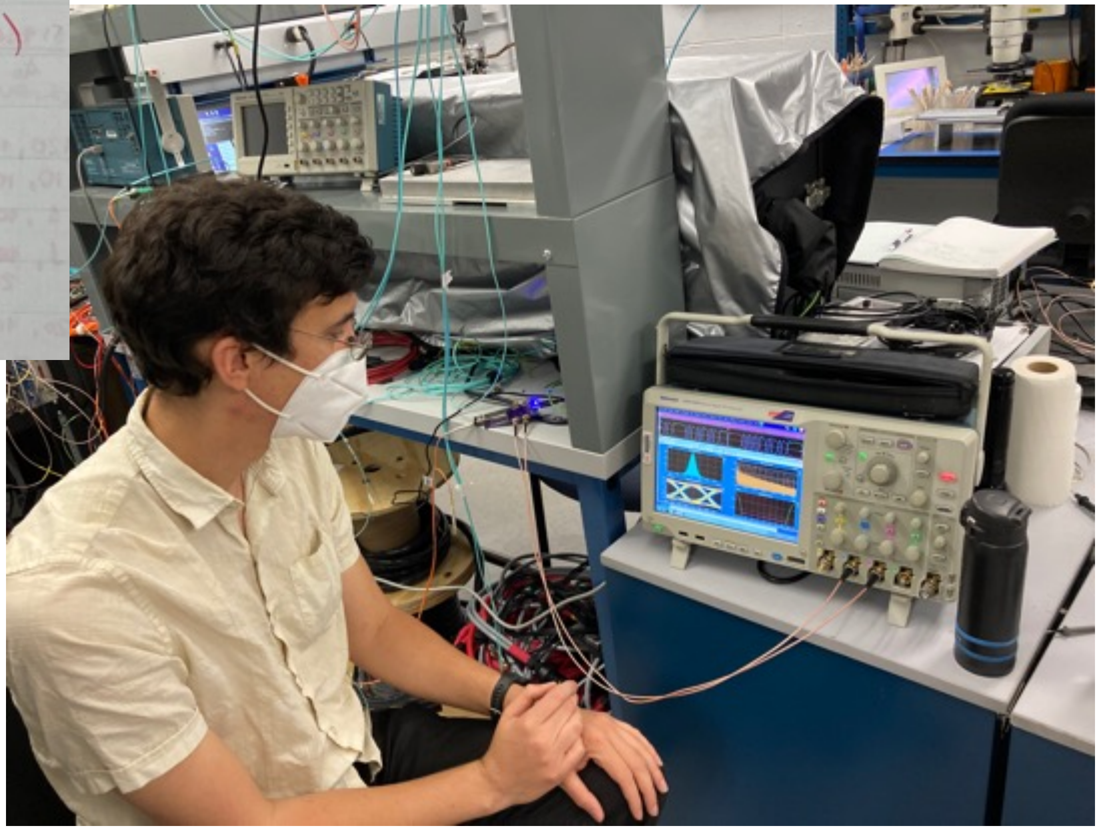
Bad port

good port

Bad port

good port

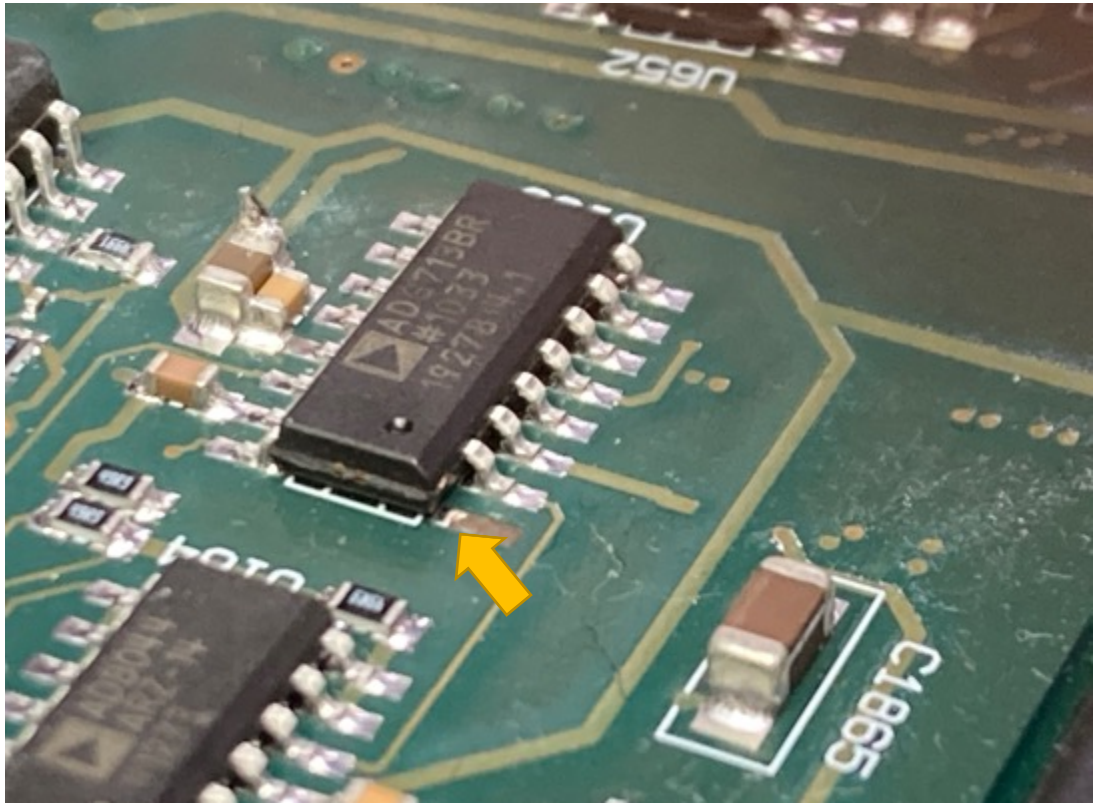




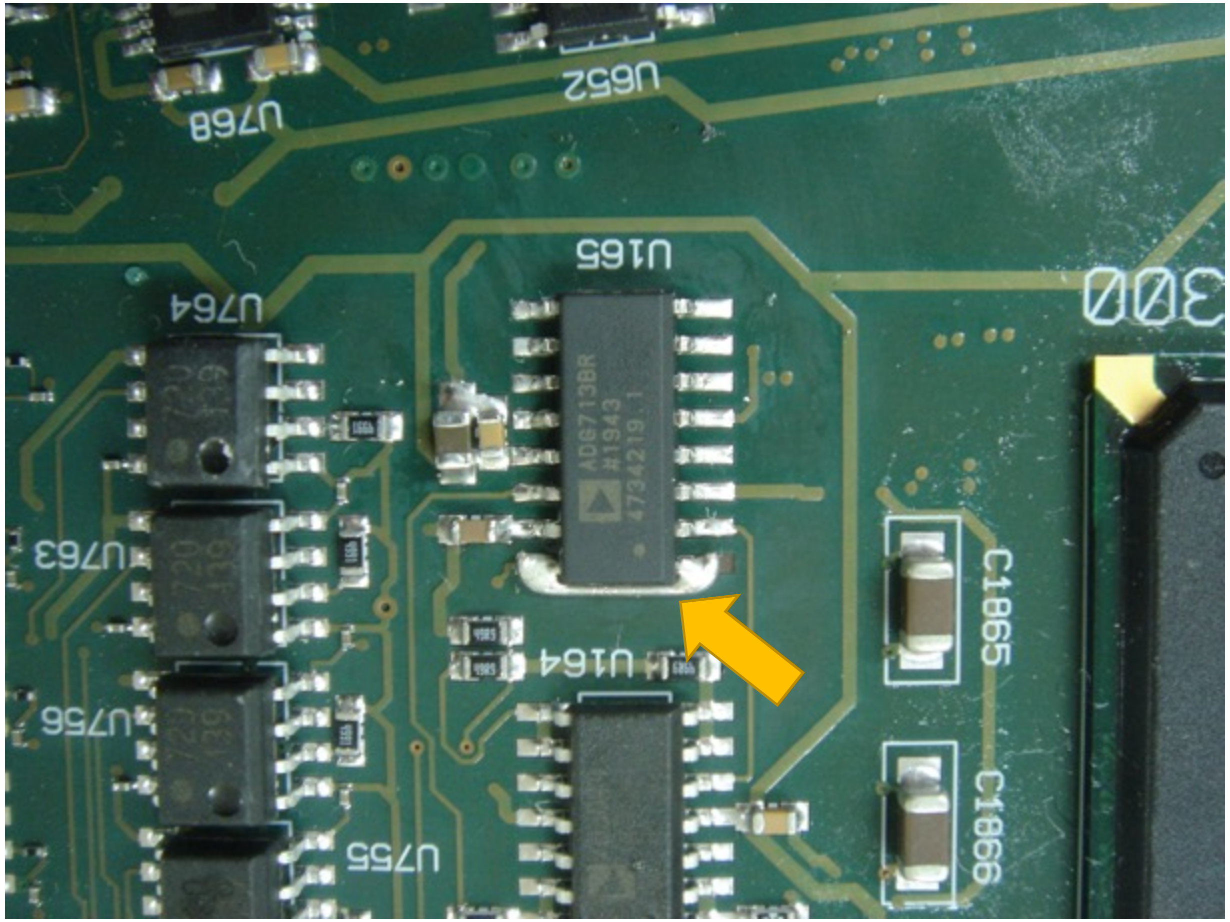
We did observed collapsed comma words which is the smoking gun of the fiber sync error. However, the cause has not been identified. Signal shapes, jitters etc all look normal. This problem remain no solution yet.

Repair Work Before/After

NE2 Column-C



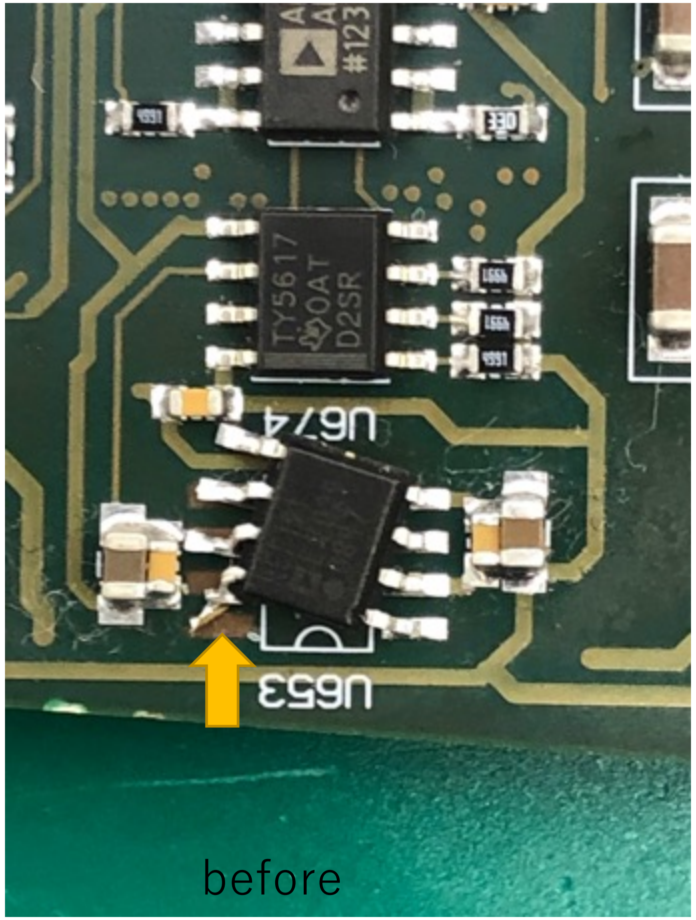
before



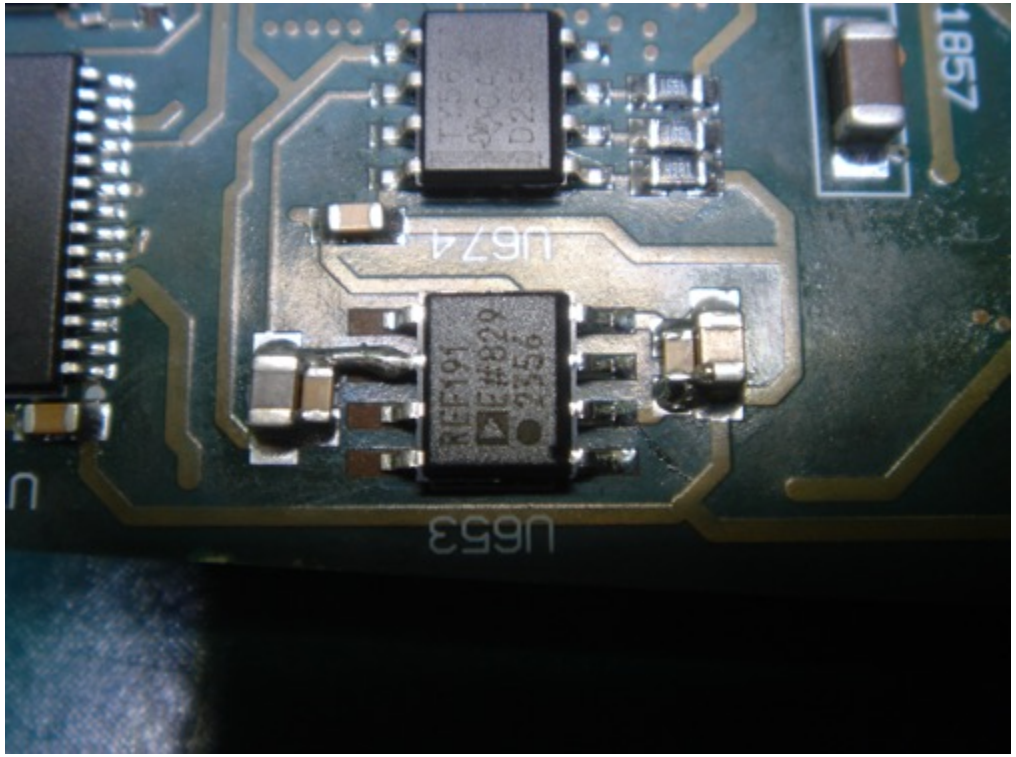
after

Repair Work Before/After

NW1 Column-A



before



after

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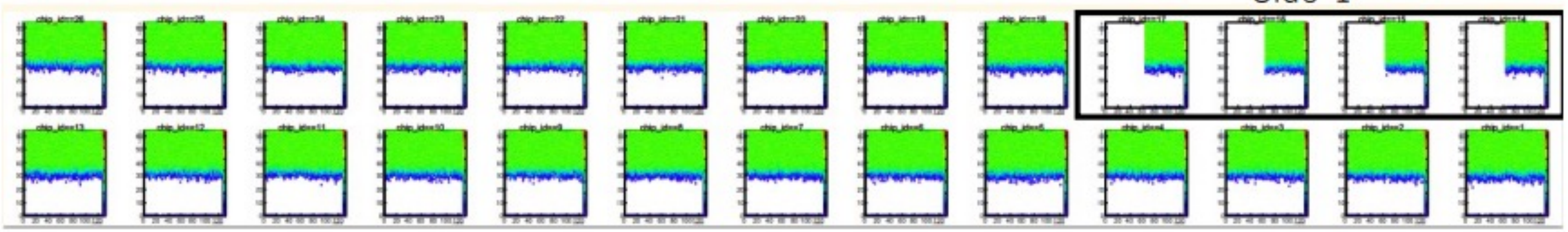
Good chance to be recovered

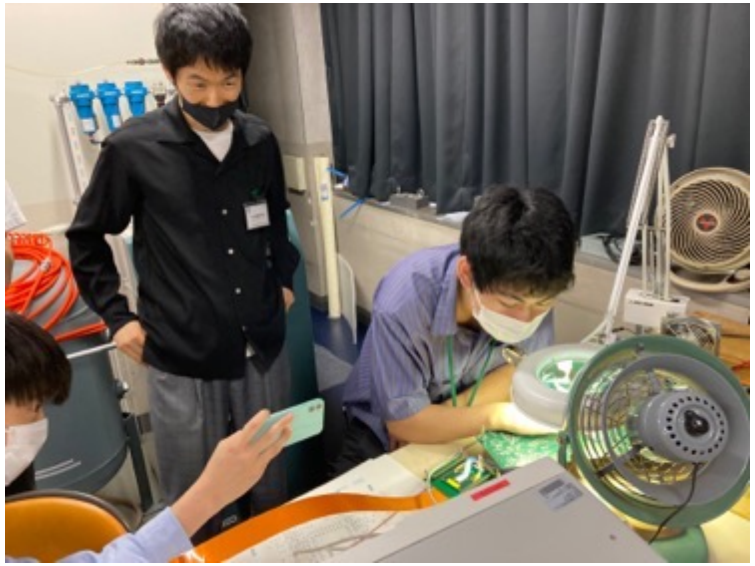
Partial Data Drop Issue

Looses part of data in D3 port with BEX + μ-coax conv. cable

Side-1



Side-0



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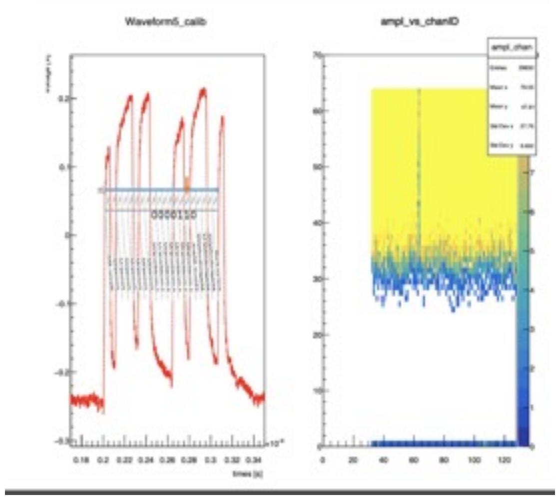
Investigation of the signal transmission with a high-speed oscilloscope.



The conclusion is :
Most likely, the data for these missing channels are not sent out from FPHX.
Need to confirm the FPHX registers.
Further debugging is pended for the readbacker to work with BEX by modifying SC FPGA code at ROC.

Summary

- ROC tests are still ongoing by Rikkyo undergrads.
- Classification of symptoms are more or less established by now.
- Issues associated with power/calibration have been recovered and have a good chance to be recovered after repair.
- Issues associated with fiber sync error or partial data collapse/missing are yet established solution. Keep investigation.
- Paper works for 2 more class-2(1) ROCs export is in progress. Target delivery to BNL is end of August.