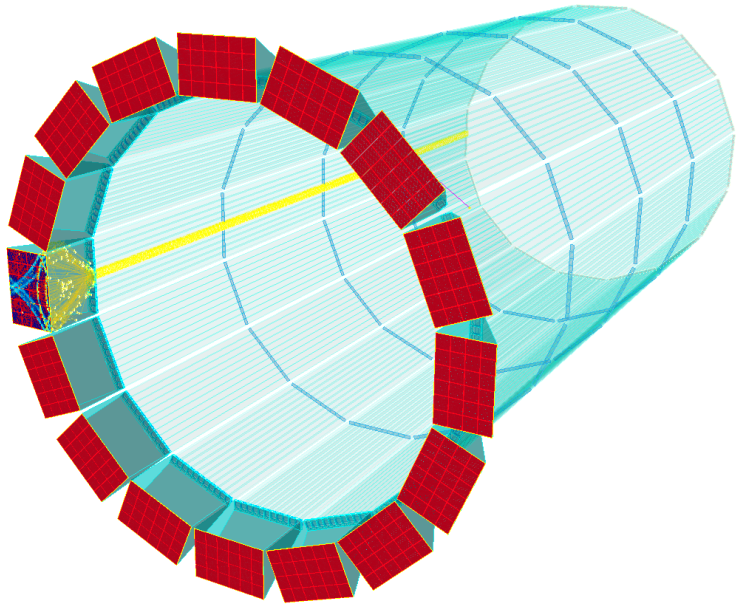
THE HIGH-PERFORMANCE DIRC

Greg Kalicy CUA

Jochen Schwiening GSI



- hpDIRC design
- Readout requirements
- Potential solution

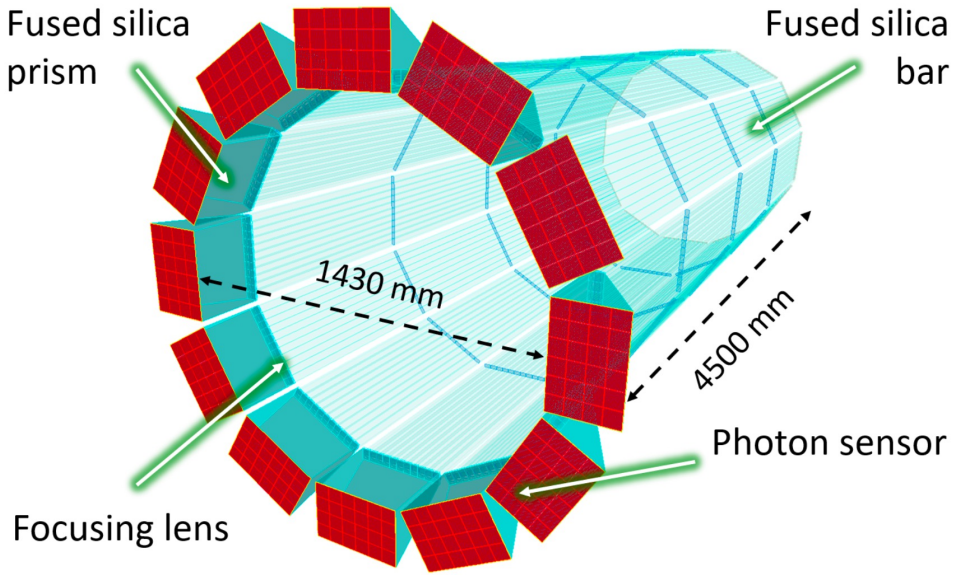
EIC EPIC HPDIRC

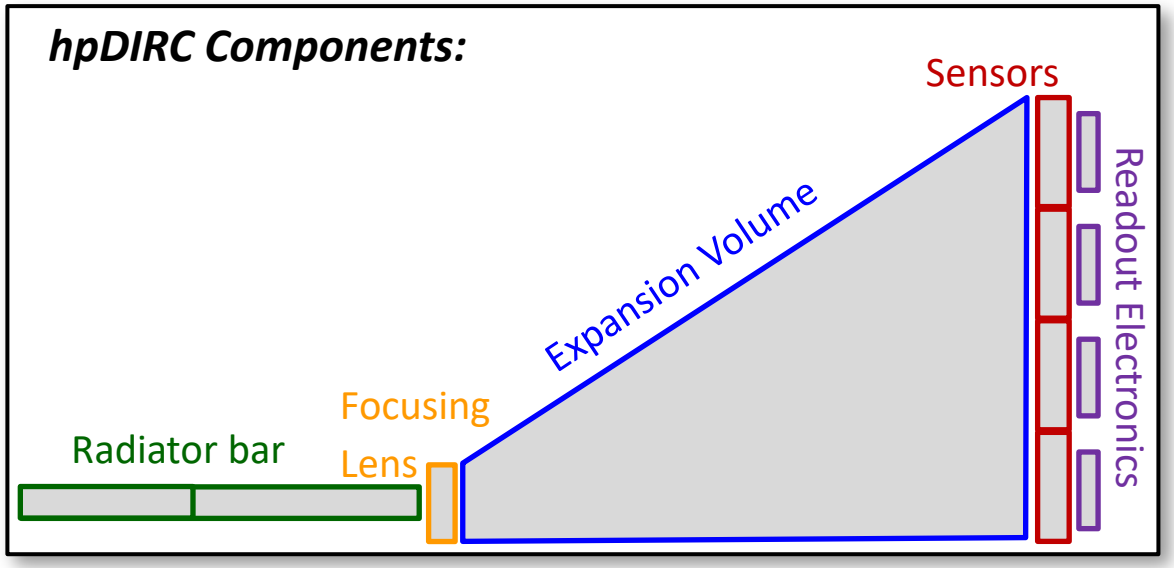
- **Barrel hpDIRC with 72cm radius**
- **Radiator bars:**
  - **420cm bar length** (works with both reused BaBar DIRC bars or new bars)
  - **12 bar boxes**, 10 long bars side-by-side in a bar box, 3 BaBar DIRC bars plus one half BaBar DIRC bar glued to form one long bar (or 3 BaBar DIRC bars plus one new short plate)
- **Focusing optics:**

  Radiation-hard 3-layer spherical lens
- **Expansion volume:**

  Solid fused silica prism: 24 x 36 x 30 cm^3 (H x W x L)
- **Readout:**

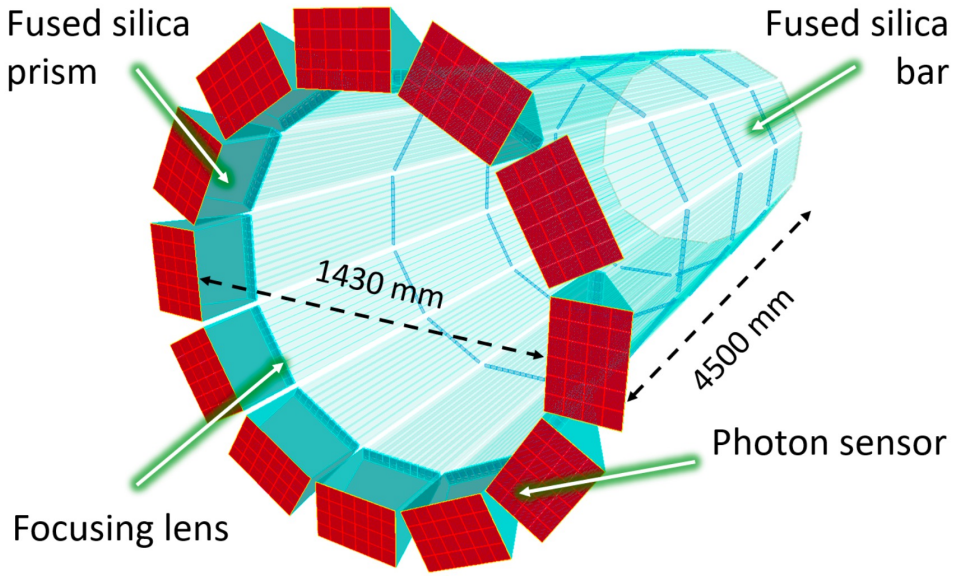
  PHOTONIS MCP-PMT Sensors + NALU's based Readout Electronics



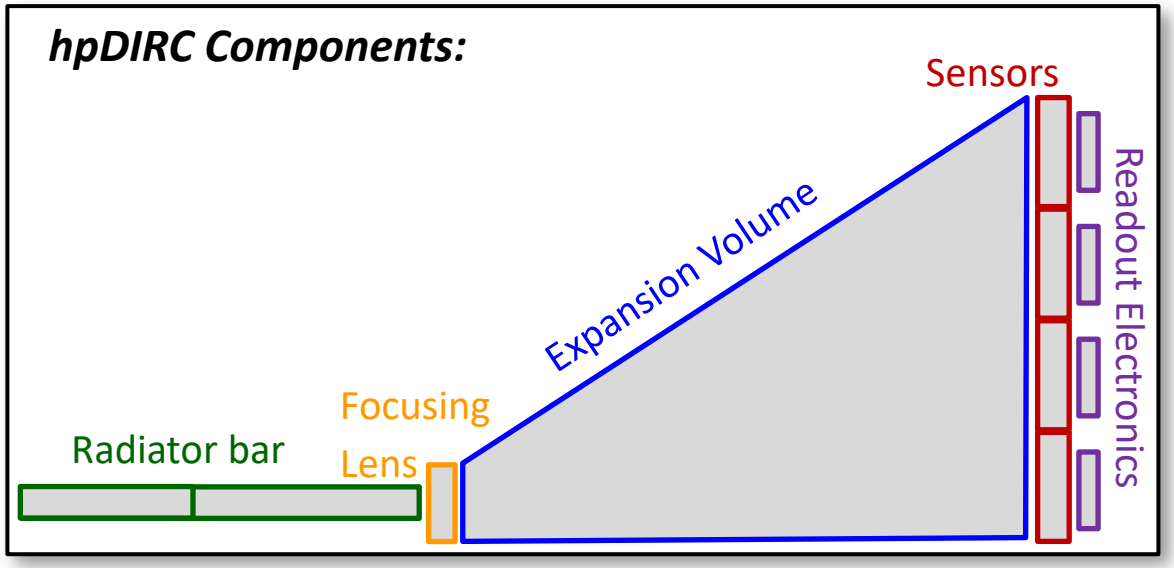


HPDIRC READOUT

- **Readout:**
  PHOTONIS MCP-PMT Sensors + NALU's based Readout Electronics
  - Total of ~74k channels.
  - 288 sensors (256 pixels/sensor)
  - 24 sensors and 6144 channels per barbox



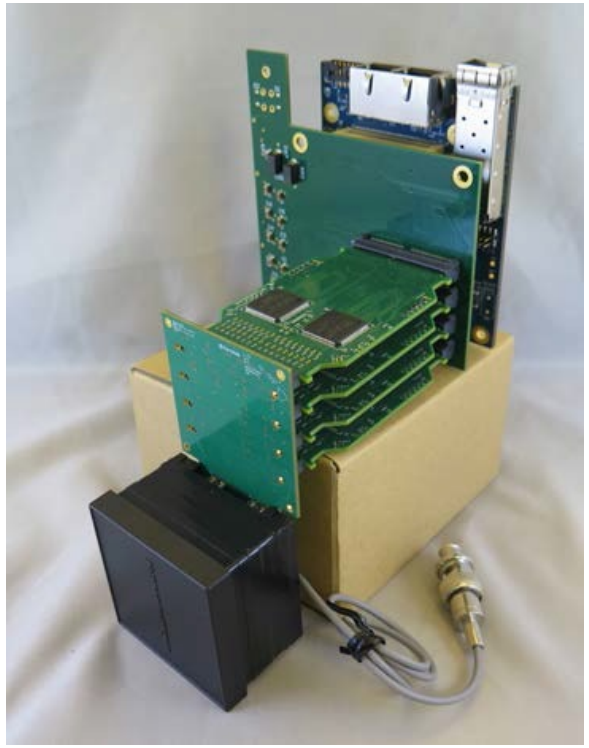
- **Expected ~500 Cherenkov photons per event (plus unknown possible accelerator background)**
- **Noise rate:** we assume the typical dark count levels for commercial MCP-PMTs for now, ~100Hz per cm^2 of MCP-PMT active area.



HPDIRC READOUT

hpDIRC unique readout requirements:

- All three leading sensor candidates (MCP-PMT, MAPMT, SiPM) share:
  - Large number of small pixels
  - Fast single photon timing
  - Relatively high photon rates and sensor occupancies
- Readout electronics must maintain 60-100ps timing resolution, matching sensors
- Performance requirements for e.g. triggerless streaming, data reduction, bandwidth, latency and throughput must be achieved while simultaneously meeting technical requirements for other critical factors such as e.g. power consumption, integration issues at the detector front end along with robust electromechanical sensor interfaces and biasing
- There is **NOTHING** on the market that meets all requirements and scales well



HPDIRC READOUT

- **High Density digitizer System on a Chip (HDSoC):**
  New front-end readout system based on the waveform sampling low-power, higher-performance SiREAD ASICs.

- ASICs integrated on boards directly matching the footprint of the sensor

- Readout cards are arranged as a board stack, placed behind the photosensor, permitting seamless abutting of the sensor array

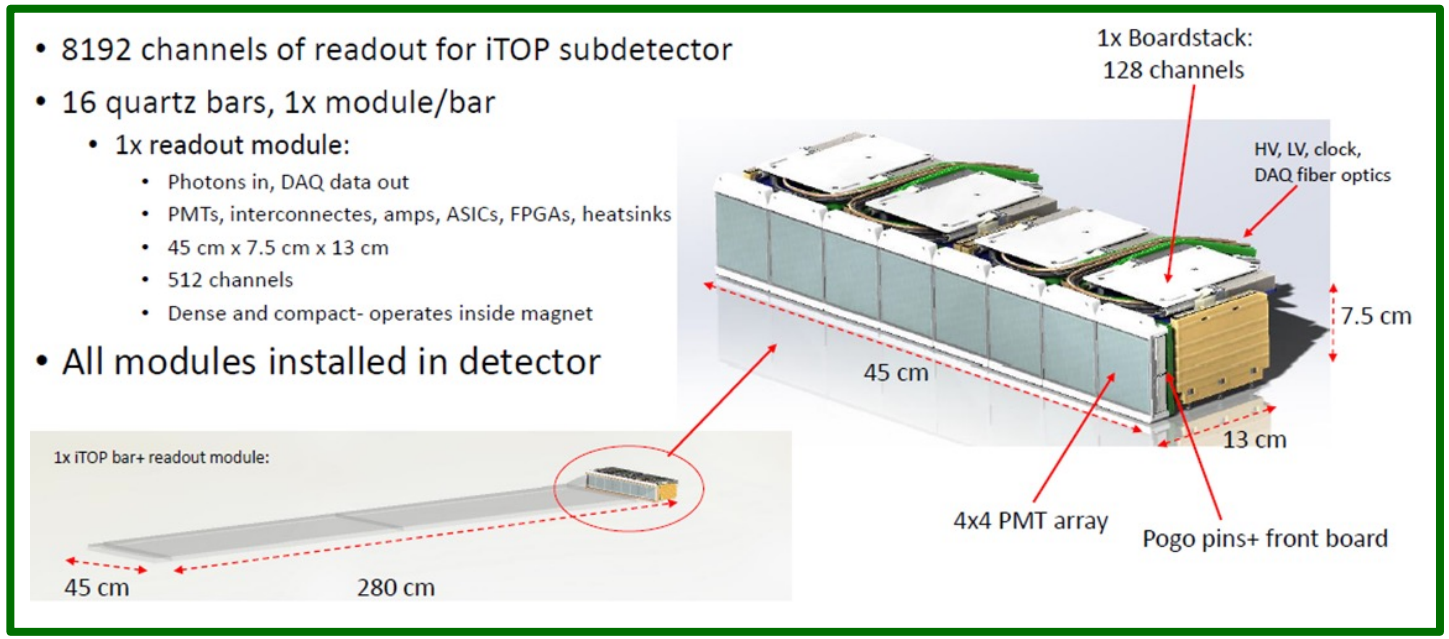
- A simple and standard power and serial interface allows groups of these 256- anode devices to be collected into a single ethernet acquisition node

HDSoC Parameter	Specifications
Channels	64
Sampling rate	1-2 GSa/s
Storage samples/ch	4096
Analog Bandwidth	0.7-1.1 GHz
RMS Voltage Noise	<1mV
Dynamic Range	10-11 bits
Signal Voltage range	2.1 V
ADC on Chip	12-bits
Feature extraction	on chip
Readout	Serial LVDS
Power Consumption	20-40 mW/ch

HPDIRC READOUT

The close collaboration between Nalu and UH was established several years ago in the design, fabrication and deployment of the Belle II DIRC TOP detector (below left), which shares many similarities to the hpDIRC.

The TOP project was awarded the DOE's Project Management Achievement Award in 2017, and was completed two months ahead of schedule and under budget while meeting or exceeding all objective Key Performance Parameters.

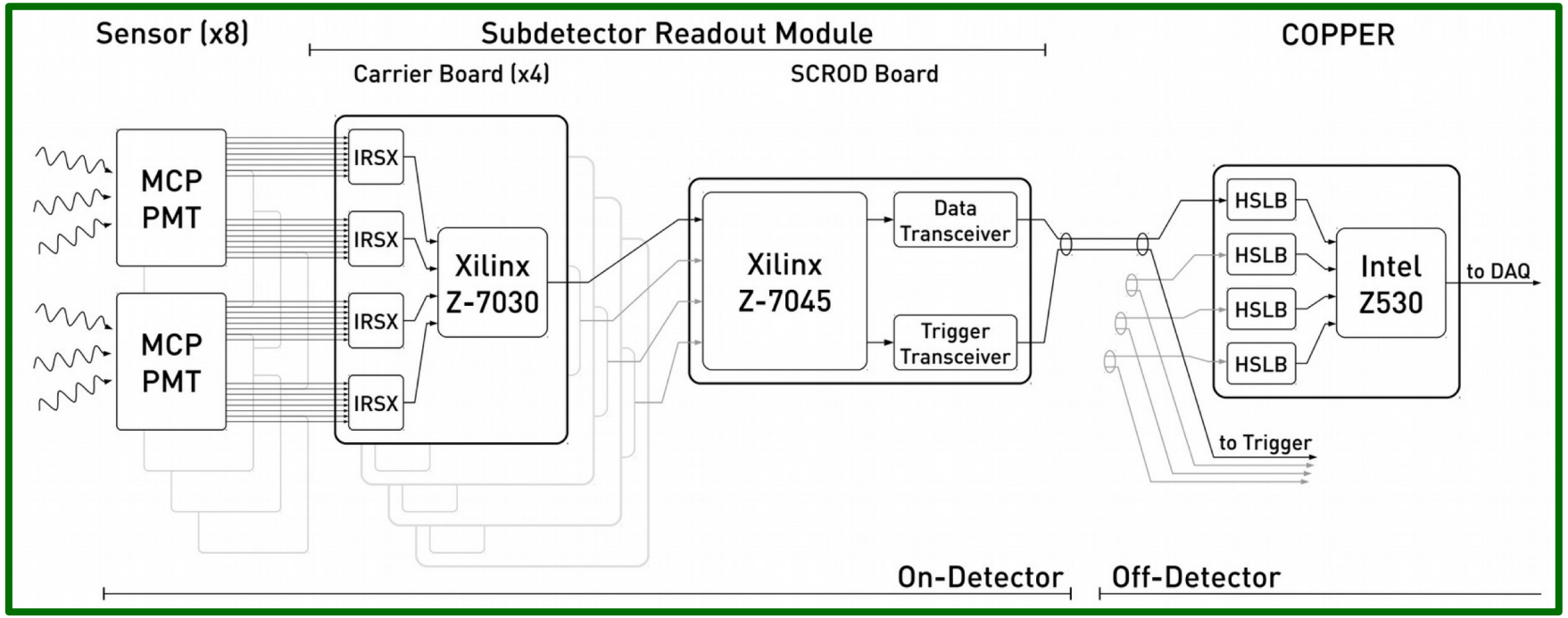


Belle II TOF TOP example of similar readout

HPDIRC READOUT

Schematic view of the data flow through a TOP subdetector readout module

Belle II TOF TOP example of similar readout (EPIC readout will be triggerless and more integrated on the chip)



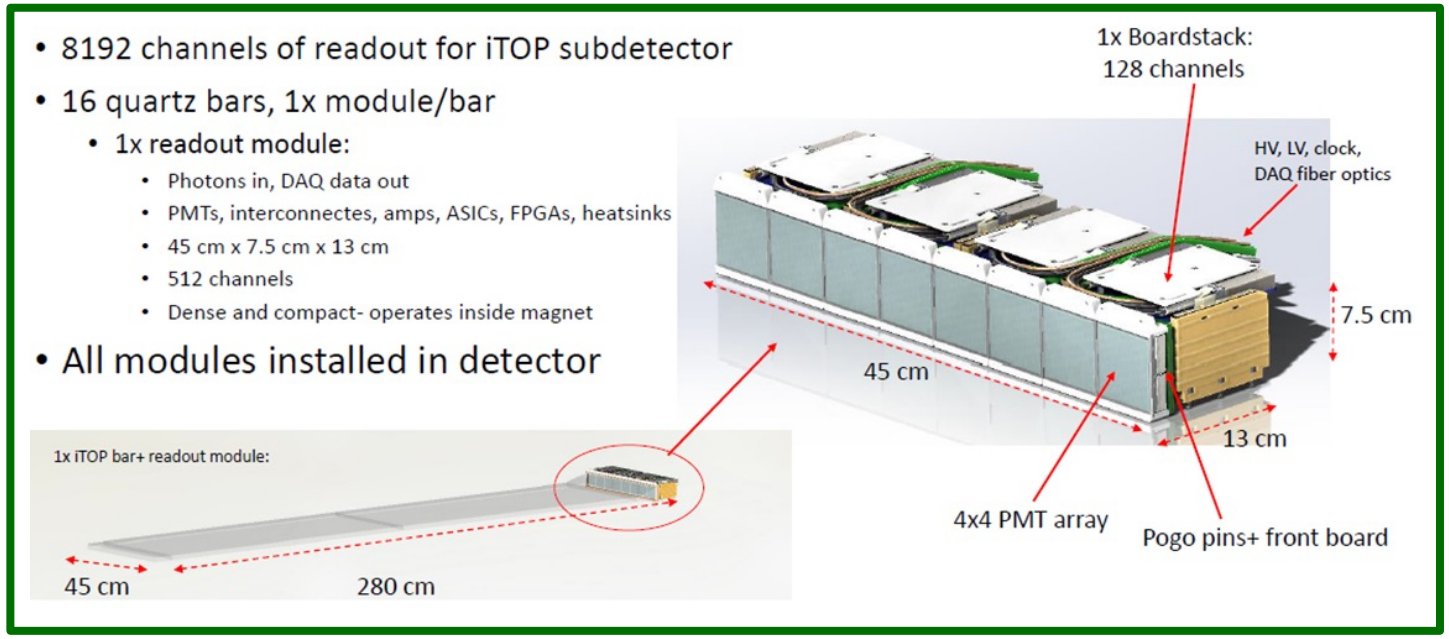
The MCP- PMT sensors on the left detect incident photons. The IRSX ASICs mounted on the four Carrier Boards sample the output of the sensor channels and convert the acquired analogue waveforms to a digital representation. This digitised waveform is read out by the Z-7030 controller SoC mounted on each Carrier Board and transferred to the attached SCROD Board via an SRM- internal serial link. The SCROD Board is equipped with a Z-7045 SoC which processes the waveforms and sends out sparsified event data via ~20m long optical data links to the off- detector COPPER boards. Each COPPER board receives data from four TOP SRMs (corresponding to a whole quartz bar module) and forwards the data to the Belle II DAQ system

HPDIRC READOUT

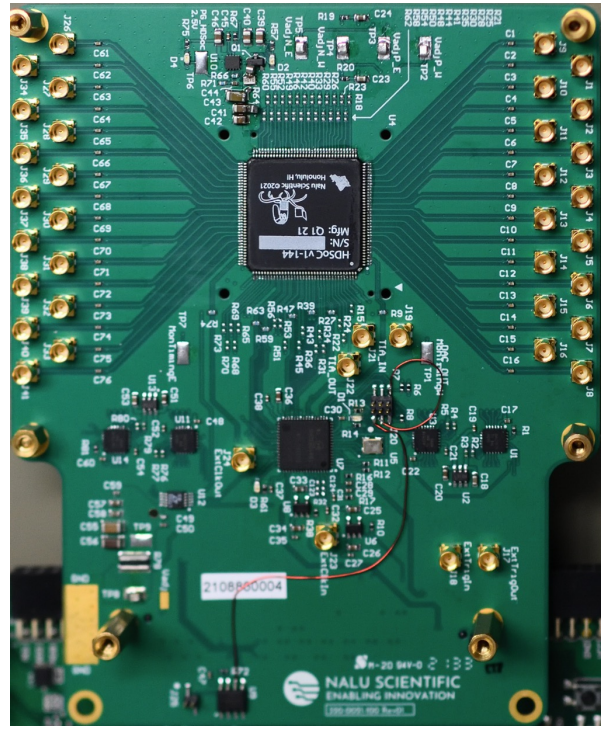
The close collaboration between Nalu and UH was established several years ago in the design, fabrication and deployment of the Belle II DIRC TOP detector (below left), which shares many similarities to the hpDIRC.

The TOP project was awarded the DOE's Project Management Achievement Award in 2017, and was completed two months ahead of schedule and under budget while meeting or exceeding all objective Key Performance Parameters.

Nalu's HDSoC ASIC (32-chnl test board below right), currently under development with a DOE Phase II SBIR, is well matched to EIC-PID's performance and technical requirements and the plan is to continue to evolve the platform to systematically address the challenges inherent in ultimately bringing the full EIC detector(s) online and ready for physics data-taking.



Belle II TOF TOP example of similar readout



Readout Electronics Ideal Plan (~1 year delayed)

FY'22- Develop and de-risk electronics

- Use 32ch HDSoC eval card as a building block to readout a subset of channels of various sensors (Photonis, HRPPD, Photek…)
- Nalu will provide 32 ch HDSoC eval board+engineering knowhow and FW/SW customization
- UH will provide post-doc and lab for testing and data analysis - prepare for cosmic telescope testing (for 32 or 64ch)
- Nalu will develop and fab the 64 channel HDSoC using Phase II SBIR funds
- Preliminary design for a modular integrated readout solution.

FY'23 - Prepare for summer '23 beam tests

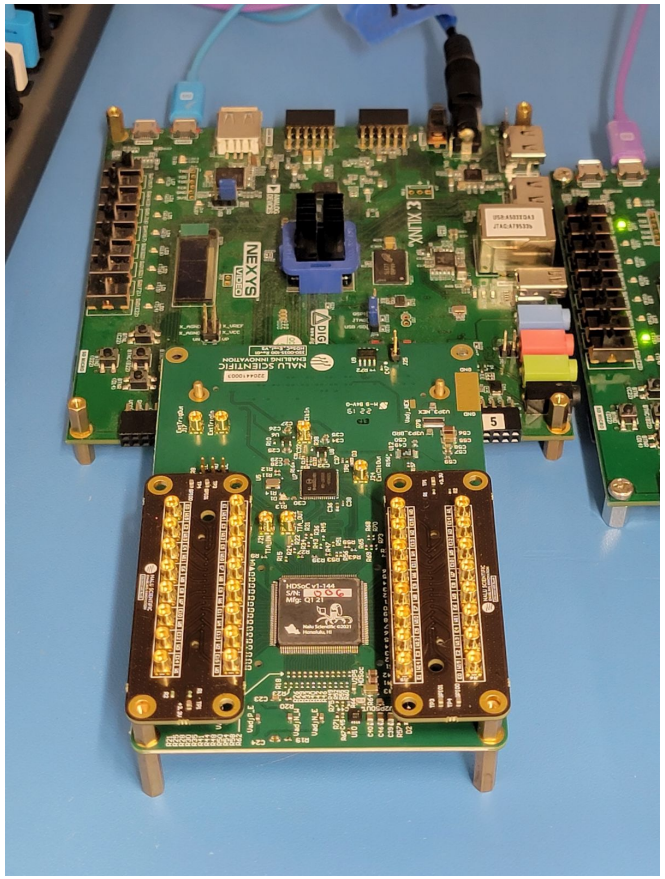
- Design and fab sensor specific 4-6k channel electro-mechanically integrated readout based on 64ch HDSoC (with design reuse in mind) and prepare for beam tests - contingent on proper budget allocation and prompt start on day one of FY23.
- Perform beam tests, analyze data and present results
- Perform a study on ASIC customization for various subdetectors (SBIR funds slightly more generic R&D than detector specific work).

FY'24-25- ASIC and electronic customization

- Customize HDSoC for speed (60ps resolution), data rates, processing capacity of each detector.
- Fab, package, test and qualify - rather low risk given underlying ASIC is mature
- Design high channel count subdetectors using customized ASICs.

FY'26-27 - Mass production

- Design for cost, dedicated ASIC fab and packaging.
- Board level designs tweaked for cost and sent to contract fab/assy houses
- Calibration, qualification, installation.



Readout electronics schedule matched hpDIRC timeline, now is slightly behind

From discussion

Comments from Oscar:

- **Schematic on slide 7** shows how it's done in the Bell II TOP system exactly. New system (for hpDIRC) is a similar ASIC with very similar features, but a lot more integration. So the the ASIC that is used in the Bell TOP system works as follows: the ASIC gives us waveform fragments or strings but all we transfer out, after feature extraction on FPGAs, to the DAQ side is for every single pulse, amplitude, and most importantly, the timing.

- **In new version for hpDIRC integrating this feature extraction into the ASIC so we don't need the incredible FPGA processing power that was needed in TOP.**

- **Timing for TOP:** After calibration the right rising edge time resolution is 85 ps per channel for single photon with Hamamatsu MCP-PMTs, pure electronics of this chip it goes down to 20ps.

- **Synchronisation of boards:** In TOP the boards are not synchronised, they are all connected to the same clock distribution system. But cable lengths are different. One module becomes T0 and is used to calibrate out the phase differences between different parts. This is not a problem and can get down to sub-picosecond accuracy and is tracked day by day. Sometimes for example, with firmware changes, one can see jumps there, but if nothing else changes it's basically stable on the sub-picosecond level, so it's never a problem for overall resolution. One can easily calibrate this out with muons, clean physics channels or laser pulses.