Ideas for possible contribution to the EPIC-TOF project

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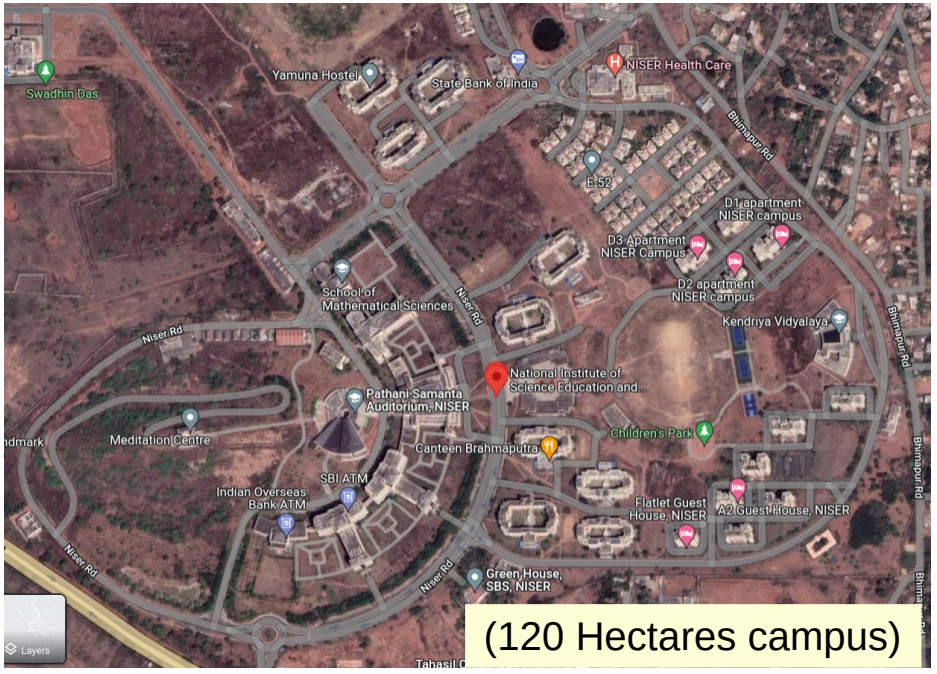
NISER - An autonomous Institute under
Department of Atomic Energy, Government of India



(120 Hectares campus)

NISER: https://www.niser.ac.in
CMRP: https://www.niser.ac.in/cmrp/

NISER group and background

- Team of 6 people: Interested to work on the EPIC-TOF project
  2 scientist (me - hardware and Mriganka- physics simulations),
  1 electronics engineer (Kirti prasad sharma),
  1 electronics (Deepak kumar), 1 mechanical assistant (Debasis barik),
  1 Technician (Subhash)
- We are currently part of the ALICE FOCAL project
  - Design, development, and production: n-and-p-type pad array (8x9) on 6'' wafer
  - Qualification studies of pad arrays (lab test, test beam experiments), ordered 25 pads
  - Focal physics simulations
- I have background in ALICE TPC upgrade (SAMPA ASIC tests) and ALICE ITS2 upgrade (ALPIDE MAPS tests, system integration), currently working in ALICE FOCAL project
- 20 m^2 ISO-6 clean room, 40 m^2 work space for silicon research lab, and various instruments required for detector qualification studies
- Working on collective funding proposal for EIC – EPIC, includes 20+ national institutes in India

NISER possible contribution – EPIC - TOF

- Could design and develop AC LGAD in Indian Fab
  - BEL Bangalore (6'' wafer), and SCL Mohali (8'' wafer, 180 nm process)
  - SiPMs were produced in India for CMS exp. in 2012 [Ref1] by SITAR*
- Could possibly contribute in simulations
  - TCAD (Process and Geometry),
  - MC (Garfield++) on detectors with gain as AC-LGAD
- LGADs require dedicated ASIC (FEE, TDC) to readout sensors
  - Either design or borrow or purchase such ASIC
  - Explore the possibilities to produce simple ASICs in Indian Si fab
- AC LGAD qualification studies: in lab (with sources, lasers, cosmic rays) and participate in test beam experiments

SiPM produced on 6'' wafers at SITAR, India

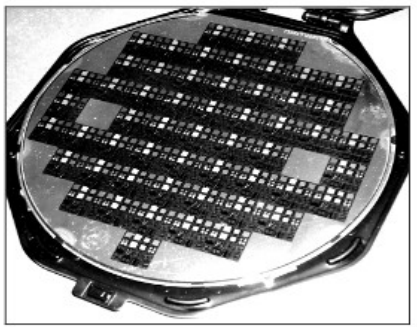
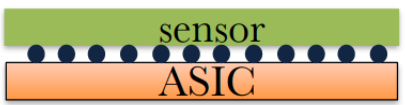


Fig. 1 Fabricated wafer showing SiPMs



LGAD + ASIC

*Society For Integrated Circuit Technology And Applied Research (SITAR)

[Ref1] Anita Topkar et al., Development of SiPM in India using CMOS Technology, https://inspirehep.net/files/2f05f40e82377fddbcaff41ae24635d1

Summary

- We could contribute in sensor R&D and construction
  - AC-LGAD production in Indian fab (8’’ Fab, 180nm CMOS capability)
- AC-LGAD coupled to Front-end ASIC qualification studies, test beam experiments
- In later stages: join the system integration, take detector calibration shifts, and related data analysis
- Detector simulations, Mechanical and Cooling related work

Thanks!

Backup!

https://www.scl.gov.in/cmos_fab_facility.html

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SCL | Semi-Conductor Laboratory
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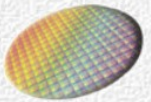
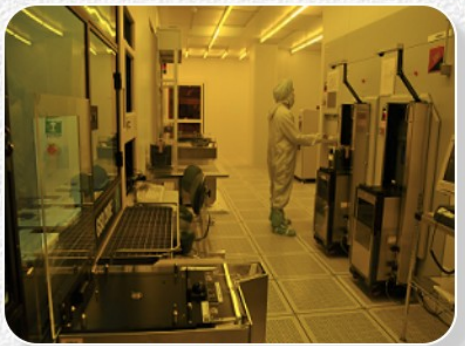


15 YEARS OF CELEBRATING THE MAHATMA

8" Wafer Fabrication Facility

- 180 nanometer CMOS Process for Fabrication of products in Digital, Mixed Signal and Analog domains
- Process Equipment Line, In-line Inspection & Metrology Tools and Support Utilities as per international standards
- Clean Rooms of Class 1, 10, 100 and 1000 with controlled environmental conditions
- Dedicated bays for Wafer Fabrication Processes viz. Diffusion, Lithography, Etching (Dry & Wet), Implantation, Thin Films working seamlessly from Wafer-in to Wafer-out
- BKMs (Best Known Methods) comprising regular Tool QCs, Preventive Maintenance and Process Control & Monitoring through in-line defect inspection & measurement through Metrology Tools as per industry standards
- Commensurate with the requirements of Fab Line, support infrastructure namely High Purity Systems, Utility Plants and Distribution Network operate on 24x7 basis



Implant Area

Thin Film Area

SCL 180nm CMOS foundry: High reliability ASIC design for aerospace applications

Publisher: IEEE

Cite This

PDF

https://ieeexplore.ieee.org/document/7208163

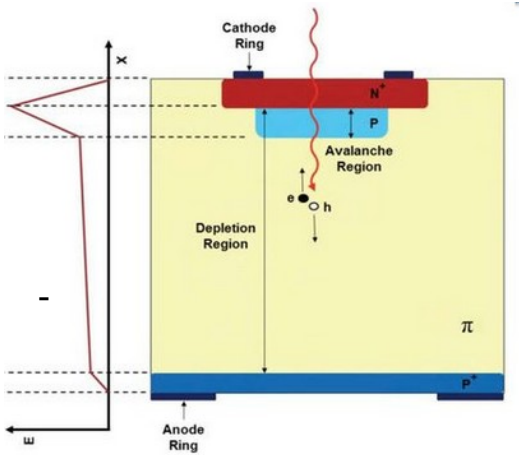
Shri H. S. Jatana ; Nilesh M. Desai **All Authors**

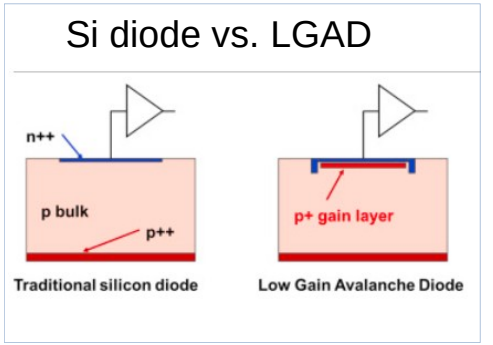
Abstract:

Semi-Conductor Laboratory (SCL) Fab. has been upgraded to 8" wafer fab to support 180 nm CMOS process made available by M/s. Tower Semiconductor Ltd, Israel. This tutorial describes SCL foundry process features and capabilities. The tutorial will cover SCL Fab base line technology features, analog process modules, digital standard cell library for core and I/Os and memory modules. End to end design flow of digital and mixed signal ASICs with case-study of recently completed ASIC designs along with EDA tools will be covered in this tutorial. SCL Packaging, testing and qualification capabilities will also be addressed. This tutorial will also cover the role of ASICs in various aerospace applications like remote sensing (microwave and optical), communication, navigation etc. Space radiation environment and its effect on electronics devices will be discussed in tutorial.

Low gain Avalanche Detector (LGAD)

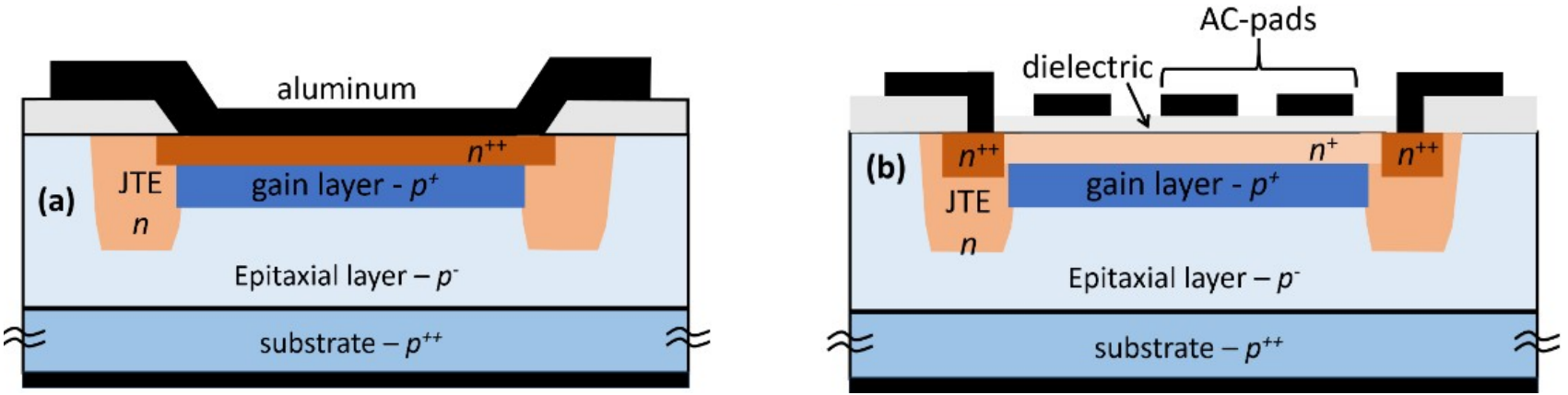
- LGAD R&D was started to explore radiation hard detectors, but now are popular for its time resolution ~ 20 ps to 50 ps
- LGAD Principle: In n-on-p type Si sensor add an extra thin p-layer (below the the junction) which increases the E-filed - the charge multiplication occurs with moderate gain (10 to 50) without breakdown (high breakdown voltage ~ 400 - 500 V)
- High doping concentration (in thin p-layer):
  High Field:- ultra fast charge collection
- Gain comparison with different Si devices:
  - Photodiode = 1
  - Avalanche Photodiodes (APD) = 100 - 1000
  - Single Photon Avalanche Photodiodes (SPAD) and SiPM = 10^7
- Typical thickness currently produced LGADs (30 μm to 300 μm)
  - Thinner sensors show better time resolution, but the detector capacitance increases (low SNR), hence sensor capacitance and internal gain optimization is crucial!
  - Time resolution drops with radiation dose, lots of R&D ongoing to improve





Ref: https://www.sciencedirect.com/science/article/pii/S0168900218317741

LGAD vs. AC LGAD



One of the main differences between AC-LGADs and standard LGADs:

- Replacement in AC-LGADs of the n++ layer by a much less doped n+ layer
- The electrodes, which the read-out electronics is connected to, are metal pads separated from the n+ layer by a thin insulator

Ref: https://arxiv.org/pdf/1906.11542.pdf