eRD24 Progress Report

EIC R&D Meeting, 3/25/2021

Alex Jentsch on behalf of eRD24

Electron Ion Collider

BROOKHAVEN NATIONAL LABORATORY

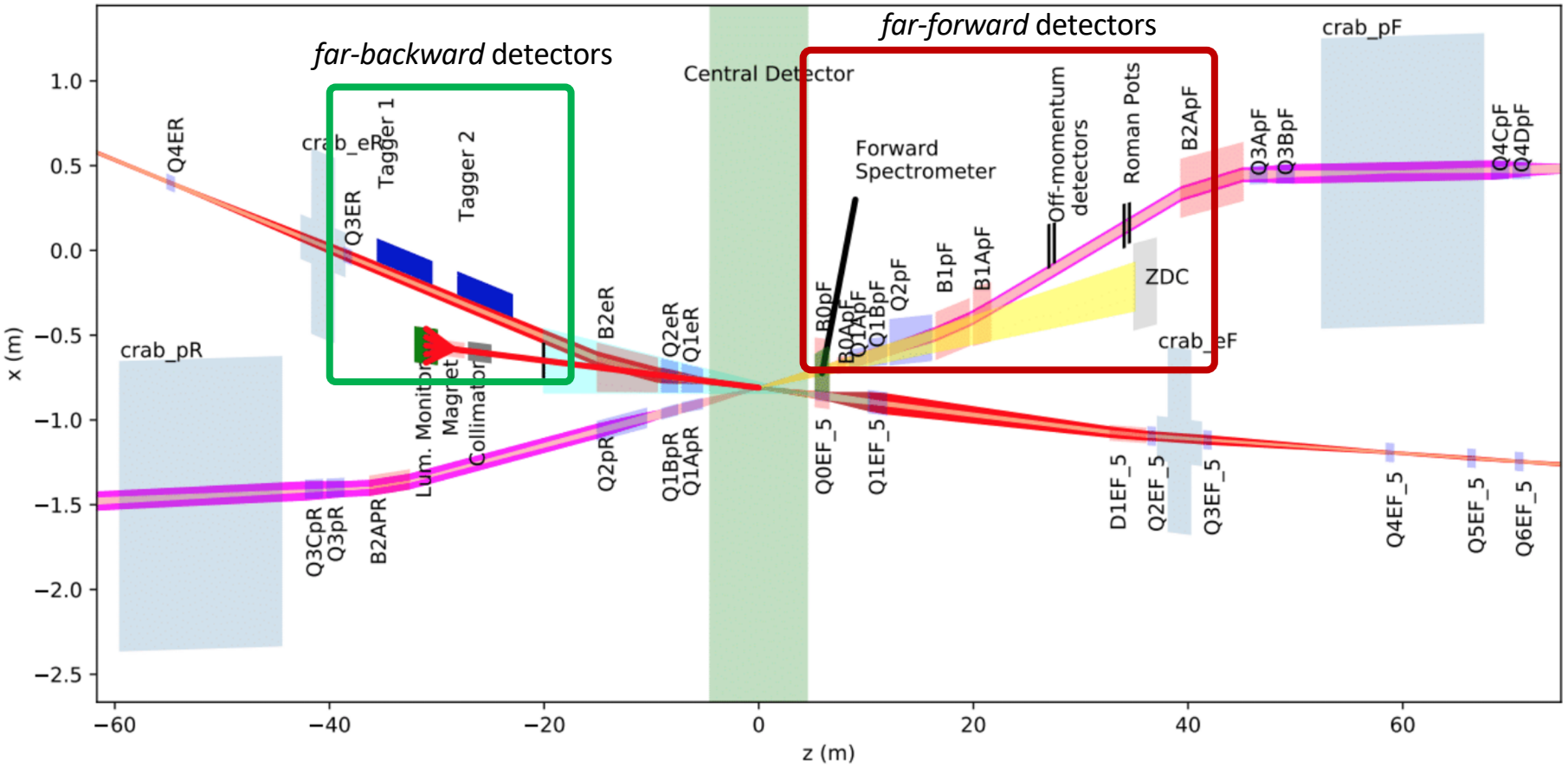
U.S. DEPARTMENT OF ENERGY | Office of Science

eRD24: Silicon Sensors with High Position and Timing Resolution for Roman Pots at the EIC

Project members
E.C. Aschenauer (BNL), A.Tricoli (BNL), A. Jentsch (BNL), S. Fazio (U. Calabria, Rende, Italy), A. Kiselev (BNL), G. Giacomini (BNL), Cinzia da Via (Manchester/SBU), M. Benoit (BNL), A. Seiden (UCSC), H. Sadrozinski (UCSC), B. Schumm (UCSC), R. Dupré (IJCLAb, Orsay, FR), D. Marchand (IJCLAb, Orsay, FR), C. Munoz Camacho (IJCLAb, Orsay, FR), L. Serin (IJCLAb, Orsay, FR), C. de La Taille (Omega, Palaiseau, FR), M. Morenas (Omega, Palaiseau, FR)

- **Expertise**
  - EIC physics, simulations, and detectors.
  - Sensor technology and development (LGADs) from LHC.
  - Readout electronics (ASIC) from LHC.

EIC Interaction Region Layout



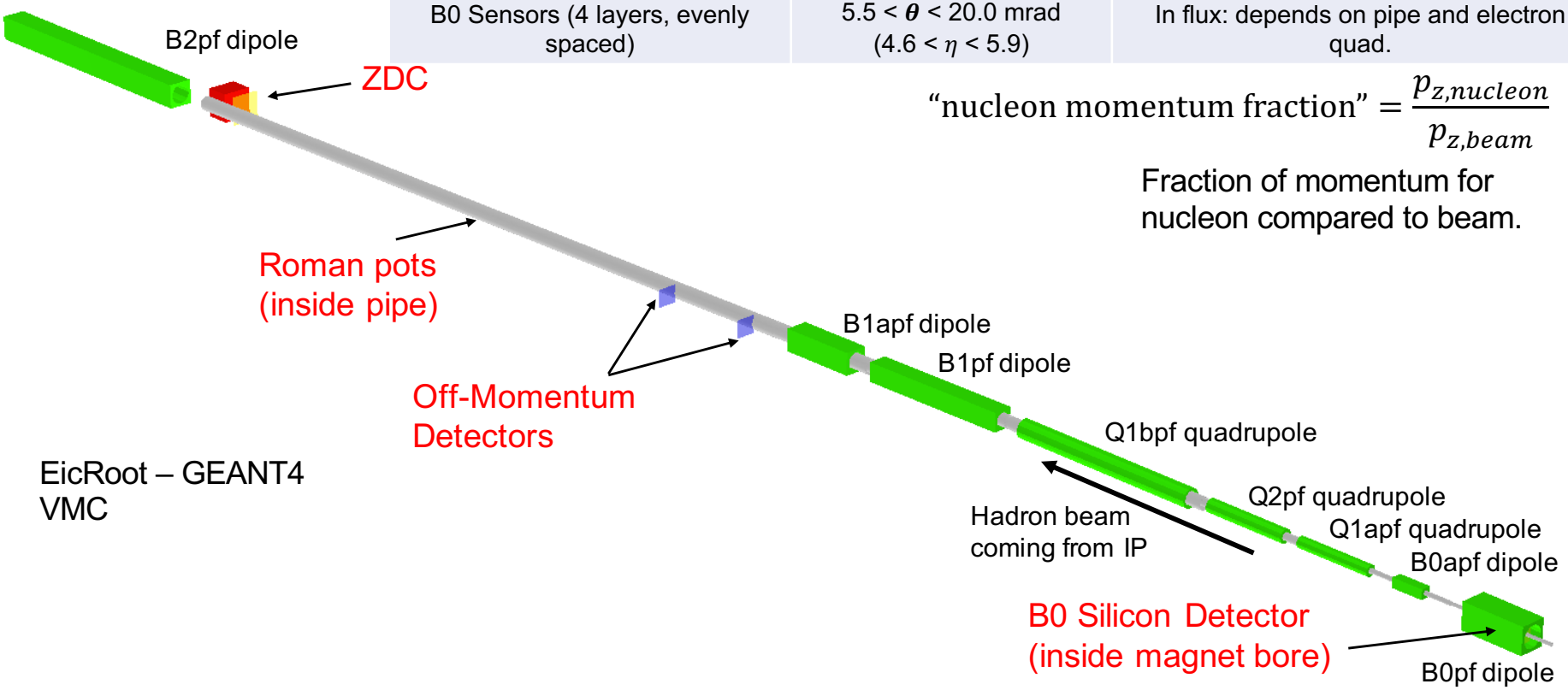
- Central detector spans -4.5 to 5 meters and is machine-component free (except for beam pipe).
- Hadron-going and electron-going directions after central detector fully instrumented.
- Hadron and electron beam cross with an angle of 25 mrad.

FF Hadron-Going Direction & Acceptance

Detector	Acceptance	Notes
Zero-Degree Calorimeter (ZDC)	θ < 5.5 mrad (η > 6)	About 4.0 mrad at $\phi \sim \pi$
Roman Pots (2 stations)	0.0* < θ < 5.0 mrad (η > 6)	$0.65 < \frac{p_{z,nucleon}}{p_{z,beam}} < 1.0$ *10σ cut
Off-Momentum Detectors (OMD)	0.0 < θ < 5.0 mrad (η > 6)	Roughly $0.3 < \frac{p_{z,nucleon}}{p_{z,beam}} < 0.6$
B0 Sensors (4 layers, evenly spaced)	5.5 < θ < 20.0 mrad (4.6 < η < 5.9)	In flux: depends on pipe and electron quad.

$$\text{“nucleon momentum fraction”} = \frac{p_{z,nucleon}}{p_{z,beam}}$$

Fraction of momentum for nucleon compared to beam.



Reminder: Requirements

- The various contributions add in quadrature (this was checked empirically, measuring each effect independently).

$$\Delta p_{t,total} = \sqrt{(\Delta p_{t,AD})^2 + (\Delta p_{t,CC})^2 + (\Delta p_{t,pxl})^2}$$

Angular divergence

Primary vertex smearing from crab cavity rotation.

Smearing from finite pixel size.

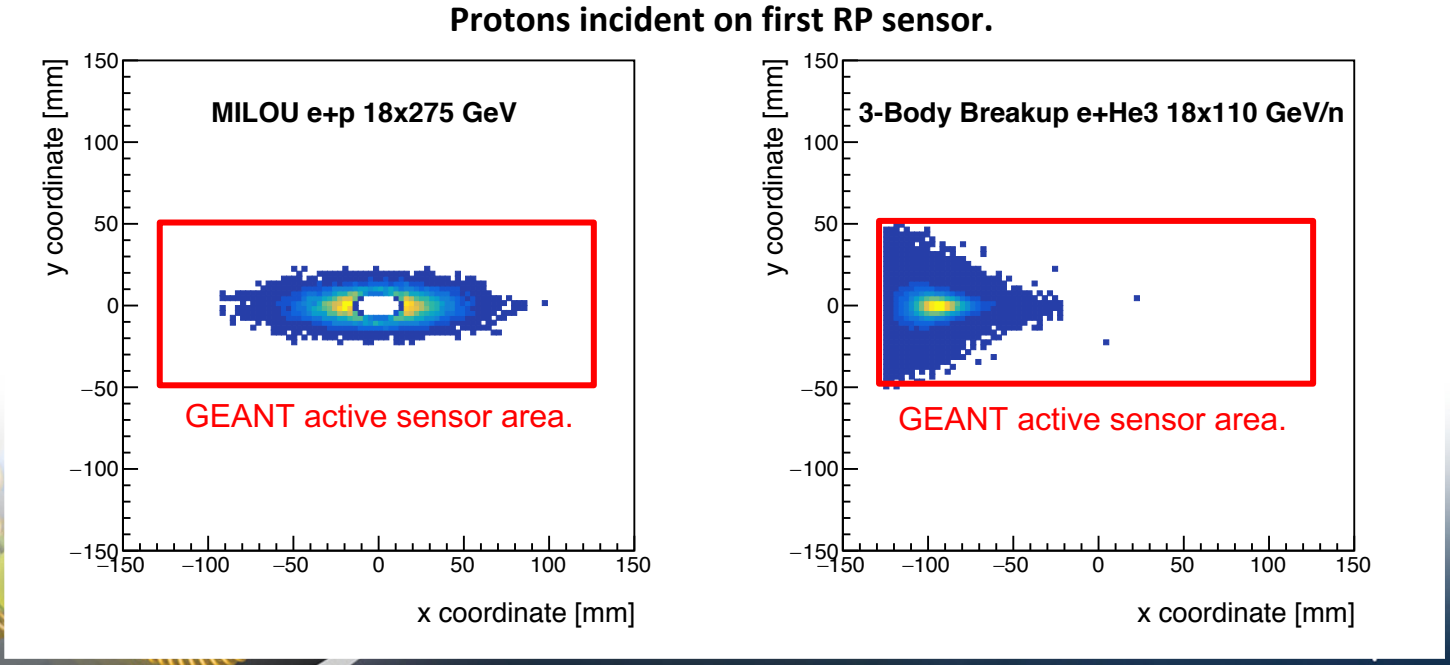
These studies based on the "ultimate" machine performance with strong hadron cooling.

	Ang Div. (HD)	Ang Div. (HA)	Vtx Smear	250μm pxl	500μm pxl	1.3mm pxl
$\Delta p_{t,total}$ [MeV/c] - 275 GeV	40	28*	20	6	11	26
$\Delta p_{t,total}$ [MeV/c] - 100 GeV	22	11	9	9	11	16
$\Delta p_{t,total}$ [MeV/c] - 41 GeV	14	-	10	9	10	12

- **Beam angular divergence**
  - Beam property, can't correct for it – sets the lower bound of smearing.
- **Vertex smearing from crab rotation**
  - Correctable with precise timing (~35ps).
  - ~70ps timing: effective bunch length is 2cm → 0.25mm vertex smearing (~7 MeV/c).
- **Finite pixel size on sensor**
  - 500μm seems like the best compromise between potential cost and smearing

Reinforcement of needed active area

- DVCS studies as a function of beam energy showed that a needed active area of ~ 25cm x 10cm was needed to provide full coverage at medium and low energy.
- Recent studies with e+He3 collisions show that this large active area is needed to tag the two spectator protons, reinforcing the requirement.



Recap of Physics and Specs

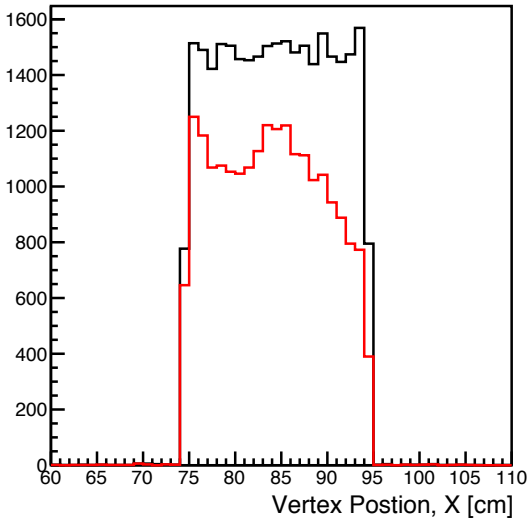
- **Physics Goals of Roman Pots**
  - Tag protons and light nuclei close to the beam from coherent processes, protons from nuclear breakup, etc.
    - Crucial for exclusive and diffractive physics.
- **Essential requirements gleaned from simulations**
  - Large active area (~25cm x 10cm)
  - Time resolution 30-50ps
  - 500μm x 500μm pixels
  - Edgeless (inactive edges ~< 150μm)
- AC-LGAD technology of choice to meet these requirements.

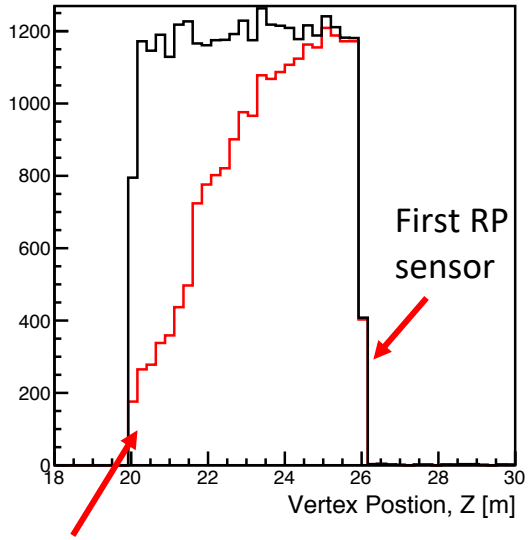
Open questions from last report and new study

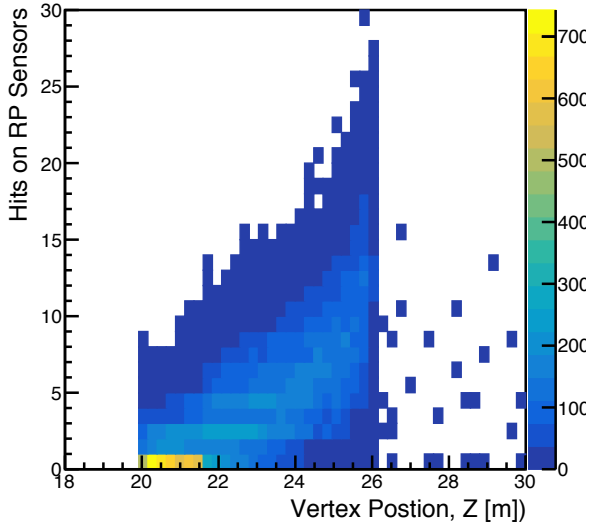
- What kinds of rates can we expect on the AC-LGAD sensors in the Roman Pots?
  - How does this translate to occupancies?
- What is the ideal design for a single sensor + ASIC?
  - How does this affect the layout for the full detector subsystem?
  - Estimate the chip area needed for an EIC optimized version of the ALTIROC as this may drive the minimum pixel size.
  - Estimate ASIC power dissipation.
- Understand accelerator clock's inherent jitter and transmission from the accelerator control room to experiment (in progress).

Backgrounds from beam+gas

- Collisions of beam hadrons with gas molecules in the beam pipe are a source of background for the Roman Pots.
  - Vacuum will be ~ 10^{-9} mbar in the drift region near the Roman Pots.
  - With the beam parameters in the CDR, collision rate will be ~ 500kHz, while the beam gas rate (assuming H_2 is dominant gas) is ~ 5kHz.



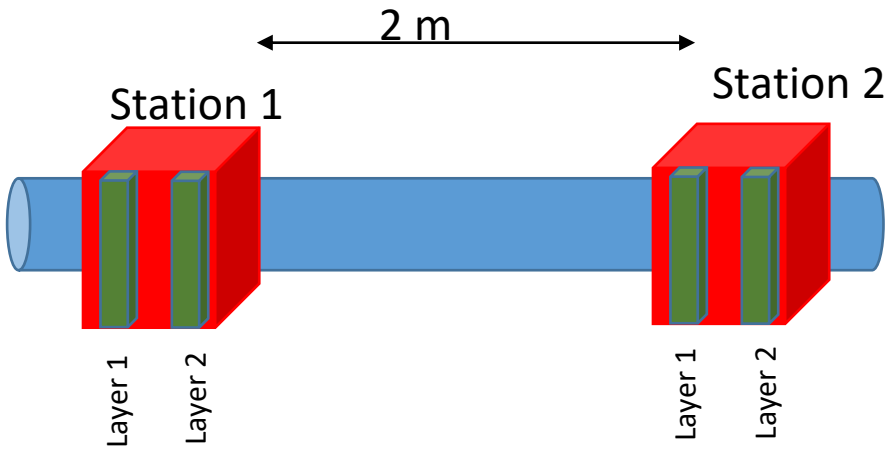


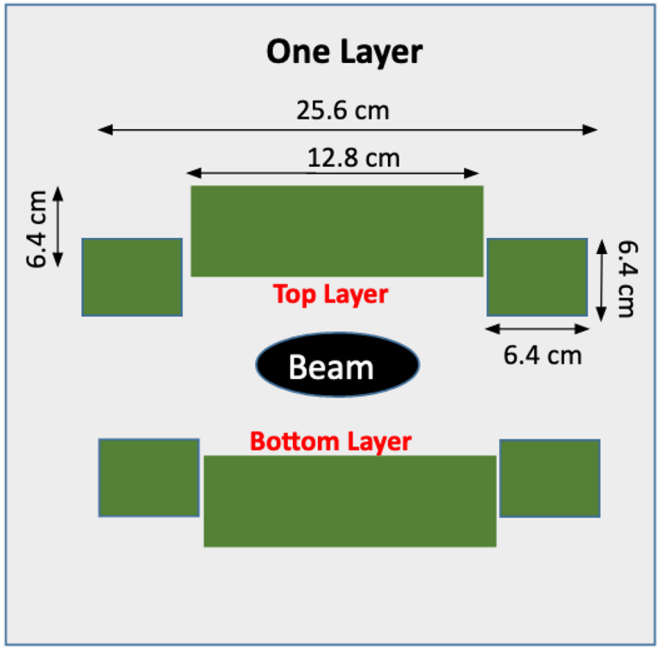


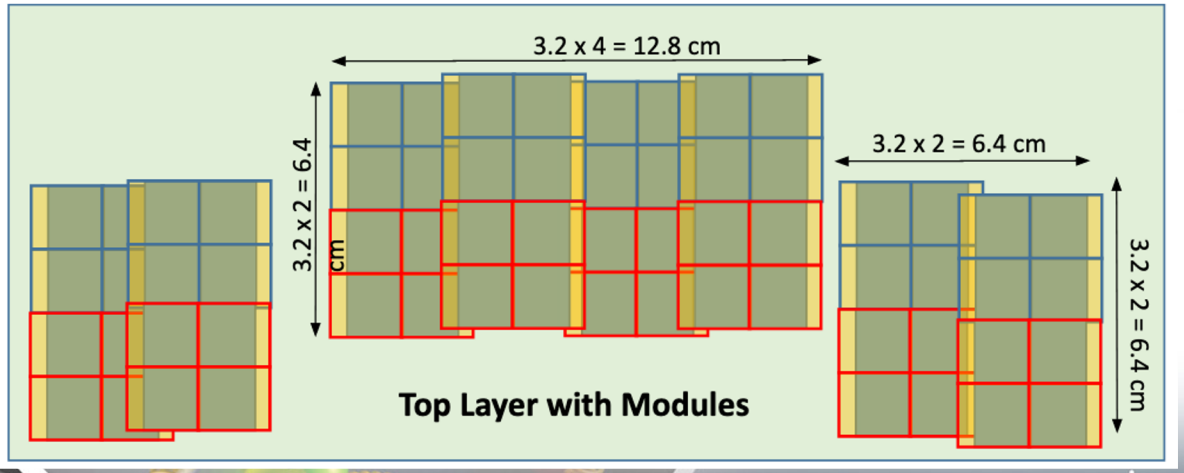
Only appreciable beam+gas events come from the drift area *after* the last dipole before the Roman Pots.

New Strawman Layout

- Updated strawman layout with current design for LGAD sensor + ASIC.

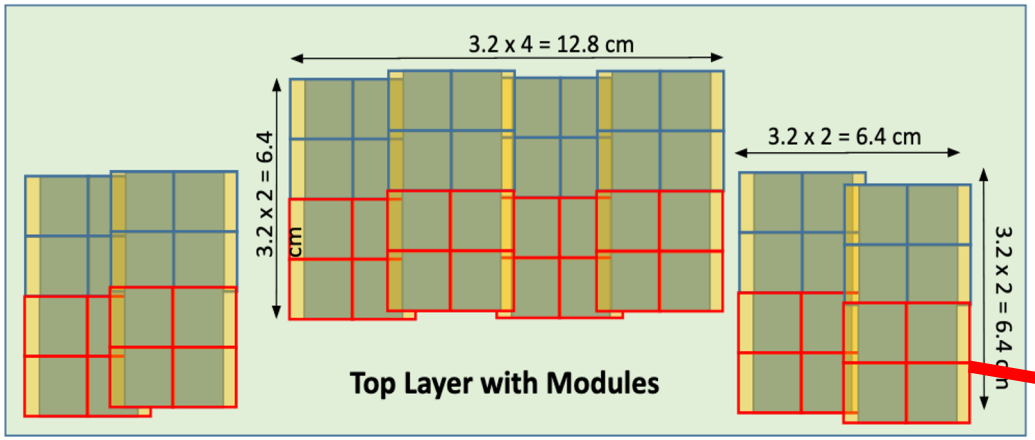


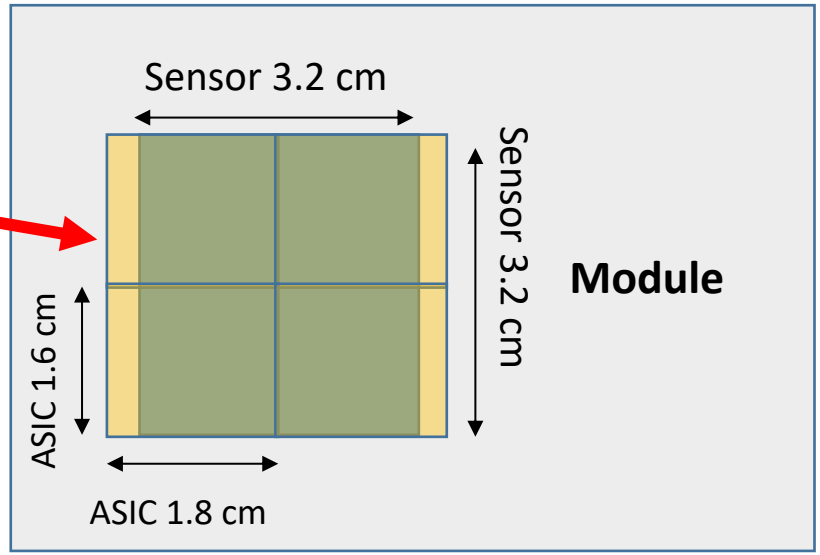




New Strawman Layout

- Updated strawman layout with current design for LGAD sensor + ASIC.





- As further developments are made, more of the realistic considerations can be included in the simulations as we move toward a TDR design.

ASIC size	ASIC Pixel pitch	# Ch. per ASIC	# ASICs per module	Sensor area	# Mod. per layer	Total # ASICs	Total # Ch.	Total Si Area
1.6x1.8 cm^2	500 μm	32x32	4	3.2x3.2 cm^2	32	512	524,288	1,311 cm^2

New sensor production at BNL

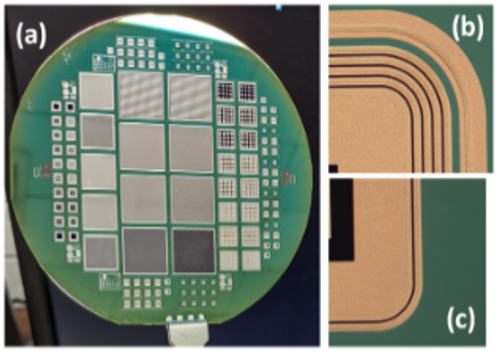
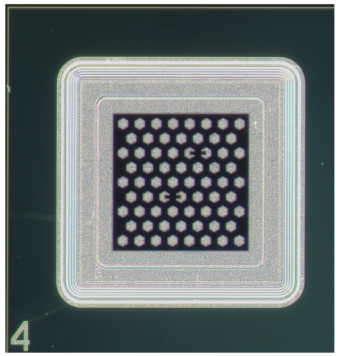
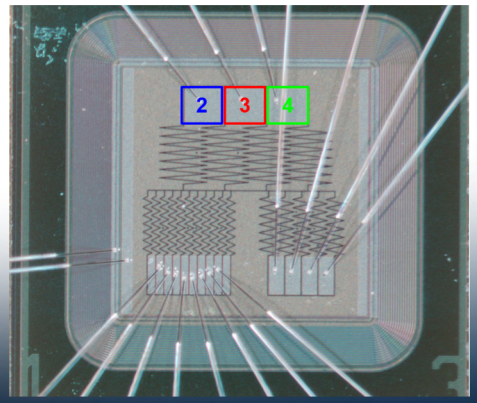


Figure 5: (a) picture of a 4" silicon wafer with the new layout. (b) corner of a device, showing the new termination, (c) slim termination featured in a subset of devices.

- New wafer production made at BNL
  - Same substrate as previous productions (4" diameter, 50 µm thick p-type epitaxial layer)
  - Process modified to correct flaws from preceding productions and those arisen from intensive tests
  - Many devices, with areas up to 1.4 cm x 1.4 cm, with a modified termination structure, including slim edges test structures.

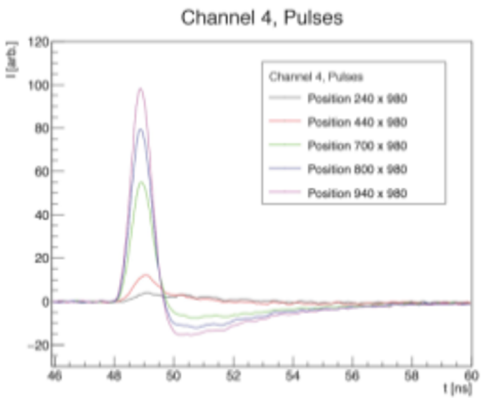


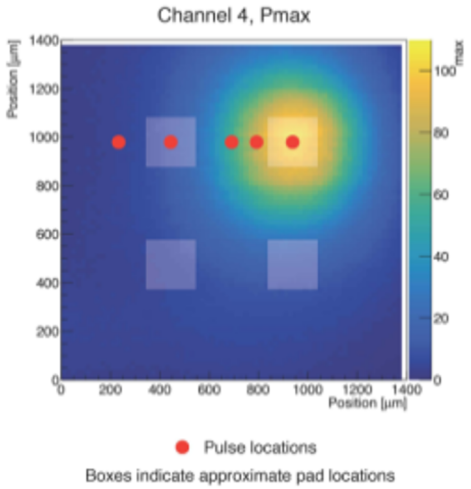
- Study of ultimate spatial resolution:
  - Strips with variable pitches and geometry (e.g. zig-zag, hexagonal, crosses)
  - Produced to test dependence of signal sharing (space resolution) on geometry - tested at test-beams.
  - Different geometrical patterns optimized for spatial resolution could allow for larger overall pixel size, and therefore less total pixels per sensor -> **leads to reduced number of channels and power consumption, and less cooling!**



Sensor Testing

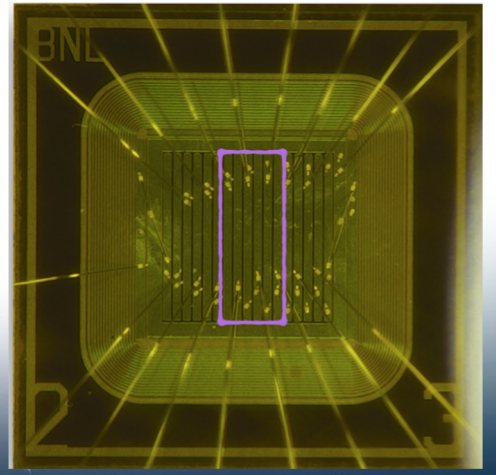
- Extensive testing in laboratories at BNL, UCSC (beta-particles, lasers scans), test-beams (FNAL)





- IR laser scans from the back of the sensor.
- Pulses close to a **pad with size 200 µm, pitch = 500 µm**
  ⇒ Signal height is a function of distance from readout pad
  - underneath the pixel metal is constant, 10% on next neighbor.
  - Signal from 4 pixels can be used to improve space resolution.
  - Size of pixel metal to be minimized to reduce capacitive pick-up between pixels and maximize information from signal sharing

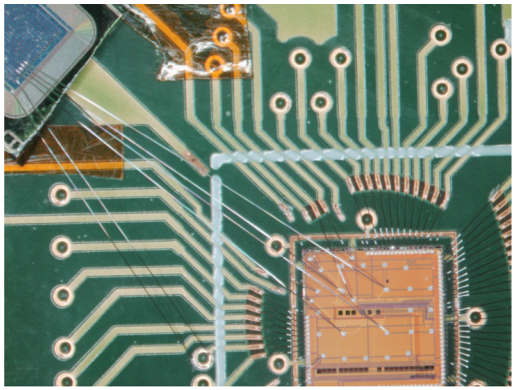
- **<u>Test-beam at FNAL with 120 GeV protons shows that AC-LGADs meet requirements</u>**
  - 30-35 ps time resolution
  - < 15 µm space resolution with strip sensor: 100 µm pitch, 20 µm gap
  - ~100% particle detection efficiency
  - See: https://indico.fnal.gov/event/46746/contributions/210254/attachments/141193/177718/Apresyan_4D-trackers.pdf



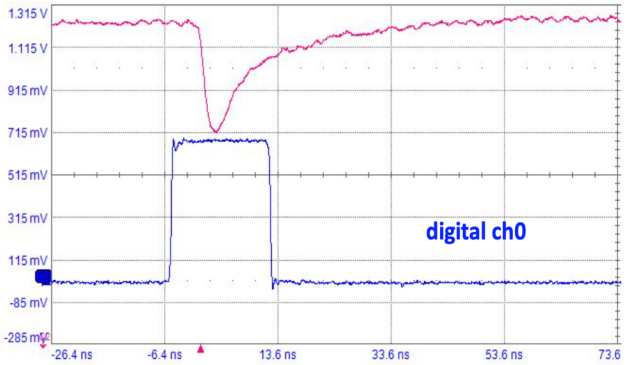
ASIC development

- Strategy to modify ASIC (ALTIROC, TSMC 130 nm) used in ATLAS timing detector (HGTD) and make it compatible to Roman Pot specs
  - Extensive discussions between electronics experts at IJCLab/OMEGA, and sensors and EIC machine experts
  - **Main modifications have been identified to reduce pixel pitch from 1.3 mm to 500 µm**
    - Low occupancy and triggerless EIC readout simplifies ASIC design, e.g. no need for SRAM
    - Starting point is same front-end concept (preamplifier, discriminator and two TDC for Time of Arrival and Time Over Threshold)
    - Replacing TDC with ADC and sampling pulses is under consideration to improve information of signal sharing
- ASIC power dissipation of a 32x32 channel ASIC
  - Per pixel power dissipation of 3 mW (assuming 10% occupancy - very conservative!, as expected occupancy <<01%)
    - **3.072 W per chip, including the peripheral electronics**
    - **1.067 W/cm^2 power density**
    - **total power dissipation in the whole detector of 1.573kW (Strawman layout)**
      - For comparison ALTIROC for HGTD: 1.2 W/chip (300 mW/cm2) and 19.3kW total power dissipation
  - Optimization: thanks to lower AC-LGAD capacitance, transistor size in the preamp can be reduced.
  - The design of a 4x4 channels prototype will start at OMEGA in spring 2021 with an expected submission end 2021 (funds secured for prototype run).
- On-going discussion with EIC accelerator experts:
  - 250 fs is estimate EIC clock jitter RMS.
  - Long term drift of the clock will need to be assessed, but can be compensated.

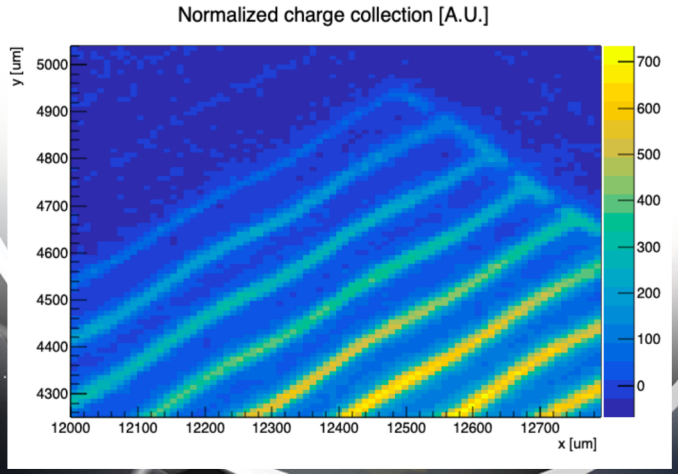
First Tests of AC-LGAD Compatibility with ALTIROC



- Assembly: ALTIROC0 v1 prototype (4 channels) + strip AC-LGAD with pitch 100 µm, and inter-strip gap of 20 µm.
- ALTIROC0 chip: analog readout after the preamplifier, 2 TDCs (Time-Of-Arrival and Time-Over-Threshold) and threshold discriminator. Time jitter smaller than 20 ps for input charge larger than 5 fC
  - ALTIROC1 + AC-LGAD already assembled for studying the Constant Fraction Discriminator. To be studied next period.



- Signal from beta-particles from 90Sr source.
- **Clear signal with negative and positive polarity.**
- Fast (~5 ns) signal compatible with published results for (DC-)LGAD sensors read-out via ALTIROC0 [JINST 15 P07007 (2020)]



- Laser Scan - Colors: integral charge of the signal peak from the ALTIROC analog output generated by IR laser on sensor.
- Results compatible with those with beta-particles ('waves' due to board vibrations - to be fixed).

These results show that the off-the-shelf ALTIROC can read the signals from the AC-LGAD! Modifications needed to optimize (in progress).

Costs

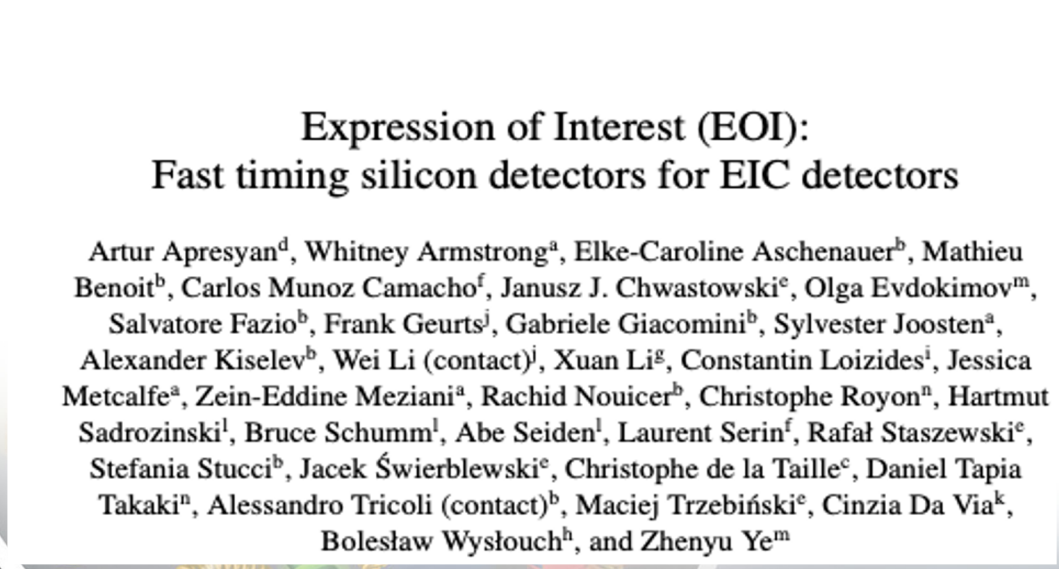
Item	Cost [k$]
Sensors	260
ASICs	280
Peripheral Electronic Boards (lpGBT, VTRX, DC-DC conv., PCB, connectors)	25
LV and HV systems	45
Cables (LV,HV,DCS), Electrical connectors	70
Fibers, Optical connectors	20
Module Assembly (incl. hybridisation, flexes, assembly)	90
Cooling system	70
Mechanics (on-det cooling plate, suport plate cooling, hermetic vessel)	30
TOT	**890**
TOT*1.33	**1,200**

The direct cost for the Roman Pots detector (excluding labor as well as R&D and pre-production cost) is estimated to be $1.2M, based on experience building the ATLAS timing detector.

The total cost includes a 1.33 factor that accounts for an underestimation of the Strawman detector layout cost, based on the experience of cost underestimation for the ATLAS timing detector in the LOI with respect to the TDR.

International LGAD Consortium

- We have also established a Consortium of 14 international institutes and 33 scientists with interests in the LGAD technology for EIC detectors.
  - See Expression of Interest on "Fast timing silicon detectors for EIC detectors", (https://indico.bnl.gov/event/8552/contributions/43183/attachments/31235/49294/EIC.EoI_LGAD_consortium.pdf)
- Two meetings have already taken place and future discussions on dedicated topics are planned in the coming weeks and months, see indico folder of the agendas https://indico.bnl.gov/category/323/



Expression of Interest (EOI):
Fast timing silicon detectors for EIC detectors

Artur Apresyan[d], Whitney Armstrong[a], Elke-Caroline Aschenauer[b], Mathieu Benoit[b], Carlos Munoz Camacho[f], Janusz J. Chwastowski[e], Olga Evdokimov[m], Salvatore Fazio[b], Frank Geurts[j], Gabriele Giacomini[b], Sylvester Joosten[a], Alexander Kiselev[b], Wei Li (contact)[j], Xuan Li[g], Constantin Loizides[i], Jessica Metcalfe[a], Zein-Eddine Meziani[a], Rachid Nouicer[b], Christophe Royon[n], Hartmut Sadrozinski[l], Bruce Schumm[l], Abe Seiden[l], Laurent Serin[f], Rafał Staszewski[e], Stefania Stucci[b], Jacek Świerblewski[e], Christophe de la Taille[c], Daniel Tapia Takaki[n], Alessandro Tricoli (contact)[b], Maciej Trzebiński[e], Cinzia Da Via[k], Bolesław Wysłouch[h], and Zhenyu Ye[m]

- Argonne National Lab (ANL)
- Brookhaven National Lab (BNL)
- Organisation de Micro-Électronique Générale Avancée (OMEGA), Ecole Polytechnique
- Fermi National Lab (FNAL)
- Institute of Nuclear Physics Polish Academy of Sciences (IFJ PAN)
- Laboratoire de Physique des 2 Infinis Irène Joliot Curie (IJCLAB)
- Los Alamos National Lab (LANL)
- Massachusetts Institute of Technology (MIT)
- Oak Ridge National Lab (ORNL)
- Rice University (Rice)
- Stonybrook University (Stonybrook)
- University of California, Santa Cruz (UCSC)
- University of Illinois, Chicago (UIC)
- University of Kansas (KU)

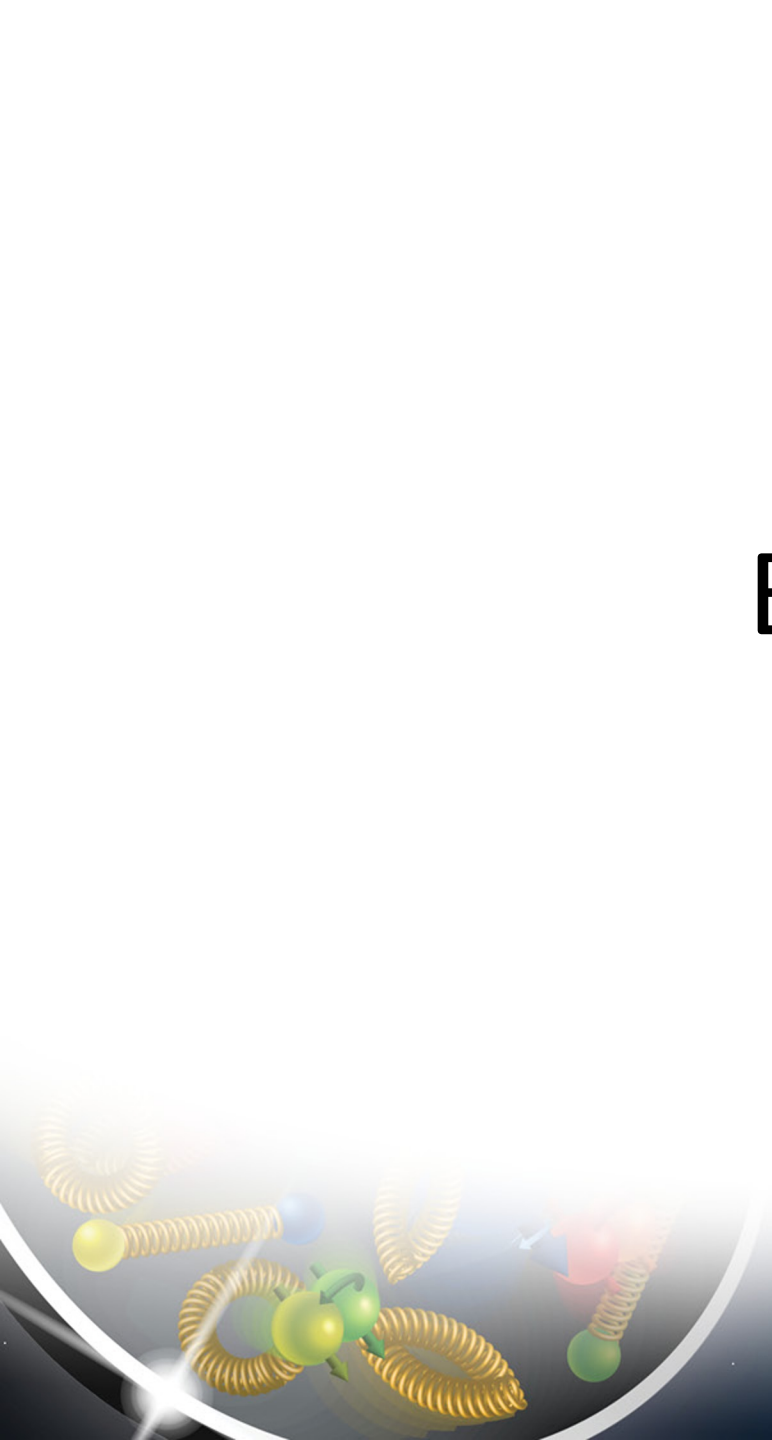
Specific plans for next period

- **Simulation Goals**
  - Implement new layout of sensors into GEANT simulations and assess impact.
  - Extend study to include the Off-Momentum Detectors. Acceptances are already understood from YR, but further study needed (e.g. layout, backgrounds, etc.).
- **Sensor development**
  - Analyze test beam data and continue lab tests to optimize fabrication parameters, comparison with TCAD simulations
  - Fabrication of sensors with varied doping of the resistive n-type layer to assess its impact on signal sharing
  - Implementation of large area prototype with design and layout towards the Roman Pots specifications (e.g. 500 µm pitch pixels, slim edges)
- **ASIC development**
  - Continue testing of ALTIROC + AC-LGAD to assess collection properties in greater detail, signal sharing between channels, dependence of time-over-threshold (TOT) on input signal charge.
  - Intensify the discussion EIC accelerator experts on clock jitter, transmission, etc.
  - Complete the redesign of the ALTIROC chip to meet the specifications of the Roman Pots of EIC (production expected beginning 2022)
  - Study alternative, low-power ASIC technologies, and perform market survey of SiGe technology. Radiation testing of SiGe technologies.

Summary

- **Simulation studies provide insight into both needed performance and expected challenges in implementation.**
  - Required layout, number of channels, backgrounds, timing, etc. implemented into GEANT simulations.
- **All of the requirements from the physics simulations are on-track to be met by the AC-LGAD.**
  - With COVID hopefully ramping down, a return to normal operations in the laboratory and further access to test-beams for full prototype implementation will drastically improve this workflow.
  - We are working towards building a large area sensors that meets all specs at the same time (time resolution, pixelation, edge size).
- **ASIC development ongoing, and initial tests of compatibility with AC-LGAD promising.**
  - Work towards a first RP-compatible ALTIROC prototype.
  - Further studies needed to minimize power dissipation.
  - Discussions with accelerator experts to assess impact of clock, etc. ongoing.
- **The LGAD Consortium for EIC will provide a framework to work collaboratively and share expertise for different detector applications**
  - e.g. we will benefit from expertise on cooling, mechanics, off-detector electronics.
- Expand effort to develop a more detailed detector architecture building from the Strawman layout.
- The 1st estimate of costs based on Strawman layout and ATLAS experience will become more accurate as designs becomes more detailed.

Back Up



ASIC development

- Strategy to modify ASIC (ALTIROC, CMS TSMC 130 nm) used in ATLAS timing detector (HGTD) and make it compatible to Roman Pot specs
  - Extensive discussions between electronics experts at IJCLab/OMEGA, and sensors and EIC machine experts
  - **Main modifications have been identified to reduce pixel pitch from 1.3 mm to 500 um**
    - Low occupancy and triggerless EIC readout simplifies ASIC design, e.g. no need for SRAM
    - Starting point is same front-and concept (preamplifier, discriminator and two TDC for Time of Arrival and Time Over Threshold)
    - Replacing TDC with ADC and sampling pulses is under consideration to improve information of signal sharing
- ASIC power dissipation of a 32x32 channel ASIC
  - Per pixel power dissipation of 3 mW (assuming 10% occupancy - very conservative!, as expected occupancy <<01%)
    - **3.072 W per chip, including the peripheral electronics**
    - **1.067 W/cm^2 power density**
    - **total power dissipation in the whole detector of 1.573kW (Strawman layout)**
      - For comparison ALTIROC for HGTD: 1.2 W/chip (300 mW/cm2) and 19.3kW total power dissipation
  - Optimization: thanks to lower AC-LGAD capacitance, transistor size in the preamp can be reduced.
  - The design of a 4x4 channels prototype will start at OMEGA in spring 2021 with an expected submission end 2021 (funds secured for prototype run).
- Parallel effort by UCSC team together with Anadyne Inc. to develop an ASIC with 500 um pitch and power (<500 µW) using SiGe bipolar technology for speed and low power.
- On-going discussion with EIC accelerator experts:
  - 250 fs is estimate EIC clock jitter RMS.
  - Long term drift of the clock will need to be assessed, but can be compensated.