EPIC TOF DAQ

with the higher pixel count in the endcaps

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Updates from previous (22 Jun 2022)

- Barrel – pixel size 0.5 mm x 10 mm (same as before)
  - area 102000 cm2 ⇒ 2 M channels (same)
- Endcap Smaller – pixel size 0.5 mm x 0.5 mm (vs 0.5 x 10 mm before)
  - area 13000 cm2 ⇒ 5.2 M channels (20x increase)
- Endcap Larger – pixel size 0.5 mm x 0.5 mm (vs 0.5 x 10 mm before)
  - area 23000 cm2 ⇒ 9.2 M channels (20x increase)
- Total channel increase: from 2.8 M to ***16.4 M***

Power estimates

- assuming 5 mW/channel (ALTIROC)
- Barrel: 10 kW
- Endcap S: 26 kW
- Endcap L: 46 kW
- BUT we also need to add
  - power for the FEE electronics (FPGA, clock chips, optical drivers, receivers, etc)
    - unknown and not small – depends on the readout topology thus the FEE count etc.
  - power for the AC-LGAD sensors themselves (probably low but unknown to me…?)

Fiber count estimates

- actual collision hit rate stays the same as Jun: 75 Mhits/second
  - and is assumed negligible compared to the noise per pixel (channel) of 1 kHz
- Barrel noise rates: 2M x 1 kHz ⇒ 2 Ghits/second
- Endcap noise rates: 14.4 M x 1 kHz ⇒ 14.4 Ghits/second
  - 5.2 for the smaller endcap, 9.2 for the larger endcap
- The 1st stage of the DAQ readout (detector-to-DAQPC) will be dominated by noise!
- so let's do the fiber count "backwards" assuming we can pipe 5 Gb/s per fiber
  - if 1 hit == 32 bits (assumption) ⇒ **1 fiber** can carry 125 Mhits/second but let's make it **100 Mhits/second** (with fudge factor)
- So:
  - barrel: 20 fibers **minimum**
  - endcap S: 52 fibers **minimum**
  - encap L: 92 fibers **minimum**
  - total: 164 (was 240 in June)
- but, minimum is not optimum and optimum can only be calculated once we have a better idea of the physical positioning of the FEEs but this depends on the mechanical design

DAQ 2nd stage

- 2nd stage DAQ is the path from the Receiver Board (in a DAQ PC in the DAQ Room) to the EPIC DAQ storage (“tape”)
  - this stays the ~same as before because the number of particles is the same and noise rejection is large and stays the same (or does it?)
- ~480 MB/s “to tape” is our current (and unchanged) canonical number

Summary

- Todo
  - we need to fix the pixel size(s) ASAP
    - which determines the channel count (*1st necessary number for electronics/DAQ*)
    - it is impossible to continue design if the channel count varies 20 times!
  - we need to have a noise measurement in “kHz per channel” ASAP
    - we expect to be noise limited so this is the 2nd most critical number for electronics/DAQ
  - we need to start discussing the physical layout of the barrel and endcaps
    - staves? panels? radial slices?
    - FEE count & size, fiber count, readout topology, power & cooling schemes ⇒ all depend on this but come mostly from the mechanical design