8/18/2022 EPIC DAQ WG Agenda

1. Discussion to clarify timing system design
2. Updated EPIC detector readout summary
    - Mini-updates from detector representatives
        - Far Forward & Far Backward
        - Si Tracking
        - MPGD Tracking
        - Calorimeters
        - PID-TOF
        - PID-Cherenkov
3. GD/I request for DAQ input to the FF/FB discussions next Monday
4. AOB

Timing System / Fiber Protocol Discussion

Requirements we have been discussing:

- General scheme for timing interface to Electrical/Optical boards will be home-grown FPGA based using COTS components
- Two versions:
  - Hi Res:
    - Dedicated clock fiber
    - Phase stability relative to EIC BX <5ps (Both while operating and between power cycles)
    - Jitter < ? (how is this impacted by phase requirements?)
  - Low Res:
    - Reconstructed clock from data in fiber
    - Phase stability < 100ps?
    - Jitter < ?
  - Both systems
    - Accept information protocol (ie. sPHENIX, or jlab) for busy/trigger/bunch identification/bunch characteristics. ~100 bits / BX.
    - Handle flow control commands
    - Handle configuration (JTAG & i2c)
    - >10Gb/s per fiber (Discussed 40Gb/s…)
    - We will **NOT** require that the ASIC/FEE use a BX derived clock for digitization
      - We will specify headers for the data packets, but are agnostic regarding internal data packets format
      - The data packets must provide sufficient information to reconstruct times relative the BX. Do we need to specify in the header some kind of scheme for tracking the relative phases & frequencies or leave that to specific detectors?

Timing System / Fiber Protocol Discussion

Issues to clarify:

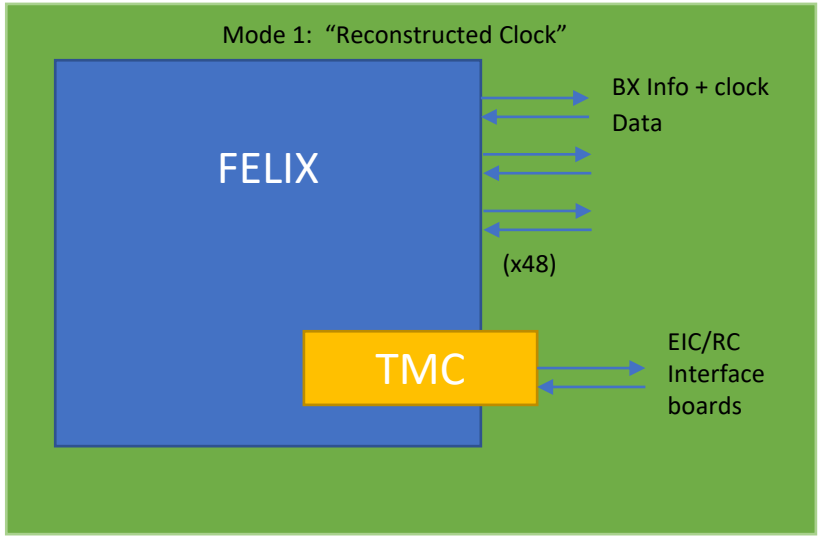
1. EIC timing system → DAM boards: Are the following assumptions correct?

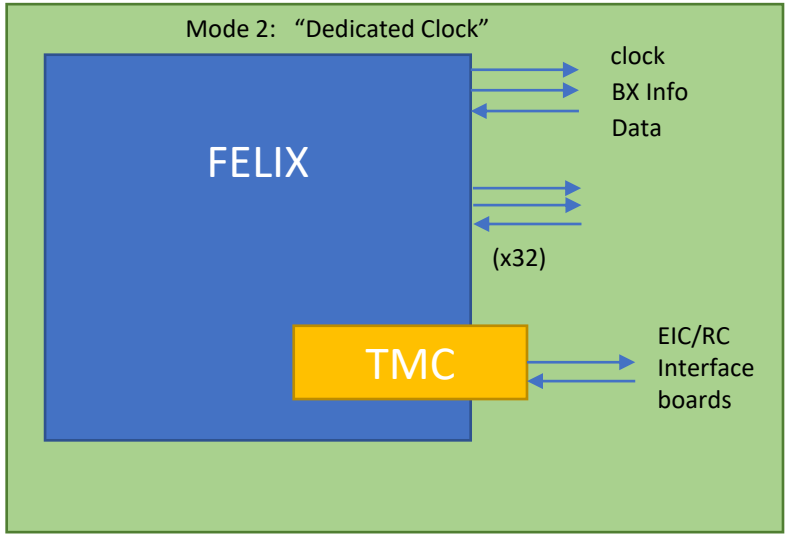
    - Interface to as yet unspecified EIC system
    - Interface to DAQ Control in quasi-real time O(seconds)
        - Run control
        - Sensing of issues, single bit upsets, need to manage flow control, recovery etc…
    - Tree of boards splitting EIC BX to O(100) DAM boards
        - I assume location is DAQ room, and multiple technologies exist including copper so that the <5ps phase is not problematic

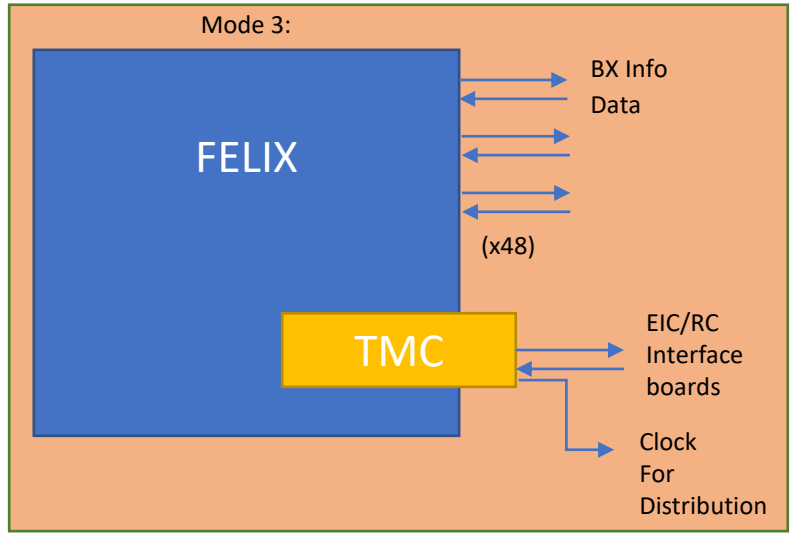
2. How should we be specifying requirements for the phase? It seems that the detectors are happy with 10-20ps resolution however I/we have been lax about distinguishing between resolution between specific components and full system resolution.

Timing System / Fiber Protocol Discussion

I'm trying to map my understanding of the FELIX features to our discussions of the Timing protocol:



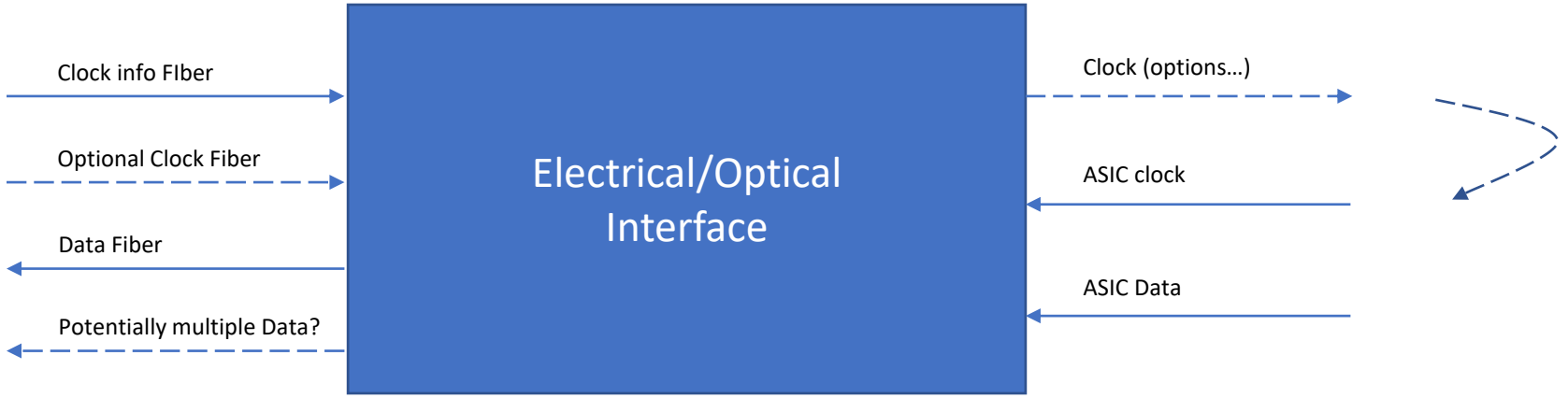




3. FELIX board TMC (Timing Mezzanine Cards) features:
    1. In general, is the expectation that the TMC has a separate fiber to the detector interface boards or use one of the 48 link pairs, or some combination?
    2. When we discuss using a dedicated clock fiber, does the answer change?
    3. Specific FELIX features:
        1. Provides reference clocks for fiber transceivers (This is TMC → DAM, correct?)
        2. DAM sends busy info to timing system… But I'm not clear on what this means. Is this DAM → TMC card, or DAM → Fiber to detectors, or both?
        3. Handling of the timing system info bits. Is this TMC card → DAM → fiber

Timing System / Fiber Protocol Discussion

4. Requirements for Electrical Optical Interface assuming FEE/ASIC clock is independent of BX clock, so



If the clocks are fully independent we'd need to measure phase, drift etc. Can we confidently leave this to FEE designers or do we need to specify, and if so how?

EPIC Detector Scale and Technology Summary:

Detector System	Channels	Fiber pair	Data Volume	DAM Boards	Readout Technology	Notes
Si Tracking: 3 vertex layers, 3 sagitta layers, 4 backward disks, 5 forward disks	7 m^2 32B pixels 5,200 MAPS sensors	300	5Gb/sec	6-8	MAPS: Several flavors: curved its-3 sensors for vertex Its-2 staves / w its-3 improvements	
MPGD tracking: 3 layers	100k	200	<10Gb/sec	4-5	64 channel SALSA ASIC	Assume 512 Channel (8 ASIC)/FEE
Calorimeters: Forward: LFHCAL pECAL HCAL inset Barrel: HCAL ECAL Imaging Backward: ECAL	 60k 25k 8k 3k (25k?) 8k 50M pixels 25k	 950 400 125 50(400) 125 (note) 400 2050(2400)	15Gb/sec	50	SiPM using HGCROC &/or FPGA bases boards with FLASH ADC	For imaging, if present: “2 level data aggregation inside detector, 1 data link per stave” ?staves?
Far Forward: B0: 3 MAPS layers 1 or 2 AC-LGAD layer 2 Roman Pots 2 Off Momentum ZDC: Crystal Calorimeter 32 Silicon pad layer 4 silicon pixel layers 2 boxes scintillator	 3x20cmx20cm (300M pixel) 300k or 600k 1M (4 x 135k layers each) 650k (4 x 80k layers each) 400 11520 160k 72	 6 30 64 42 10 10 10 2	1Gb/sec	5	 MAPS AC-LGAG / EICROC AC-LGAD / EICROC AC-LGAD / EICROC APD HGCROC as per ALICE FoCal-E	 600^cm layers (1 or 2 layers) 13 x 26cm layers 9.6 x 22.4cm layers There are alternatives for AC-LGAD using MAPS and low channel count DC-LGAD timing layers
Far Backward: Low Q Tagger 1 Low Q Tagger 2 2 Calorimeters	 1.3M 480k 700	 80 32 1	100Gb/sec (1 Gb/sec to tape)	4	 AC-LGAD / EICROC AC-LGAD / EICROC SiPM? PMT? MCPMT?	 40cmx40cmx500um 30cmx20cmx500um
PID-TOF	3M-50M	240-500	6Gb/sec	6-12	EICROC / AC-LGAD	Channel / Fiber counts depend on sensor geometry. Considering pitches of: .5mm x 1cm, .5mm x .3cm, .5mm x .5mm
PID-Cherenkov: dRICH pfRICH (if selected) mRICH (if selected) DIRC	 300k 225k ??? 74k	 200 150 288 288	 1830Gb/s (<20Gbps to tape) 1380Gb/s (<15Gb/s to tape) ??? 11Gb/sec	 20 14 5 6	 SiPM / ALCOR SiPM / ALCOR HDSoC64	 Worse case after radiation. Includes 30% timing window. Requires further data volume reduction (software trigger, or AI/ML) 12 boxes x 24 sensor x 4 asic x 64 ch

Summary of Channel Counts

Detector Group	Channels				Fibers	DAM	Data Volume Estimate (Gb/s)	Data Volume To Tape (Gb/s)
	MAPS	AC/DC-LGAD	SiPM/PMT	MPGD				
Tracking	32B			100k	500	335013	15	15
Calorimeters	50M		150k		2050	50	15	15
Far Forward	300M	2.3M	500		174	5	1	1
Far Backward		1.8M	700		113	4	100	2
PID		3M-50M	600k		638	40	3220	45
TOTAL	32B	7.1M-54M	750k	100k	3475	112	3350	78

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