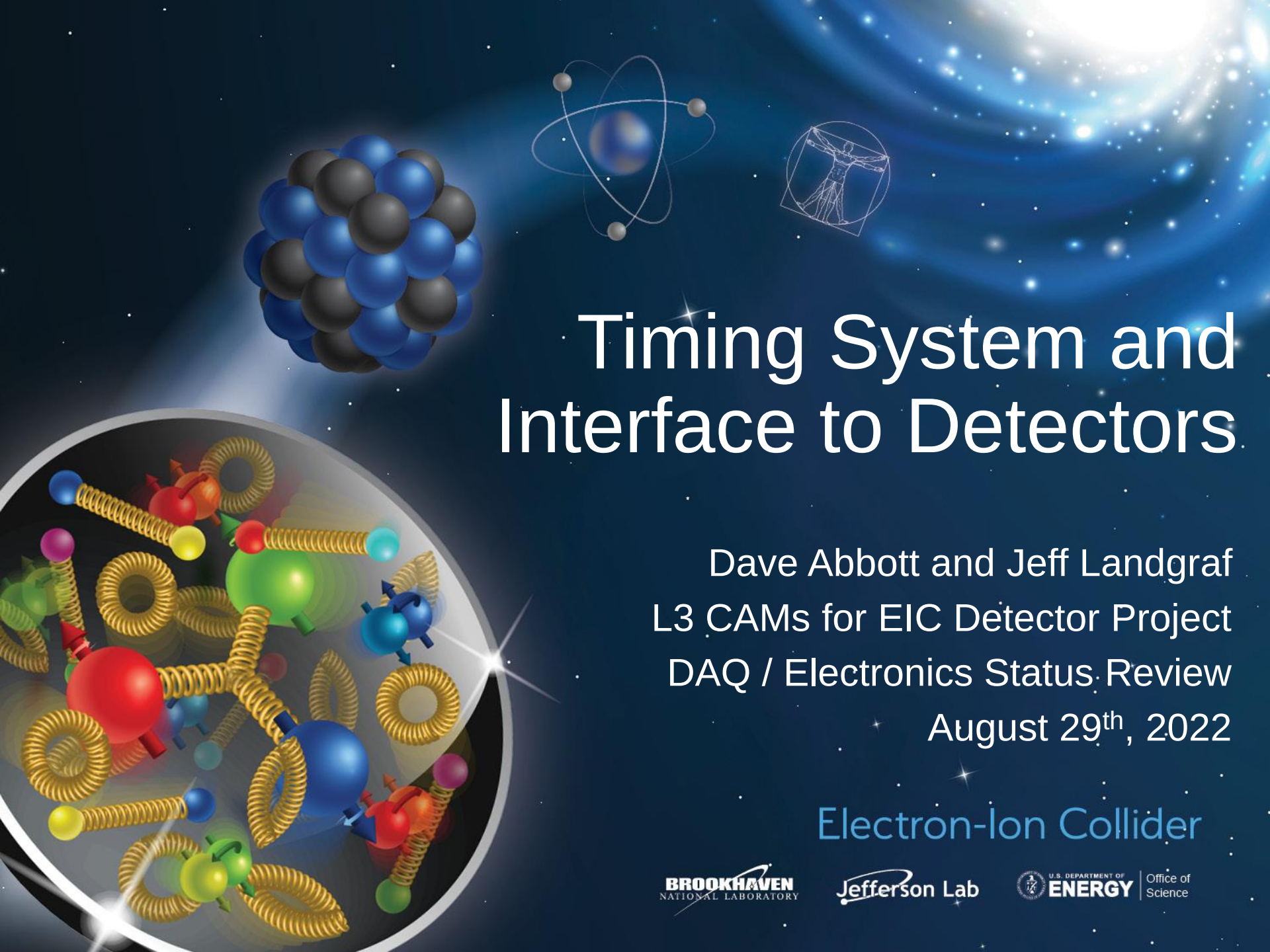


Timing System and Interface to Detectors

Dave Abbott and Jeff Landgraf

L3 CAMs for EIC Detector Project

DAQ / Electronics Status Review

August 29th, 2022

Electron-Ion Collider

BROOKHAVEN NATIONAL LABORATORY

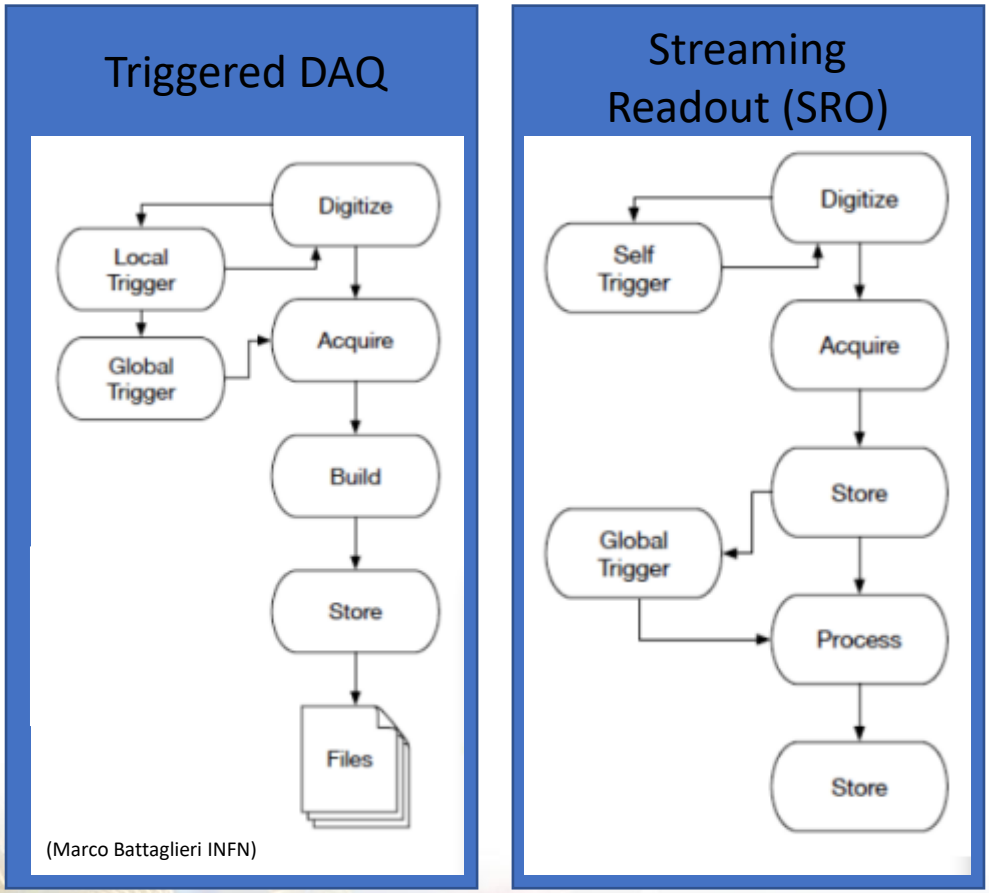
Jefferson Lab

U.S. DEPARTMENT OF ENERGY | Office of Science

Organization of this presentation

- Overview of DAQ
- Detector Interfaces
- Timing System
- Safety Review Process

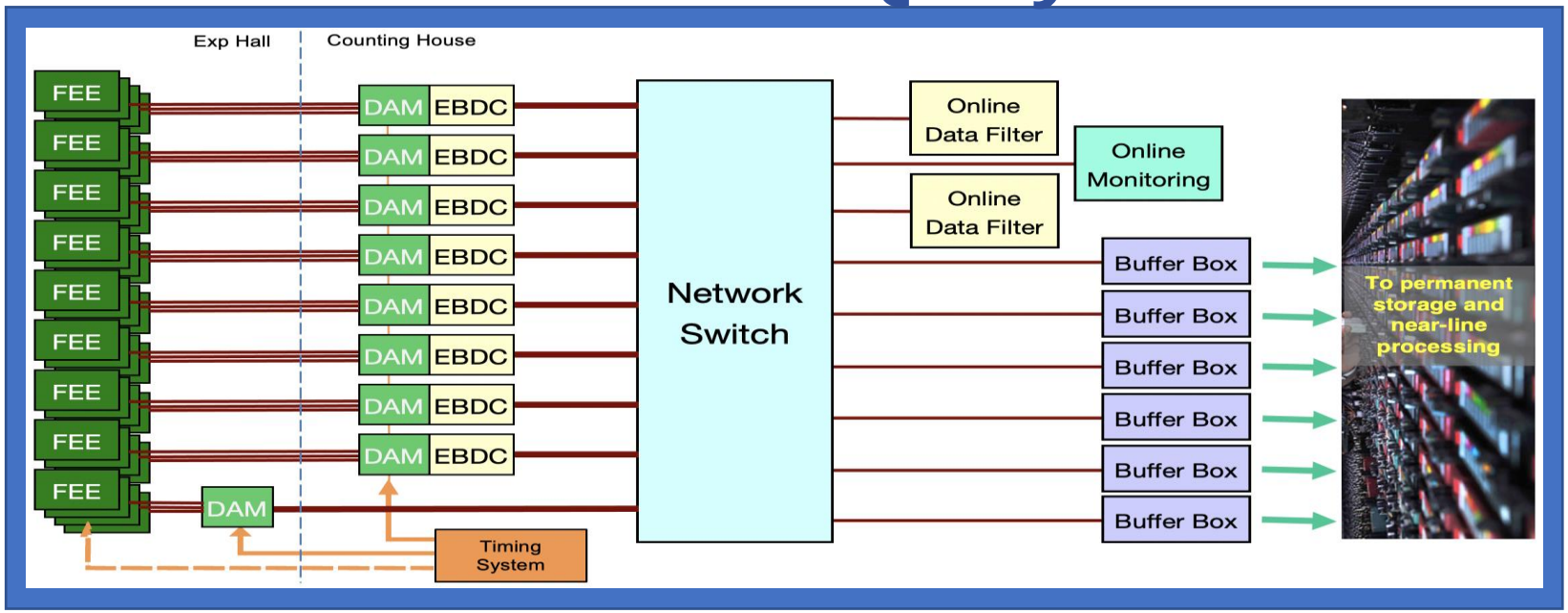
ePIC Streaming Readout



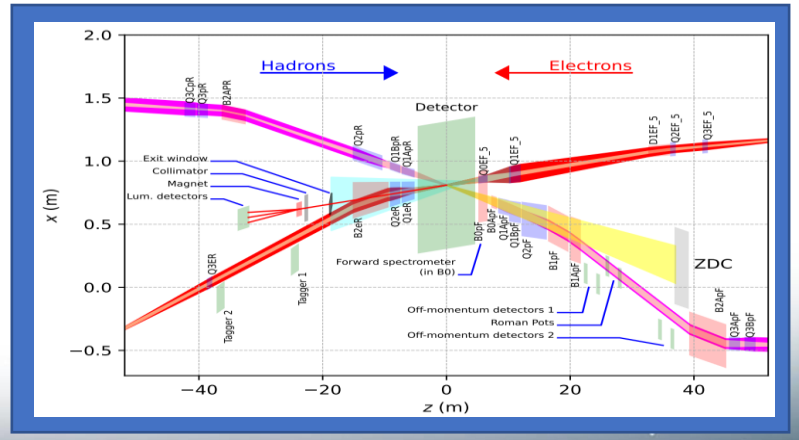
Features of ePIC SRO

- No global trigger
  - No global trigger electronics
  - Zero-suppress early (ASICs)
- Hits identified by time stamp rather than by event
- Flexibility in event selection
  - Can be performed in CPU, FPGA, or GPU
  - Can be performed with all channels available
  - Can be performed at different times, using different methods, for different purposes
- Cons
  - SRO has greater sensitivity to noise and background

Overview of the DAQ System



- Triggerless, streaming DAQ
  - Large Channel counts / Low Occupancy (<15KB / interaction)
  - Multiple Technologies
  - Bunch Crossing Rate of 100MHz
  - Interaction rates up to 500KHz
  - Large physical extents (+/- 40m)



Scale and main challenges

Detector Group	Channels				Fibers	DAM	Data Volume Estimate (Gb/s)	Data Volume To Tape (Gb/s)
	MAPS	AC/DC-LGAD	SiPM/PMT	MPGD				
Tracking	32B			100k	500	13	15	15
Calorimeters	50M		150k		2050	50	15	15
Far Forward	300M	2.3M	500		174	5	1	1
Far Backward		1.8M	700		113	4	100	2
PID		3M-50M	600k		638	40	3220	45
TOTAL	32B	7.1M-54M	750k	100k	3475	112	3350	78

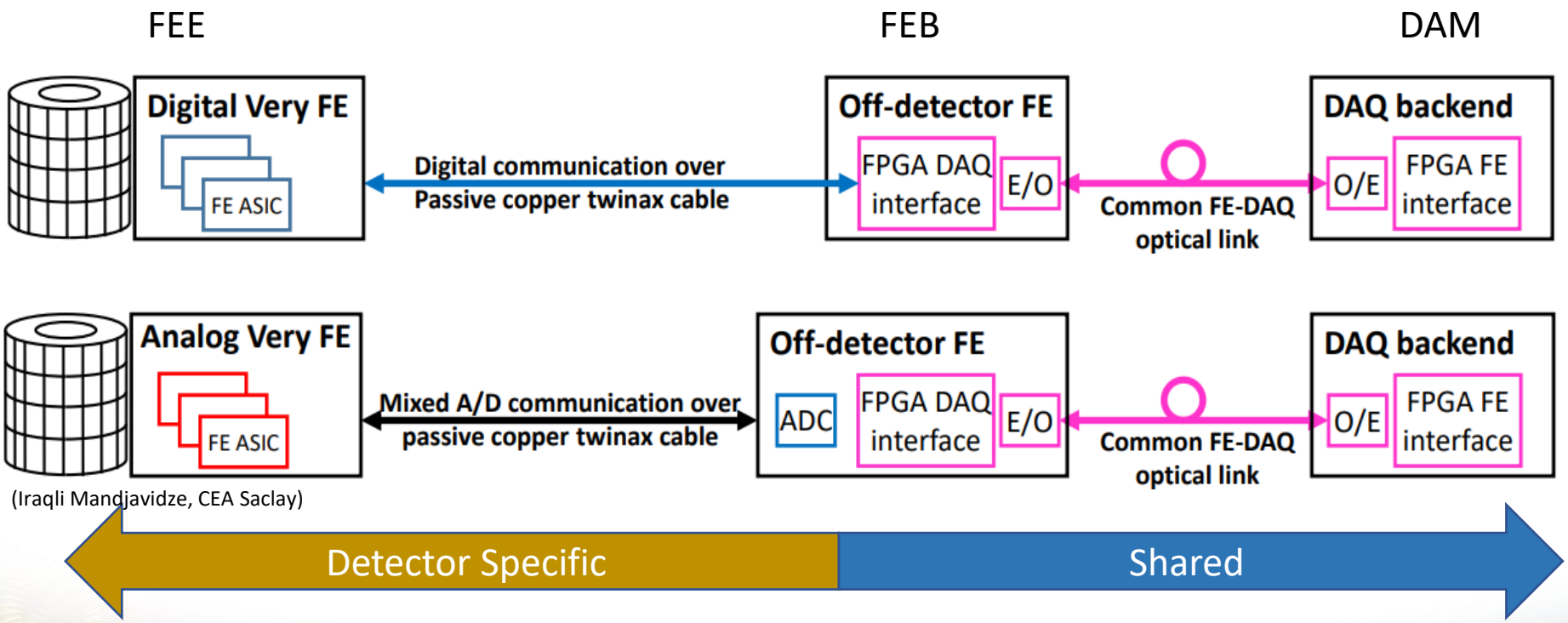
- Function of DAQ is to reduce ~1M channels @100MHz → 100Gb/sec
- The primary strategy is aggressive zero suppression, which is an important requirement for all detector readouts (FEE/FEBs)
- Other secondary strategies include
  - Feature extraction (cluster finding, tracking etc)
  - Noise identification and removal
  - Algorithmic data compression
  - AI/ML to be evaluated for each of the above
  - Software triggering

Full Detector Summary

Detector System	Channels	Fiber pair	Data Volume	DAM Boards	Readout Technology	Notes
Si Tracking: 3 vertex layers, 3 sagitta layers, 4 backward disks, 5 forward disks	7 m^2 32B pixels 5,200 MAPS sensors	300	5Gb/sec	6-8	MAPS: Several flavors: curved its-3 sensors for vertex Its-2 staves / w its-3 improvements	
MPGD tracking: 3 layers	100k	200	<10Gb/sec	4-5	64 channel SALSA ASIC	Assume 512 Channel (8 ASIC)/FEE
Calorimeters: Forward: LFHCAL pECAL HCAL inset Barrel: HCAL ECAL Imaging Backward: ECAL	 60k 25k 8k 3k (25k?) 8k 50M pixels 25k	 950 400 125 50(400) 125 (note) 400 2050(2400)	15Gb/sec	50	SiPM using HGCROC &/or FPGA bases boards with FLASH ADC	
Far Forward: B0: 3 MAPS layers 1 or 2 AC-LGAD layer 2 Roman Pots 2 Off Momentum ZDC: Crystal Calorimeter 32 Silicon pad layer 4 silicon pixel layers 2 boxes scintillator	 3x20cmx20cm (300M pixel) 300k or 600k 1M (4 x 135k layers each) 650k (4 x 80k layers each) 400 11520 160k 72	 6 30 64 42 10 10 10 2	<1Gb/sec	5	MAPS AC-LGAG / EICROC AC-LGAD / EICROC AC-LGAD / EICROC APD HGCROC as per ALICE FoCal-E	 600^cm layers (1 or 2 layers) 13 x 26cm layers 9.6 x 22.4cm layers There are alternatives for AC-LGAD using MAPS and low channel count DC-LGAD timing layers
Far Backward: Low Q Tagger 1 Low Q Tagger 2 2 Calorimeters (Up/Down) Photon Detector	 1.3M 480k 700	 80 32	100Gb/sec (<1 Gb/sec to tape)	4	AC-LGAD / EICROC AC-LGAD / EICROC PMT / SiPM	40cmx40cmx500um 30cmx20cmx500um Possible tracking layers
PID-TOF	3M-50M	240-500	6Gb/sec	6-12	EICROC / AC-LGAD	Channel / Fiber counts depend on sensor geometry. Considering pitches of: .5mm x 1cm, .5mm x .3cm, .5mm x .5mm
PID-Cherenkov: dRICH pfRICH (if selected) mRICH (if selected) DIRC	 300k 225k 74k	 200 150 288 288	 1830Gb/s (<20Gbps to tape) 1380Gb/s (<15Gb/s to tape) 11Gb/sec	 20 14 5 6	 SiPM / ALCOR SiPM / ALCOR HDSoC64	 Worse case after radiation. Includes 30% timing window. Requires further data volume reduction (software trigger, or AI/ML) 12 boxes x 24 sensor x 4 asic x 64 ch

Detector Interface Organization

Typical organizations for the ePIC detector readouts



Currently working on the question: What form should the shared portions of the Electrical/Optical Interface take?

Shared Electrical/Optical Interface

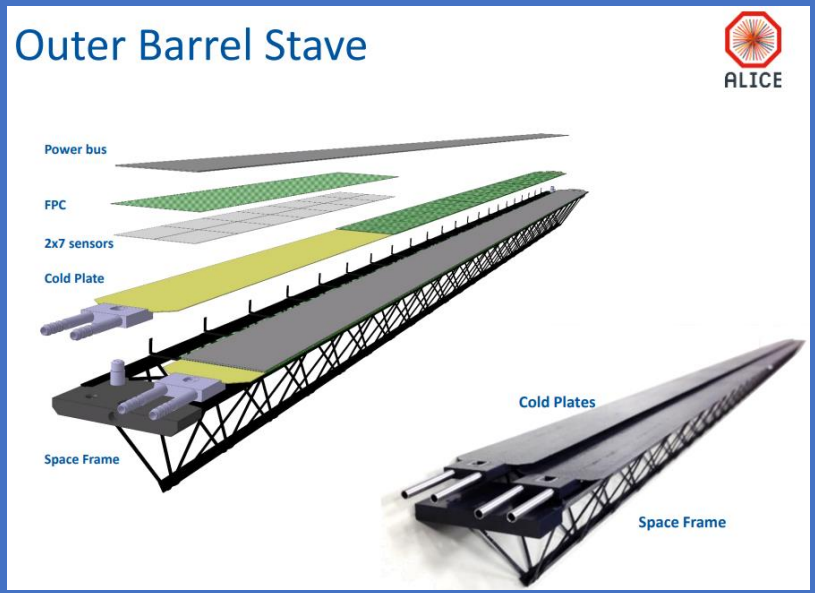
- Organization of this is not fully defined but high priority!
  - This interface carries critical aspects of the DAQ
    - Portions of the timing system
    - The data transfer path
    - The configuration of the FEEs
  - Will be need to be established before detector readout design can finish
  - Planned to be the subject of a meeting under the auspices of the Streaming Workshop for November or December 2022
- There are some requirements that are established
  - ~>10 Gbit/sec transfer speeds per data fiber
  - Needs I^2C for communication and configuration
  - JTAG for loading FPGA code
  - If digitizing ASIC does not use EIC BX clock for operation, the FEB must provide all constants to report hit times in reference to the BX clock
  - Needs to support the timing protocol and adhere to the timing protocols flow control commands.
  - Need to be able to sense and disable channels firing at abnormal rates do to single bit upsets or other hardware failures.

Detector Interface Example: (MAPS)

Many Geometries

- Tracking
  - Forward/Backward Disks
  - Vertex
  - Sagitta
- Far Forward
  - B0
- Imaging Calorimeter
  - Astropix

Stave Example

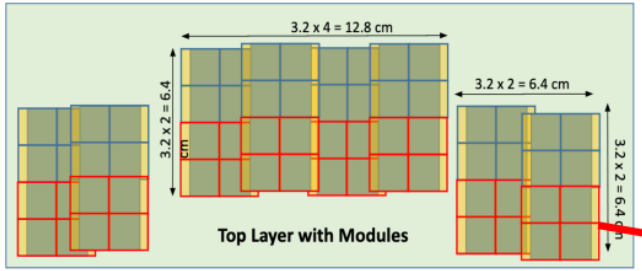


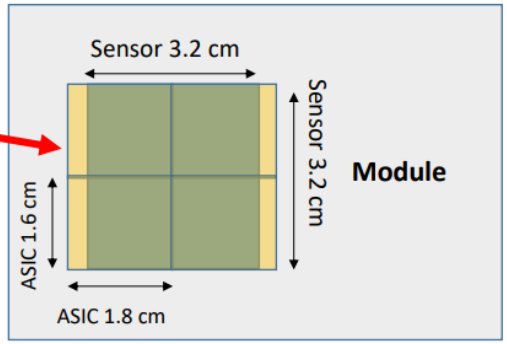
Detector Interface Example: (AC-LGAD)

Detectors

- Far Forward
  - Roman Pots
  - Off Momentum
  - B0
- Far Backward
  - Low Q Taggers
- TOF

- Updated strawman layout with current design for LGAD sensor + ASIC.

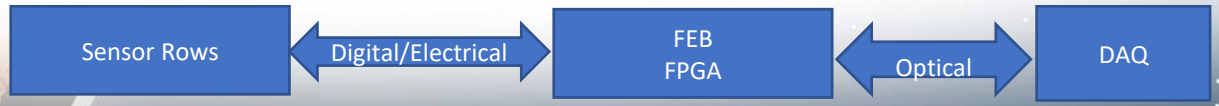




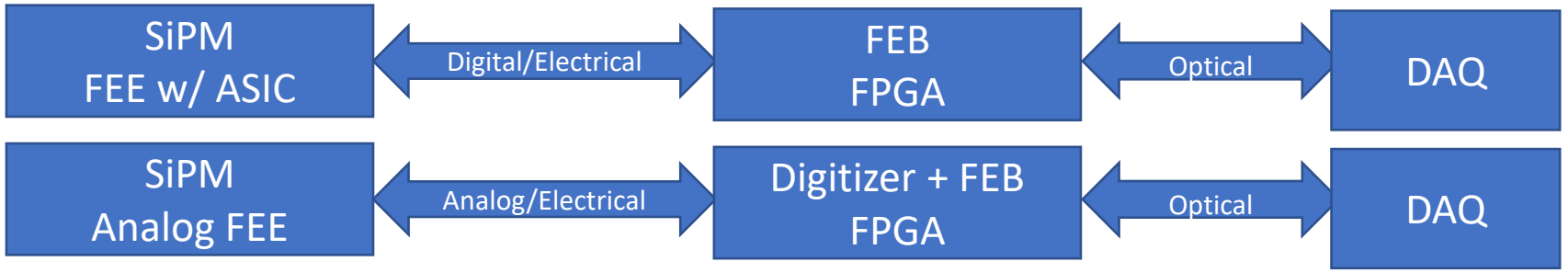
- As further developments are made, more of the realistic considerations can be included in the simulations as we move toward a TDR design.

ASIC size	ASIC Pixel pitch	# Ch. per ASIC	# ASICs per module	Sensor area	# Mod. per layer	Total # ASICs	Total # Ch.	Total Si Area
1.6x1.8 cm^2	500 μm	32x32	4	3.2x3.2 cm^2	32	512	524,288	1,311 cm^2

Expect to aggregate each sensor row onto a FEB board

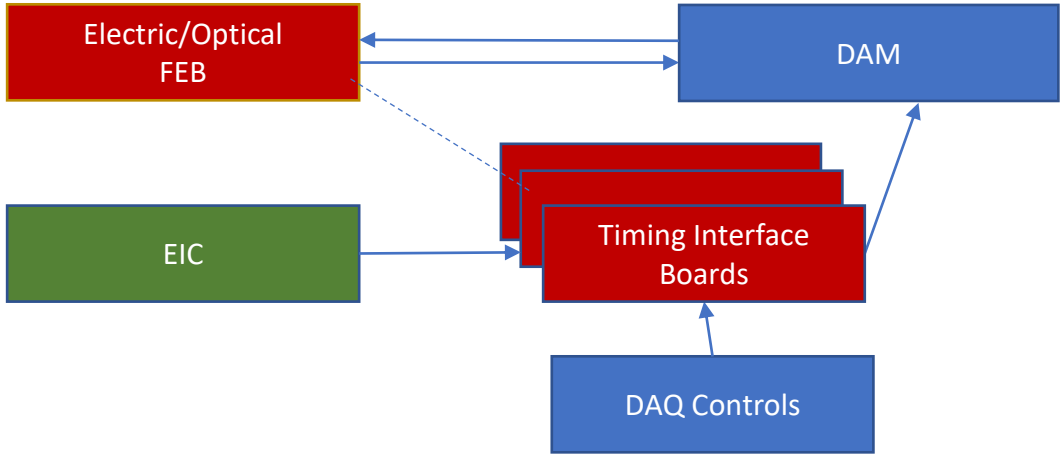


Detector Interfaces (SiPM)



- Calorimeter Possibilities
  - ASIC based FEE using HGCROC
  - Analog/FEE + Digitizer&FEB
  - Analog/FEE + Digitizer + (aggregated to) FEB
  - High Threshold so zero-suppression + aggregation are biggest issues
- dRICH (pfRICH)
  - ASIC based FEE using ALCOR
  - Low threshold so high noise due to dark currents
    - 300Hz/mm^2 increasing to 270KHz/mm^2 with several years radiation damage before annealing

Timing System Connectivity



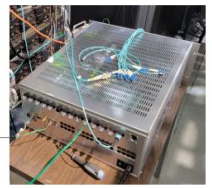
- The baseline plan is for the FEB to use a reconstructed clock based upon the info fiber transmitted to the FEB
- There are reports of O(1ps) phase stability using the reconstructed clock, even after power cycling. There are caveats though. They used specific features of the Xilinx Ultrascale FPGA family and also ran using specific clock frequencies.
  - Reserve the possibility to distribute a dedicated clock from the timing interface boards to detectors requiring 20ps phase stability
- Where possible, the ASICs/digitizing chips should use a BX derived clock. In cases where that is not possible the FEB boards must provide sufficient information (drift measurements, phase differences, frequency differences) to allow time reporting in reference to the BX clock.

Timing System Functions

- Timing System must synchronize data between detectors. This requires a 10ns resolution
  - 40m forward and backward ~135ns delays to calibrate
  - Need procedures to set delays and to monitor the synchronization
  - Absolutely critical to get this right if there is any sort of software trigger or filtering of data on one detector relative using information from another.
- Timing System must provide high resolution 20ps phase stability to actual bunch crossing persisting over power cycles
  - 20ps phase stability to EIC clock
  - Account for transitive loading due to EIC acceleration (species/energy dependent phase correction)
  - Ability to set fine delays and monitor the synchronization
  - Implies higher resolution O(1ps) required between components
- Timing system is the only source for real-time global information
  - Revtic (to identify bunch number)
  - 64 bit bunch crossing identifier
  - Bunch structure
  - Spin State
  - Control zero-suppression, feature finding, AI/ML algorithms
  - Flow Control (start / stop / implement common busy)
  - Define time frames for packetization of detector data
  - Fallback for handling hardware trigger for debugging, commissioning and/or handling specific detector problems (dRICH?)

Protocols

- Timing System Protocol
  - Expect about 100bits / BX
    - 10Gb/s into 100MHz
  - 64 Bits BX
  - ~30bits
    - Defined flow control
    - System control
    - Detector needs
    - Trigger signals
- Data protocol
  - DAQ defined header for time windows
  - Internal data format agnostic



Timing System

Pick a convenient multiple of the beam clock frequency

Have a global, never-reverting master BCO counter – 64 bit, transmit BCO LSBs to front-ends (40 bits)

Front-ends embed a number of those bits in their lower-level data structures (Felix - 40, FEE - 20)

The **only way** to send information to the FEE on a per-crossing basis (like, have the FEE do something different in the abort gap)

Bit Number	Function	Beam clock phases					
		0	1	2	3	4	5
7-0	Mode bits /BCO	Modebits bits 7-0	BCO bits 7-0	BCO bits 15-8	BCO bits 23-16	BCO bits 31-24	BCO bits 39-32
8	Beam clock phase0	1	0	0	0	0	0
9	LVL1 accept	X	0	0	0	0	0
10	Endat 0	X	X	X	X	X	X
11	Endat 1	X	X	X	X	X	X
12	Modebit enable	1	0	0	0	0	0
15-13	User bits	3 user bits	0	1	2	3	4

10

Example: sPHENIX Timing System

Timing System Components

- EIC Clock System
- Timing Interface boards
  - Tree of boards
  - Reads info from EIC
  - Reads info from DAQ Controls
  - Writes info to DAM Boards
  - Needs feedback from DAM boards, most likely in the form of ethernet connections between readout computers and DAQ Controls computers, so is not a real-time feedback. Sufficient for overall-scale “flow control” but not for a traditional “busy”
- DAM Boards
  - Accept and transmit timing information stream
  - Use timing input clock to use as clock for fiber transceivers
  - Clock to FEB boards reconstructed from information stream on transmitting fiber
    - Reported 1ps phase stability, with caveats (Xilinx Ultrascale FPGA family, transceiver clock frequency, etc…)
    - Reserve the potential to supply separate fiber clock to be distributed to selected detector FEBs from Timing Interface Boards
  - Transmit fiber must also be able to pass configuration information (JTAG/i2c) in separate modes
- FEBs
  - Accept timing protocol
  - Format Data packets in appropriate time frames

Triggering and the Streaming DAQ

- Hardware Trigger (as fallback)
  - Support must be present in timing system
  - Hardware trigger is not part of baseline
  - Support will be simple
    - Provide electrical inputs in timing board to input trigger
    - Link these inputs to bits in the trigger information passed each BX
    - No / rudimentary support for prescale, busy, trigger counters, etc…
    - Expect trigger signal lag due to flight time and processing O(usec) so hardware support must be driven by detector needs / design
    - Potential mixed trigger (hardware selection but filtering implemented in DAM)
- Software Trigger
  - Reduce Data volume for RICH detectors (fallback from AI/ML)
    - SiPM sensitive to single photons
    - 1830Gb/sec from dRICH
      - Assuming zero-suppression
      - 1/3 data reduction by applying time window with respect to the BX
  - Reduce data volume for Far Backwards Detectors
    - Electron Bremsstrahlung leads to up to 20 tracks per bunch crossing in Far Backward detectors
    - ~100Gb/sec
      - Data to be analyzed by front end computers to produce luminosity measurements
      - Small fraction to be read out in concert with central detector activity

ESH Safety Requirements at BNL

- Detector systems are subject to a BNL experiment safety review process to ensure that safety rules and standards are followed and that hazards are properly mitigated
  - The experimental details and hazards are submitted to the ESH Coordinator
  - An ESR form must be submitted to the C-A department
  - The local representative must give a formal presentation to an ESH committee
  - Before operations, the equipment must be inspected by the review committee and approved for operation

Summary

- ePIC will implement a triggerless streaming readout system
- The interface between the detectors and the DAQ will use an optical protocol featuring fiber pairs running between the FEB connecting to the detector FEEs and DAM boards connected to the COTS computing
- The timing system needs to deliver 20ps phase stable system wide time resolution.
- The data transfer fiber will be capable of ~>10Gb/sec per fiber
- The transfer fiber will carry both timing and configuration information to the FEBs
- The timing system needs to deliver 20ps phase stable system wide time resolution.