EIC Electronics Requirements

Fernando Barbosa (TJNAF), L3 CAM Electronics

Electronics/DAQ Status Review

August 29, 2022

Electron-Ion Collider

BROOKHAVEN NATIONAL LABORATORY

Jefferson Lab

U.S. DEPARTMENT OF ENERGY | Office of Science

Outline

- Requirements and Design Philosophy
- EIC Streaming Readout
- Channels
- Specifications
- ASICs
- eRD109
- EIC Electronics Needs
- Infrastructure and Standards
- EHS&Q
- Timeline
- Summary

Requirements and Design Philosophy

- Maximize synergies in electronics:
  - Use same designs and architectures across sub-detectors, as much as possible. A number of variants are to be expected.
  - Minimize number of distinct devices: fewer part #s, less maintenance.
  - Design re-use from proven implementations, including ASIC IP blocks.

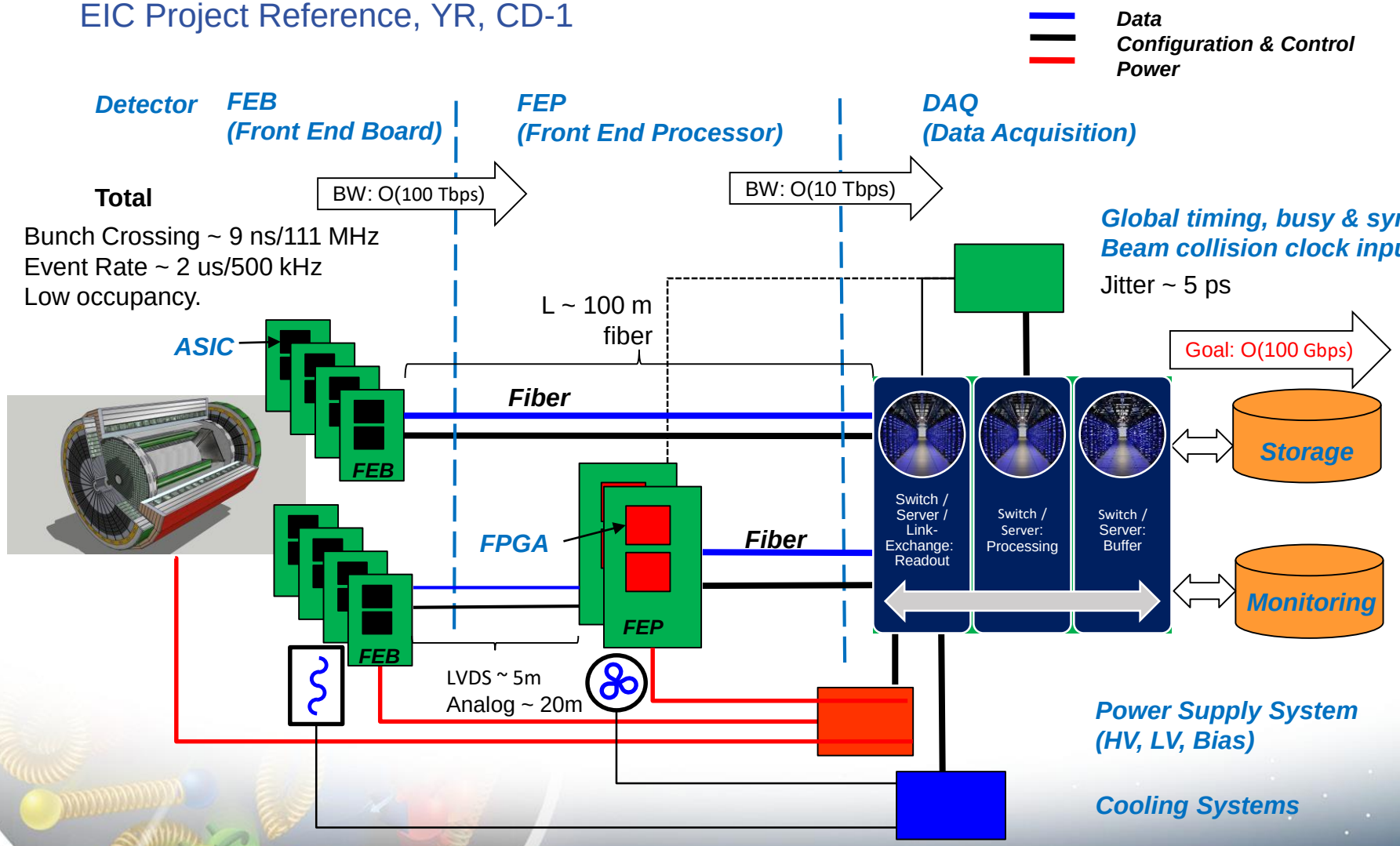
- Minimize cabling:
  - Fibers feature predominantly in our approach to signal/data transport but copper-based interfaces will still be used extensively.

- Electronics, including digitizers, close to the detector as much as possible and where applicable.
- Limit FPGA use inside detector volume.
- Serviceability as a design criteria.
- Triggerless operation of the electronics as default; triggered operation for calibration, test, de-bugging.
- Meet current US standards per NEC, UL, FCC, NEMA:
  - There are equivalency agreements for various norms.

- Equipment assessment reviews for conformance to EHS&Q.

Streaming Readout Architecture

EIC Project Reference, YR, CD-1



w/ Jin and Kai

EIC Streaming Readout Partitioning

- **FEB – Front-End Boards**
  - Custom designed for each detector and populated with ASICs, large magnetic fields.
  - ASICs designed to process analog signals and digitization tailored to each type of detector technology. Data reduction (e.g. zero suppression) is desirable.
  - Simplification of testing and calibration operations with triggered-mode configuration.
  - Data transport via optical fibers to minimize cabling is preferred.
  - Minimize use of FPGAs.

- **FEP – Front-End Processors**
  - Custom designed to process and aggregate data streams from multiple FEBs.
  - Functions may be addressed by DAM, Link Exchange or similar boards.
  - FPGAs are dominant components on these PCBs.
  - Algorithms reduce data flow (e.g., zero suppression)
  - Data transport via optical fibers to minimize cabling.

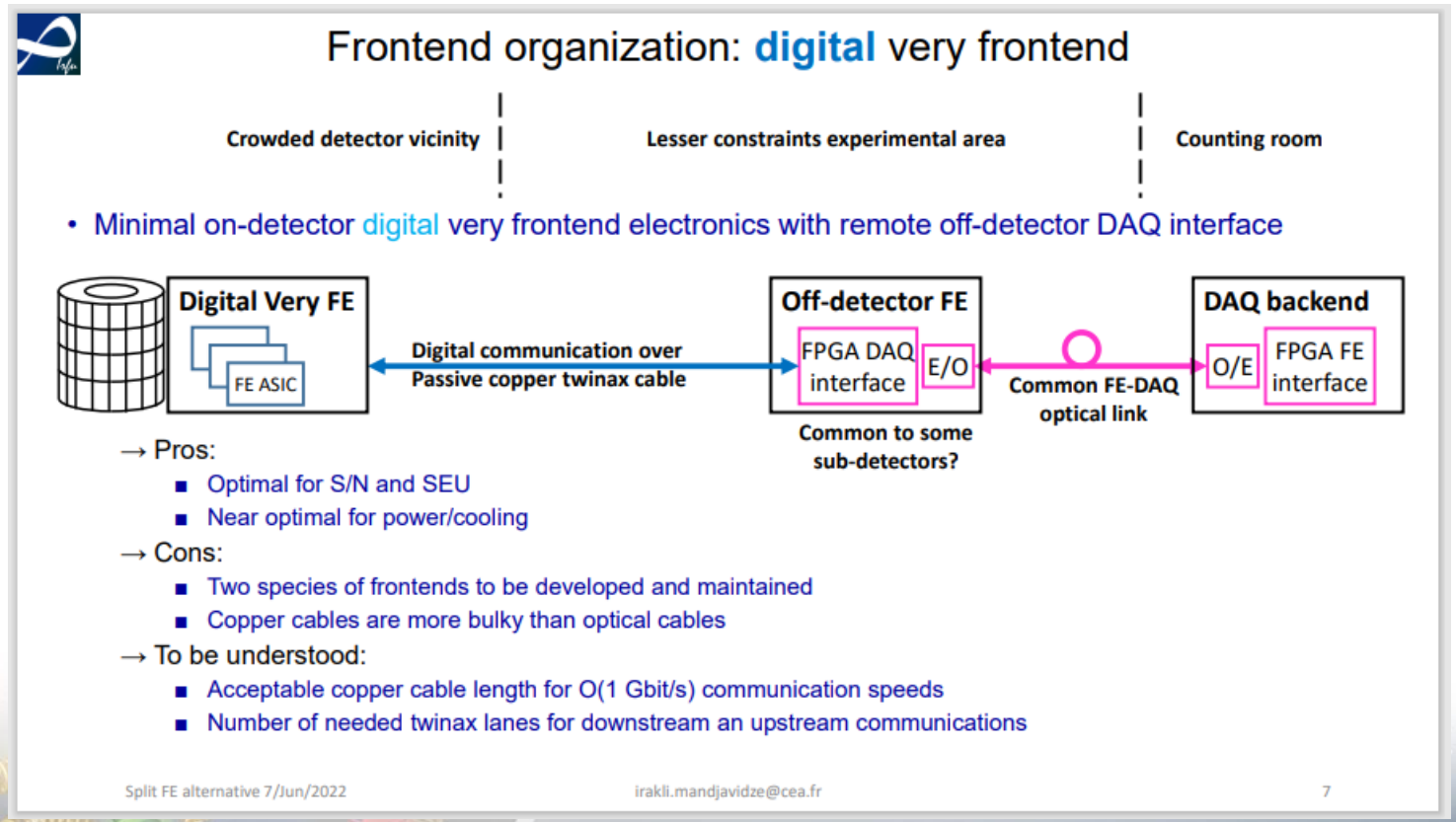
- **Global Timing**
  - High speed and precision combines custom designed and COTS componentry.
  - Provides synchronization of and clock distribution to the readout elements.
  - Jitter ~ 5 ps.

- **Network Switches/Servers/Computing/Link Exchange (FELIX)**
  - High performance COTS infrastructure.
  - Enables further reduction of data flow prior to storage via sophisticated algorithms, e.g., ML and AI.

- **Radiation levels** are much lower than at LHC. Studies are being performed to inform readout technology selection, however.

EIC Streaming Readout - Preferred Partitioning

- Reference proposal and Irakli's "digital very frontend" are similar and preferred.
- But some sub-detectors may adopt partitioning variations.



FEBs & FEPs Development

- "Coalesce" specifications to minimize the number of ASIC/FPGA/PCB part numbers.
- Power is nominally 1 W ± 0.25 W per ASIC (64 ch, 32 ch). Cooling systems will be an integral part of the detector design.
- Serviceability as a design criteria. Reliability assessment of componentry
- ASIC Development timeline is critical ~ **3.5 – 4 Years**
  - Revise and adapt present designs is our strategy.
  - Design re-use of IP blocks from existing ASICs.
- Standardization of data format (header, timestamp, etc.) at the system design level.
- Firmware development requires specialized expertise in close connection with both the detector development and the DAQ systems.
- Power demands for the FEPs, which are outside of the detector volume, can be high: cooling and other infrastructure needs are easier to manage.
- Testing and integration (w/ detectors/prototypes) takes considerable time and resources.

ePIC Detector Channels

Detector System	Channels	Nominal Readout Technology
Si Tracking: 3 vertex layers, 3 sagitta layers, 4 backward disks, 5 forward disks	7 m^2 32 B pixels 5,200 MAPS sensors	MAPS
MPGD tracking: 3 layers	100k	Strips
Calorimeters: Forward: LFHCAL pECAL HCAL inset Barrel: HCAL ECAL Imaging, if used Backward: ECAL	 60k 25k 8k 3k (25k?) 8k 50M pixels 25k	 SiPM
Far Forward: B0: 3 MAPS layers 1 or 2 AC-LGAD layer 2 Roman Pots 2 Off Momentum ZDC: Crystal Calorimeter 32 Silicon pad layer 4 silicon pixel layers 2 boxes scintillator	 3x20cmx20cm (300M pixel) 300k or 600k 1M (4 x 135k layers each) 650k (4 x 80k layers each) 400 11520 160k 72	 MAPS AC-LGAG AC-LGAD AC-LGAD APD HGCROC
Far Backward: Low Q Tagger 1 Low Q Tagger 2 2 Calorimeters	 1.3M 480k 700	 AC-LGAD AC-LGAD
PID-TOF	3M-50M	AC-LGAD
PID-Cherenkov: dRICH pfRICH (if selected) mRICH (if selected) DIRC	 300k 225k 74k	 SiPM SiPM SiPM

- Combining ECCE and ATHENA requirements.
- Subject to change but already well documented.

- ATHENA and ECCE were the two large submitted detector proposals and these had similar strategies on electronics and streaming readout.

Readout Channels

Detector Group	Channels			
	MAPS	AC/DC-LGAD	SiPM/PMT	MPGD
Tracking	32 B			100k
Calorimeters	50M		150k	
Far Forward	300M	2.3M	500	
Far Backward		1.8M	700	
PID		3M-50M	600k	
TOTAL	32 B	7.1M-54M	750k	100k

ASIC	ITS-3	EICROC	HDSoC HGCROC3 ALCOR-EIC	SALSA

- These ASICs are leading candidates for the EIC. The large number of channels, density, granularity and geometry favor high circuit density solutions.
- We continue to assess ASIC developments from other sources such as Pacific Microchip, Alphacore, SenseICs, Weeroc.
- Some sub-detectors, with less restrictive requirements, may benefit from discrete implementations and developments such as from STAR and sPHENIX.

Specifications *(subject to sub-detectors' final designs)*

- Nominal specifications for MPGD readout (ASIC)

Detector	
Capacitance	<200 pF nominal (500 pF maximum).
Noise	<3000 e^- @ 100 pF
Charge	25 fC – 100 fC (1 pC maximum).
Gain	$5x10^3 – 2x10^4$
Signal Time	100 ns – 500 ns (10 us ion drift time maximum), multiple hits per channel.
Signal Range	$<10^6$ e^-
Rates	<2 kHz per channel.
Readout	
Attributes	Amplification, digitization and buffering.
Features	Amplitude and time per hit; waveform samples for testing and calibration functions. Zero suppression; triggerless and triggered operation.
# Channels	64
Input Impedance	<70 Ohm
Gain	2 mV/fC – 30 mV/fC, configurable.
Peaking Time	40 ns – 250 ns shaping, configurable.
Crosstalk	<1 %
ADC Resolution	12 bit (>10 bit ENOB)
TDC Resolution	<20 ns
Sampling Rate	>80 MSPS
Optional	Discriminators and scalers are desirable.
Triggering	Streaming (triggerless) readout is the default mode. Triggered operation is required for testing and calibration functions.
Pulsing	Channel group pulsing desirable for testing function.
Output	TBD. Data format to be determined and to be consistent with optical fiber data transport between FEBs and FEPs.
Control Interface	TBD. Slow controls and configuration interface to be consistent with optical fiber data transport between FEBs and FEPs.
Technology Node	65 nm CMOS or higher.
Packaging	BGA or other SMT industry standard packages.
Power	1 W ± 0.25 W or < 20 mW per channel.
Supply	<+3 V DC

- Design of sub-detectors is on-going and their readout characteristics will change as well.
- Choice of GEM geometry and/or technology will impact Cd, for example.
- Design choice will inform ASIC optimization strategy for low noise, gain, etc.

- Nominal specifications for photon sensor readout (ASIC)

Detector	
Capacitance	60 pF – 5 nF (depending of cell size and grouping), <30 pF for PMTs.
Noise	1 p.e. @ <100 kHz, nominal (extends to 3 p.e.), lower for PMTs.
Gain	$<10^6$
Signal Time	3 ns – 80 ns
Rise Time	1 ns – 3 ns
Signal Range	<1 V into 50 Ohm or $<10^5$ pixels.
Rates	<50 kHz per channel.
Bias	Vop ~ 50 V DC for SiPMs.
Readout	
Attributes	Waveform sampling. Amplification, signal conditioning, digitization and buffering.
Features	Amplitude and time per hit. Zero suppression; triggerless and triggered operation. Input offset voltage adjustment.
# Channels	64
Input Impedance	<50 Ohm, depends on configuration.
Gain	1 - 10, configurable.
Peaking Time	<40 ns for SiPMs, ~1 ns for PMTs.
Crosstalk	<1 %
ADC Resolution	10 - 14 bit
TDC Resolution	1 ns for SiPMs, <100 ps for PMTs.
Sampling Rate	>80 MSPS for SiPMs, >1 GSPS for PMTs.
Optional	Discriminators and scalers are desirable.
Triggering	Streaming (triggerless) readout is the default mode. Triggered operation is required for testing and calibration functions.
Pulsing	Channel group pulsing desirable for testing function.
Output	TBD. Data format to be determined and to be consistent with optical fiber data transport between FEBs and FEPs.
Control Interface	TBD. Slow controls and configuration interface to be consistent with optical fiber data transport between FEBs and FEPs.
Technology Node	65 nm CMOS or higher.
Packaging	BGA or other SMT industry standard packages.
Power	1 W ± 0.25 W or < 20 mW per channel.
Supply	<+3 V DC

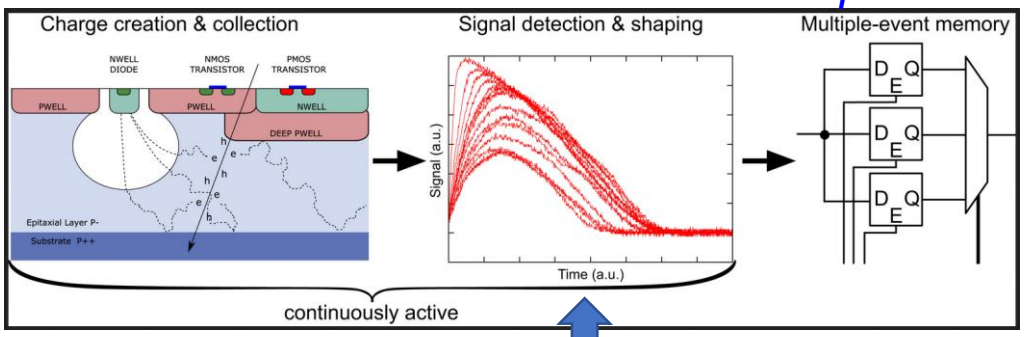
- SiPMs have relatively large capacitance: paralleling multiple cells presents some challenges to the design of the front-end.
- The large number of channels, good temperature stability and overvoltage control favor an ASIC solution.

MAPS – ITS-3

(Monolithic Active Pixel Sensor)

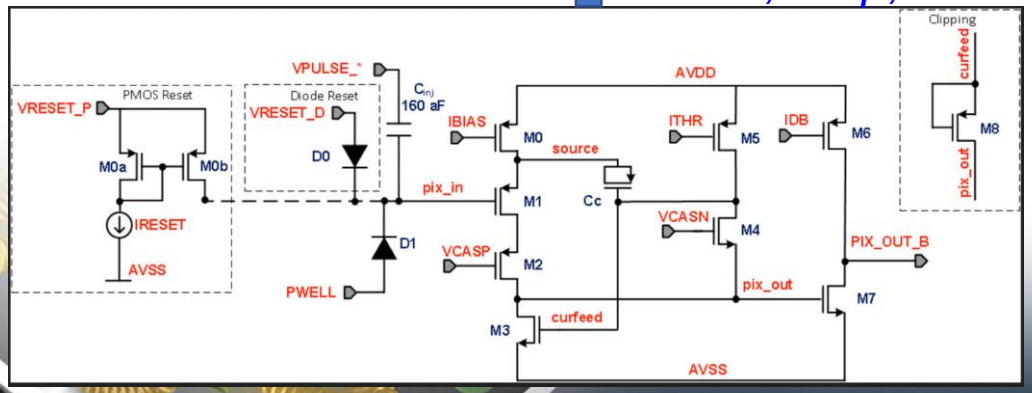
- Based on ALICE ALPIDE - 62 nm CMOS.
- Development under eRD112, closely coupled to detector.
- Tr < 2 us, longer shaping ~ delay line: strobed into in-pixel buffers.
- Power Density 40 nW/pixel.
- Radiation Tolerant.

Operation



- Asynchronous readout via Priority Encoder.
- Hit-driven readout.
- 1.2 Gbps serial link, ~7 m twinax.
- Data packet with Timestamp.

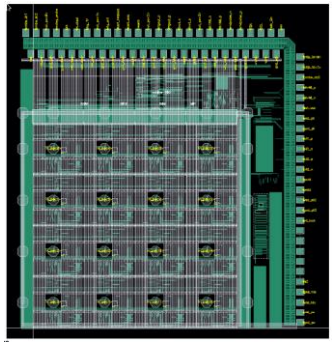
Reset, Amp, Disc



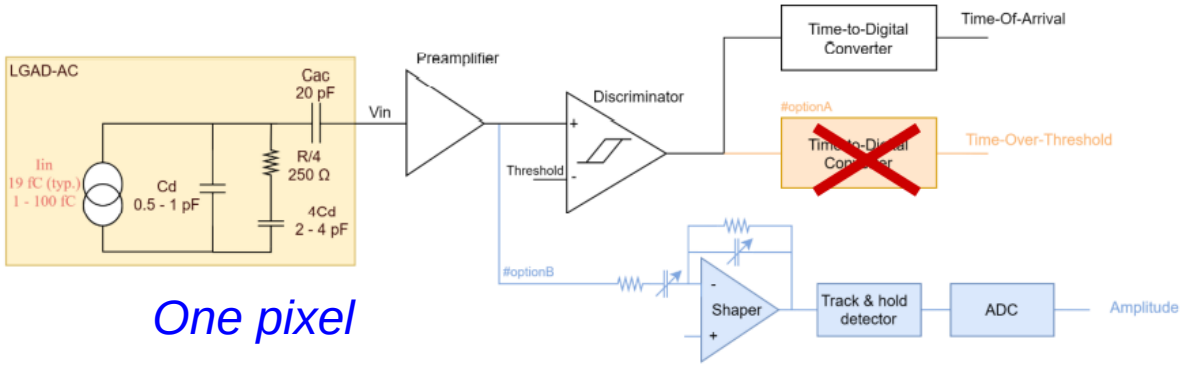
AC-LGAD – EICROC0

(Low Gain Avalanche Diode)

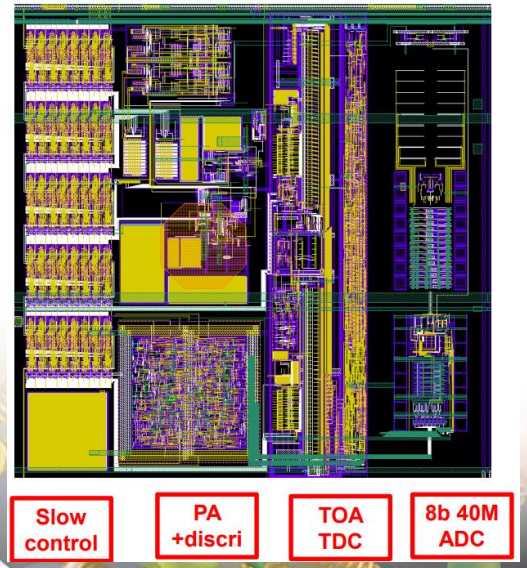
- Development under eRD112, closely coupled to detector.
- Collaboration of IJCLAB/OMEGA/Irfu/AGH.



4x4 500 um pixels



One pixel



One pixel

- Preamp, discriminator – ATLAS ALTIROC.
- I2C slow controls – CMS HGCROC.
- TOA TDC – Irfu Saclay.
- ADC (8b) – AGH Krakow.
- Readout FIFO depth 8 (200 ns).
- Jitter: 15-20 ps.
- Power: 1-2 mW/Ch.

- EICROC0 – under test.
- EICROC1 – Larger, FY23.

SiPM/PMT/LAPPD – HDSoC/HGCROC3/ALCOR

(//Large Area Picosecond Photo Detector)

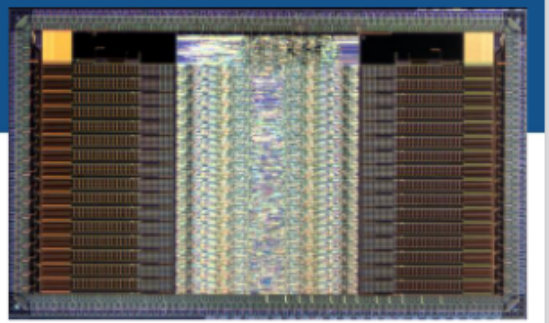
HDSoC V1 DESIGN DETAILS

High density waveform digitizer with dead-timeless readout

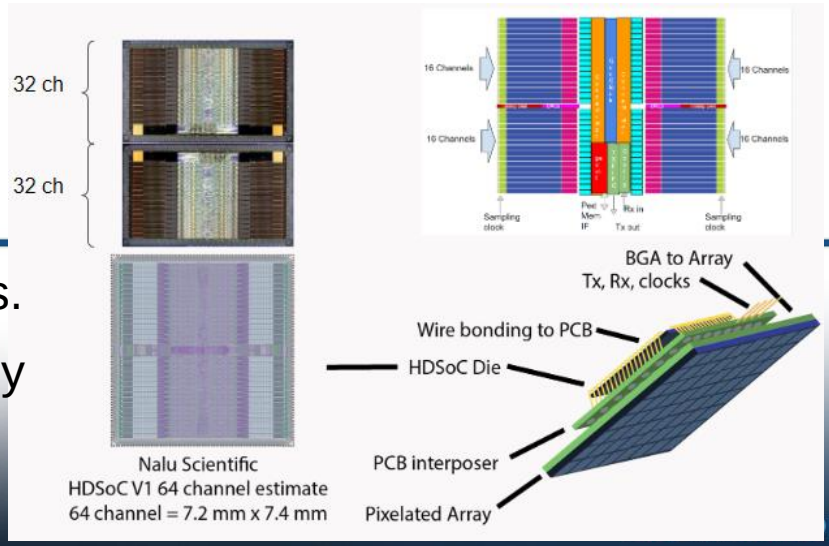
- High Density: 64 channels
- Highly integrated, SiPM gain + bias
- Commercially available, low cost CMOS

Parameter	Spec
Sampling Rate	1-2 GSa/s
ABW	> 600MHz
Depth	2k Sa
Trigger Buffer	~3 us*
Deadtime	0**
Channels	64
Supply/Range	2.5
ADC bits	12
Timing accuracy	80-120ps
Technology	250 nm CMOS
Power	TBD

- On chip calibration
- Serial interface
- On chip feature extraction
- Virtually dead-timeless
- 32 ch proto chip fabricated
- Phase II SBIR in progress
- Chip under test
- Next steps: more testing, rev 2 fab

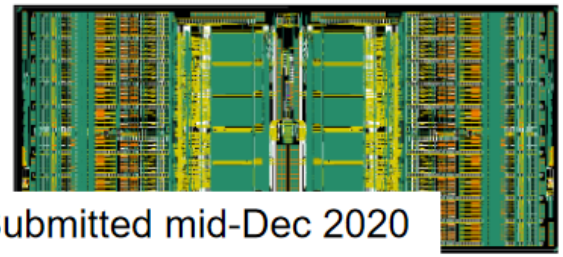


HDSoC v1 die shot

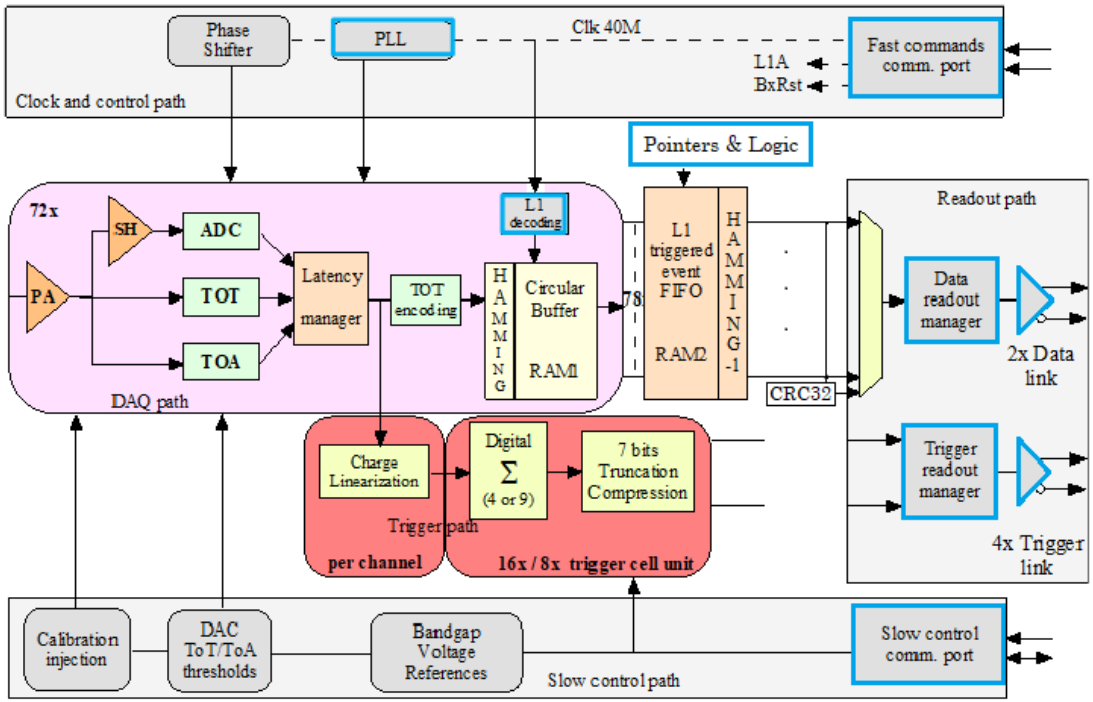


- Triggerless and Triggered modes.
- 64 ch V2 submission late 2022 by NALU.

HGCROC3



Submitted mid-Dec 2020

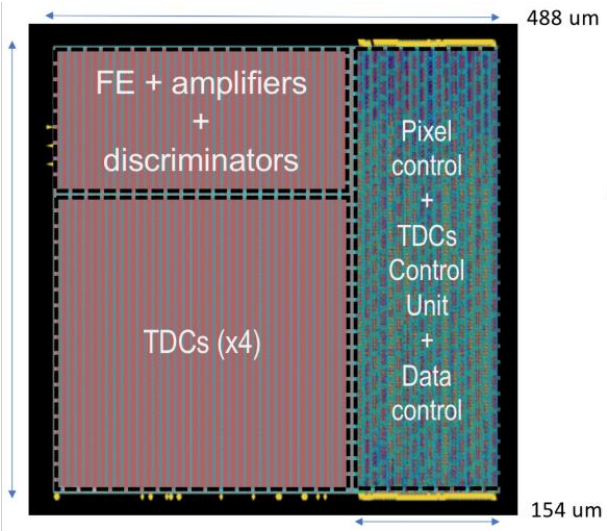


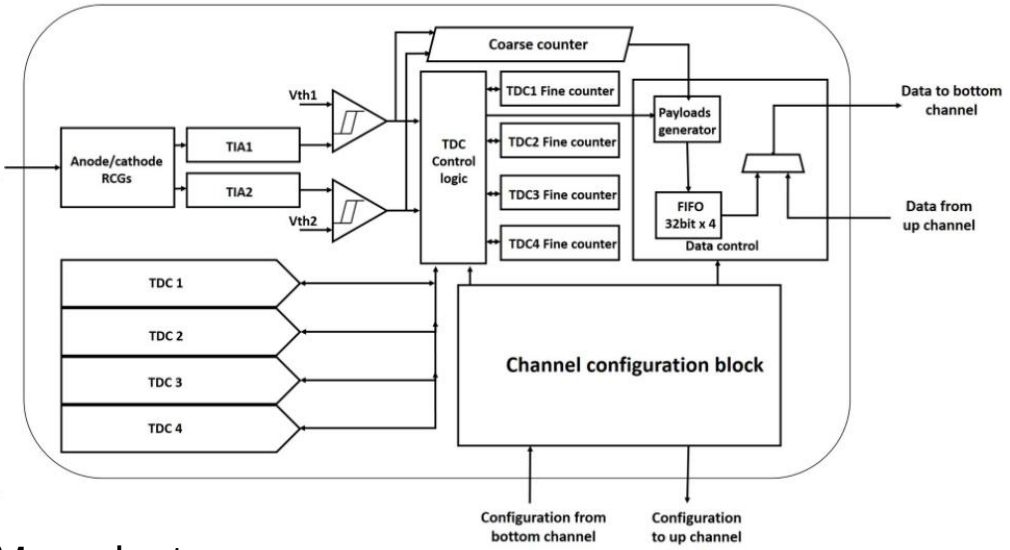
- Si, SiPM versions.
- Large dynamic range.
- Low noise.
- Charge: ADC+TOT.
- Time: TOA (25 ps).
- 512 DRAM buffer.
- 2x 1.28 Gbps links.
- I2C controls.
- 40 MHz operation.
- 20 mW/Ch.
- Radiation tolerant.

- Possible redesign for EIC streaming readout: 100 MHz, Cin ~ 2 nF.

ALCOR-EIC

- Development by INFN.



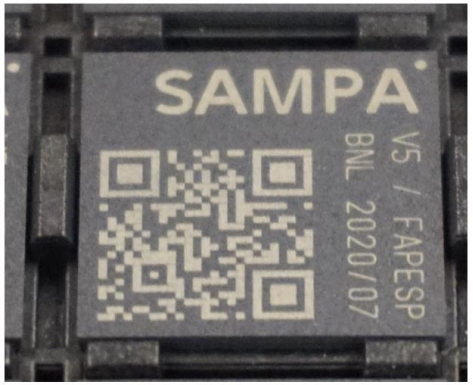


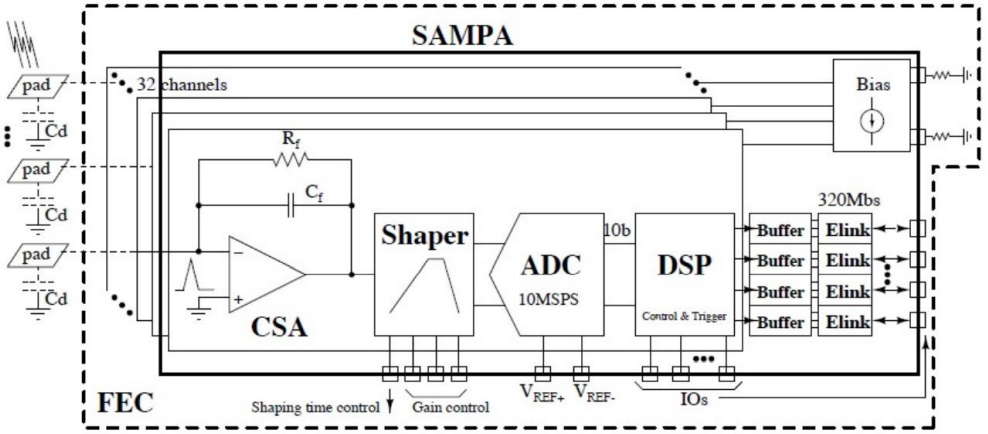
- 32-Ch, 110 nm CMOS, SiPM readout.
- Dual polarity, RCG Amplification, conditioning, digitization.
- Modes of operation: single-photon tagging or time and charge.
- Triggerless and triggered operation.
- 50 ps TDCs (320 MHz).
- 4x 625 Mbps LVDS links.
- SPI configuration.

- ALCOR-EIC0 – FY22.

SALSA

- Collaboration of Irfu CEA Saclay and U. of Sao Paulo.





- 64-Ch, updated design from SAMPA V5, migrating to 65 nm CMOS.
- Peaking time: 50 – 500 ns
- Inputs: Cin optimized for 200 pF; Rates: 25 kHz/Ch; Dual polarity.
- ADC: 12 bits, 10 – 50 MSPS.
- Extensive data processing capabilities.
- Triggerless and triggered operation.
- Power: 15 mW/Ch
- Gbps links.
- I2C configuration.

- SALSA prototype submission – late 2022 (a few channels).

eRD109 – Upcoming R&D Initiative

- Addresses ASIC and Electronics R&D needs.
- Call for proposals communicated to all sub-detector working groups.
- Proposals due by October 2022.
- Duration of 4 Years.
- Tentative funding (total): $2.5M.
- Preliminary interest from:
  - EICROC – In-kind contribution to date.
  - HGCROC3 – possible updated design.
  - ALCOR-EIC - In-kind contribution to date.
  - SALSA – awaiting determination from French and Brazilian funding agencies.

EIC Electronics Needs - Summary

- **ASICs** – Application Specific Integrated Circuits
  - Design and/or Fabrication Services – e.g., MOSIS, TSMC, Global Foundries, etc. Multi-channel, low power, high speed. Qty. > 10,000 devices.
  - Design re-use from existing and under-development ASICs.

- **Photon Sensors (SiPMs/MCP-PMT/MaPMT)** – COTS. Qty. < 1 Million cells

- **Electronic components & PCBs** – by consignment or turnkey fabrication and assembly services – e.g., multi-layer with ASICs, FPGAs, etc. Qty. < 1,000.

- **Cabling** – Turnkey fabrication services of various types of cables and optical fibers (COTS) and per supplied specifications. Cables must meet a minimum of UL CL2 specifications. Qty. > 1,000.

- **Power Supplies** – Multi-channel, Low Noise, Floating, Modules:
  - Low Voltage (LV) - < 15 VDC, 5 A – 10A range per channel. Qty. > 1,000.
  - Bias - < 100 VDC, mA range per channel. Qty. > 10,000.
  - High Voltage (HV) - < 8 kV, mA range per channel. Qty. > 1,000.

- **Racks and Cooling** – COTS. Qty. < 100.

Infrastructure and Standards

Environment	21 °C ± 2 °C, RH < 50%.
Grounding	Grounding in detector interaction region area by bonding of segregated loads via multiple, low inductance conductors to existing infrastructure.
Cabling	NEC 2011 NFPA 70, UL CL2 or better.
Cable Routing	NECA/NEMA 105-2007. Open cable tray systems.
EMI & RFI	FCC part 15 Class B, CISPR 11/ EN 55011 Class B, CISPR 22/ EN 55022 Class B and EN 61000-6-3, or equivalent.
Power Supplies	Floating and referenced to the detector ground.
Racks	Open frame, COTS (e.g., Hammond C4F247736) with horizontal and vertical cable managers.

Note that exceptions to or non-conformance with these standards and guidelines must be approved prior to installation.

Infrastructure and Standards - Grounding

- Power Supply & Cooling Systems
  - Use COTS units – Wiener, CAEN, …

- Grounding & Shielding
  - Builds upon the STAR installation, uses floating supplies referenced to ground at the detector for low noise and good signal integrity.

Grounding Column in IR

Low Impedance connection via 6, 4/0 cables.

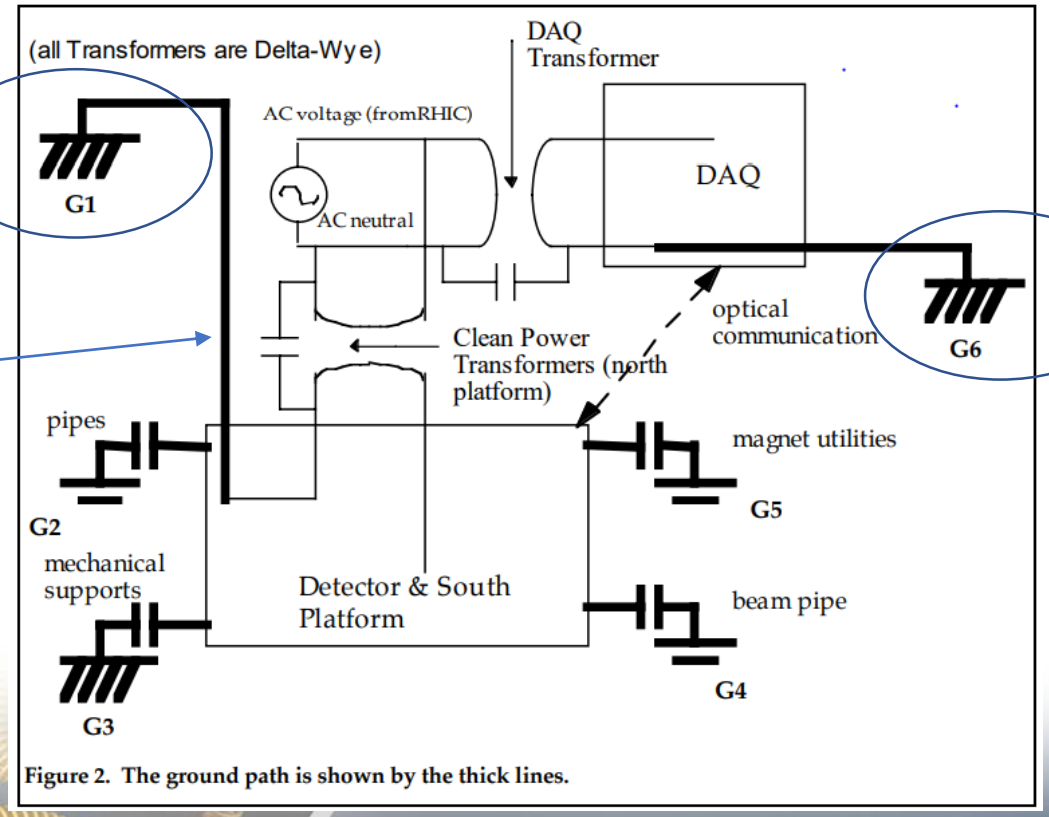


Figure 2. The ground path is shown by the thick lines.

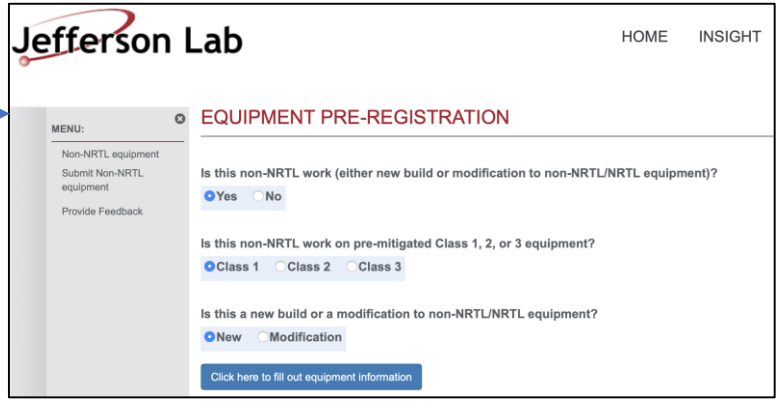
Grounding in DAQ House

*Minimize capacitive coupling (G2 – G5).

STAR Note 202A, H. Matis, D. Jared

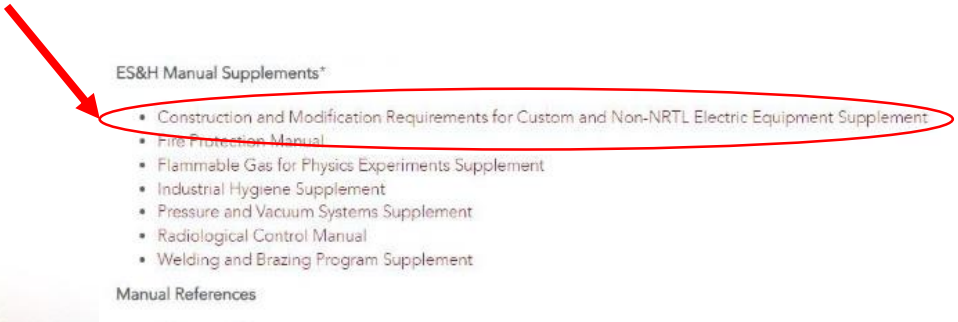
JLAB EHS&Q Process for “in-kind” Electronics

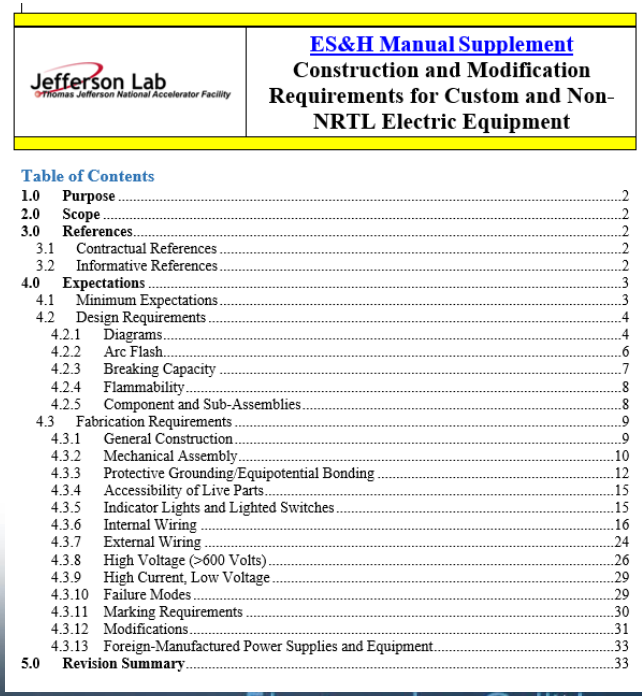
- Custom electronics built by collaborators for use in experiments at JLAb must go through a registration process first.



- This is any equipment that is NOT certified by a Nationally Recognized Test Lab (NRTL) like UL and recognized by OSHA.

- The JLAB EHS&Q Manual has a supplement guide for construction and/or modification of any custom or non-NRTL equipment.




Jefferson Lab
Thomas Jefferson National Accelerator Facility

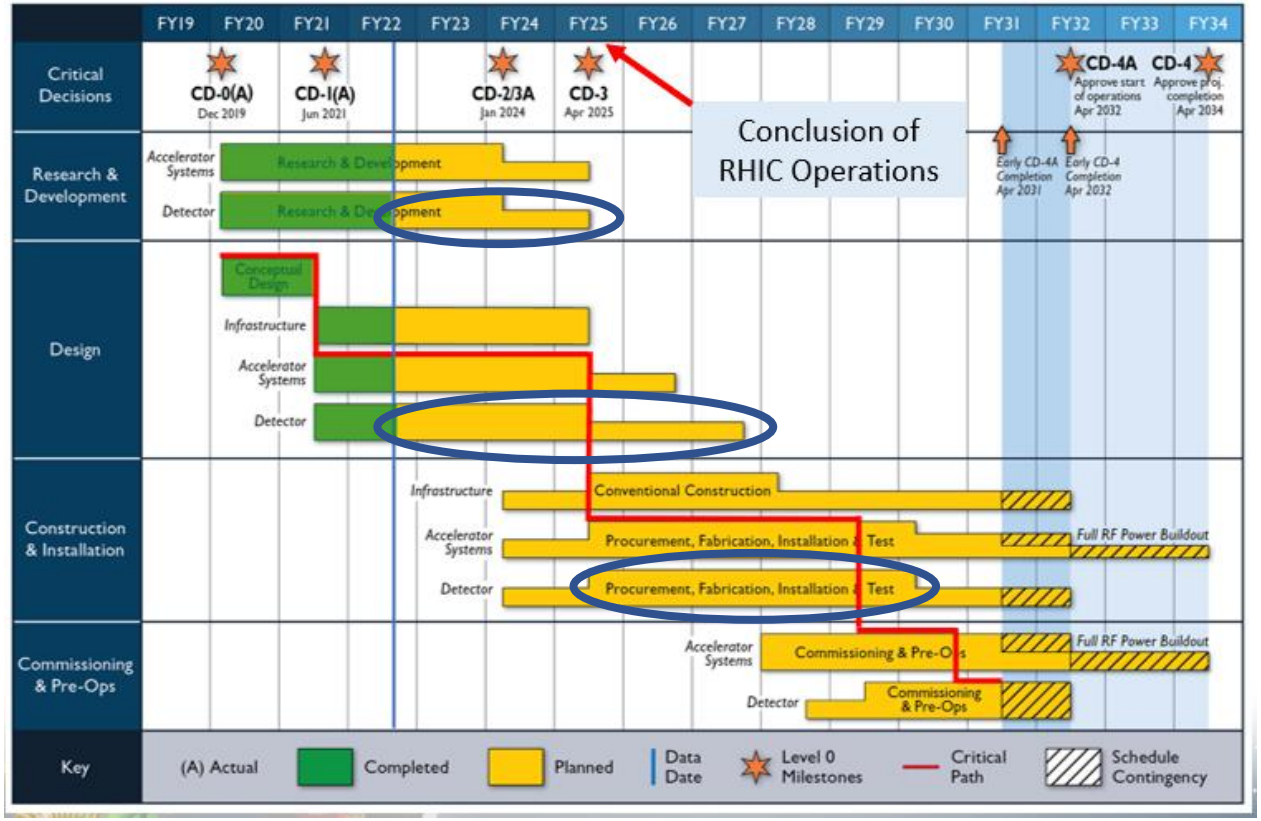
ES&H Manual Supplement
Construction and Modification Requirements for Custom and Non-NRTL Electric Equipment

Table of Contents

- BNL also has a review process in place.

Timeline

- **Construction and Installation includes procurements and deliveries and are initiated at different times of this phase.**



R&D until 4/2025.

(Most~1.5 Years)

Design until 9/2027.

(Most~2 Years)

4/2025 to 4/2031.

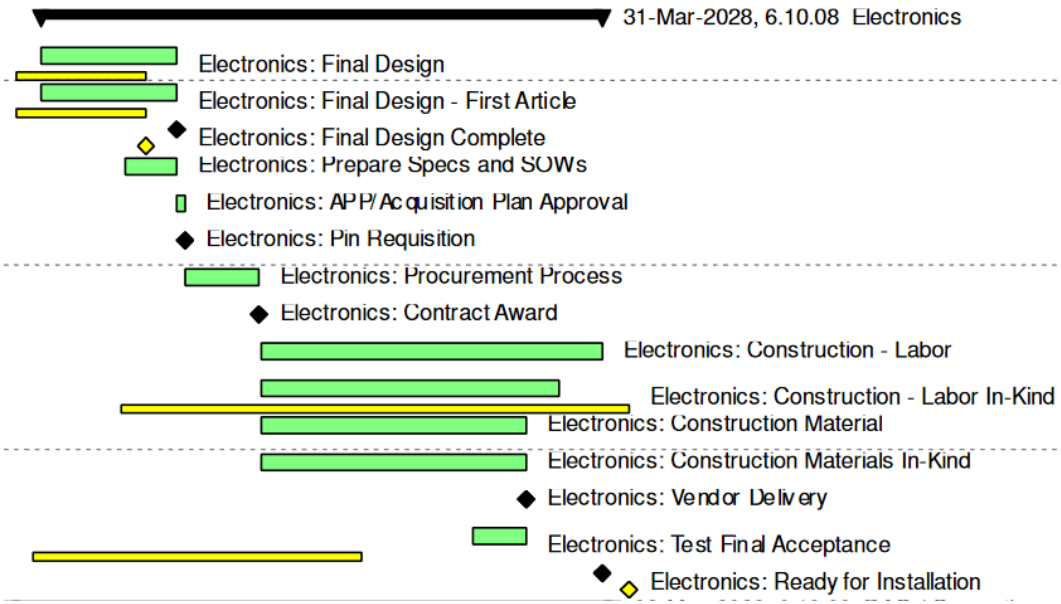
(~6 Years)

- **Bulk of Construction & Installation phase for Electronics: April 2025 – January 2030.**
- **Installation of some items may be extended to April 2031.**

Timeline

- Resource loaded schedules were earlier developed for the Reference Detector (CD-1) and then for the ECCE selected proposal.
- ePIC presently follows the ECCE proposed schedule.

Summary Gantt chart for Electronics WBS 10.06.08 (internal tasks not shown for simplicity)



- The Primavera P6 will be submitted by January 2023 with updated information and as designs mature.

- DOE OPA Status Review: January 2023 (Primavera P6 towards final version).
- CD-2/3A – Baseline: January 2024
- CD-3 – Construction Phase: April 2025 – January 2030

Summary

- ePIC is actively developing a streaming readout architecture, benefiting from resources within its large collaboration and to meet the physics goals of the EIC.
- Developing the readout electronics by building upon previous developments, with design re-use as a guiding principle.
- Engaging the community and benefiting from in-kind contributions.
- Developing resource-loaded schedules to meet the overall EIC project schedule within cost boundaries.
- Developing a readout system meeting US standards and within the EHS&Q frameworks of partner organizations, BNL and JLab.