

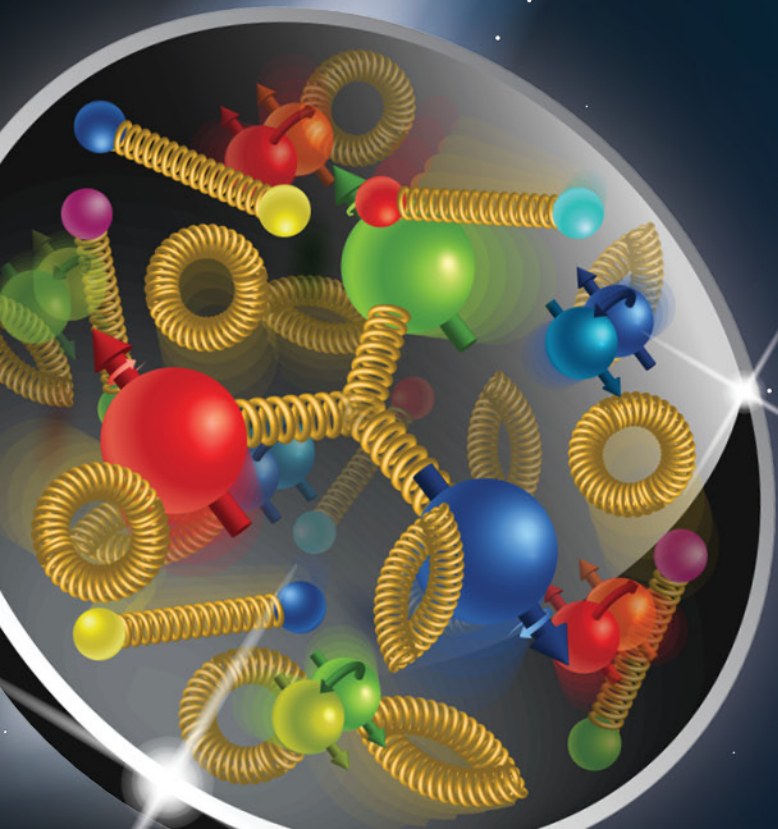
# EIC Project Update

## EIC DAQ Status WBS 6.10.9

David Abbott and Jeff Landgraf  
L3 CAMs for EIC Detector Project  
Electronics/DAQ status Review

August 29, 2022

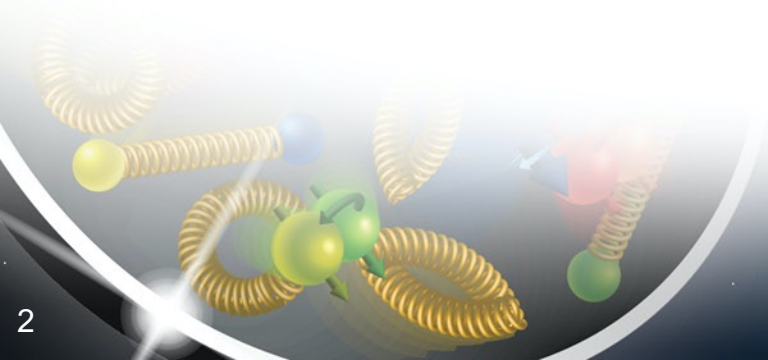
Electron-Ion Collider



# EIC DAQ/Online Computing Overview

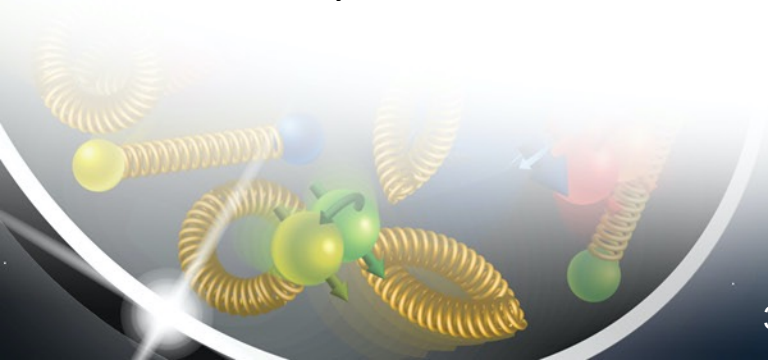
- The EIC Streaming Readout (SRO) Consortium was formed in 2018 with the goals of engaging the nuclear physics community in exploring the advantages, challenges and requirements to implement a 100% streaming readout architecture for the EIC detectors.
  - Series of ten workshops between 2018 and 2022.
- General agreement in the Yellow Report, that the adoption of SRO would maximize the impact of the physics program for EIC.
- In this presentation the focus is on DAQ and Online Computing (EIC Project)
  - General DAQ architecture
  - Expected technology choices
  - Interface with "offline" computing
  - Relative schedule wrt to the EIC Detector project

| EIC Critical Decision Plan |                     |
|----------------------------|---------------------|
| <b>CD-2/3a</b>             | <b>January 2024</b> |
| CD-3                       | April 2025          |
| CD-4a early finish         | April 2031          |
| CD-4a                      | April 2032          |
| CD-4 early finish          | April 2032          |
| <b>CD-4</b>                | <b>April 2034</b>   |

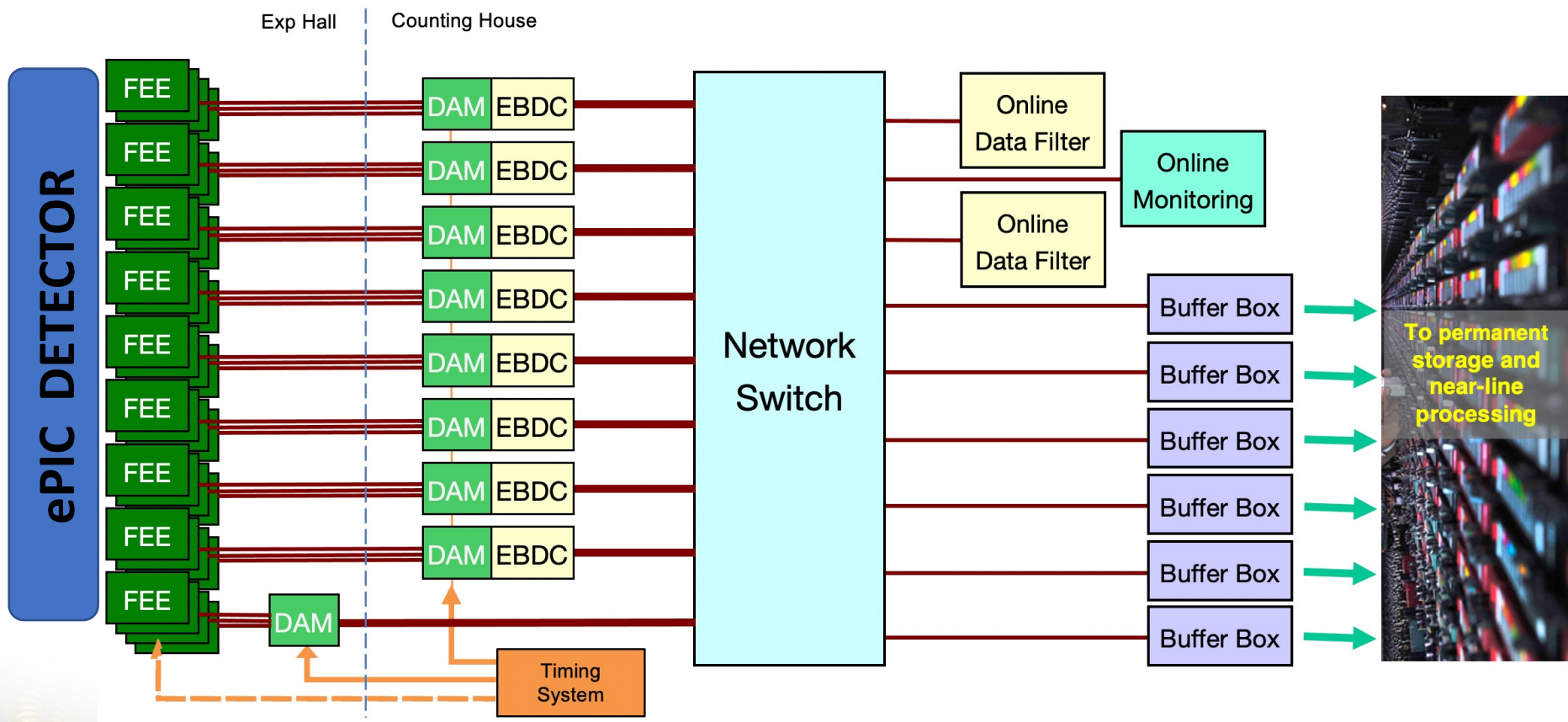


# EIC SRO Community

- Streaming Readout X Workshop (May 2022)
  - 74 participants
  - Discussions on requirements/plans/priorities and future of the SRO consortium
  - Brought together Electronics, DAQ, Computing and Industry interests
- ePIC Electronics/DAQ Working Group
  - A Camsonne (JLAB), C. Cuevas (JLAB), J. Landgraf (BNL), J. Schambach (ORNL)
  - Regular meetings to focus on design and requirements specifically for the new EPIC detector
  - Interface to detector, readout, DAQ, online processing, monitoring and control.
- ePIC Software/Computing Working Group
  - A. Bressan (CERN), C. Fanelli (W&M), S. Joosten (ANL), D. Lawrence (JLAB)
  - Coordinating software development for EIC physics
  - Analysis Frameworks, Reconstruction, Simulation, AI & ML



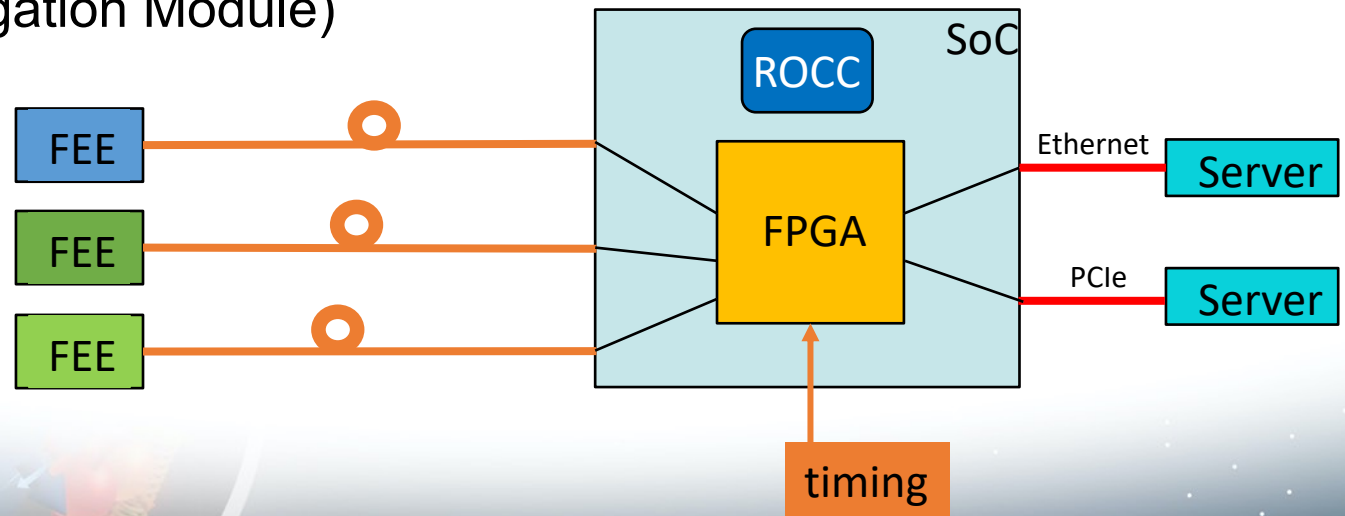
# EIC Streaming DAQ/Computing Architecture





# DAQ Interface to the Detector Systems

- Managing data “streams” is ideally done in a deterministic way – e.g. FPGAs
- Proprietary communication with the front-end electronics.
  - Bi-directional link (fiber)
  - Send: clock, commands, control, config
  - Receive: high speed data streams
- System on Chip (SoC) facilitates DAQ/User applications to communicate with the Front-end.
  - Readout Configuration and Control
- DAM (Data Aggregation Module)

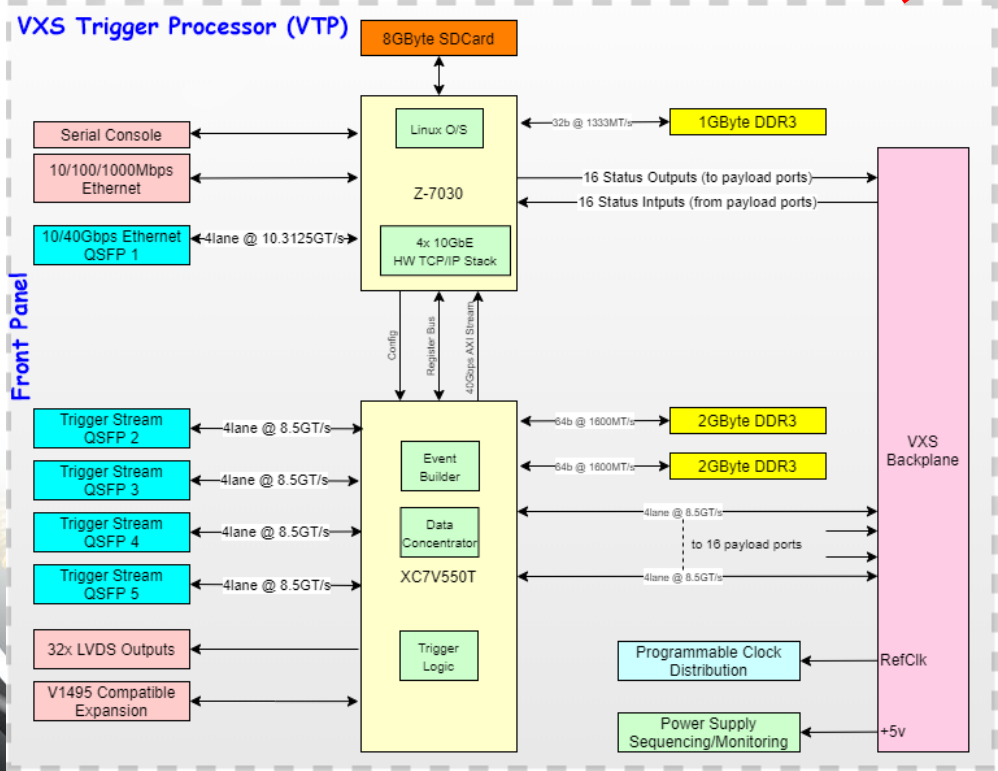


# JLAB VXS/VTP

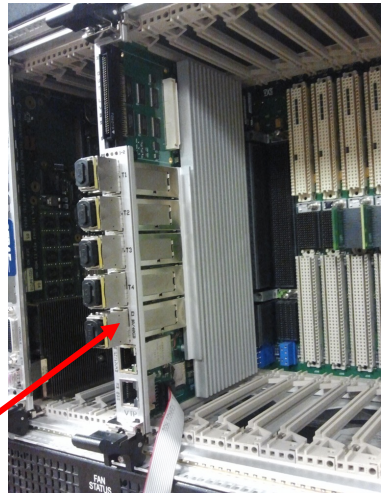
Linux OS on the Zync-7030 SoC  
(2-core ARM 7L , 1GB DDR3)  
10/40Gbps Ethernet option

## Xilinx Virtex 7 FPGA

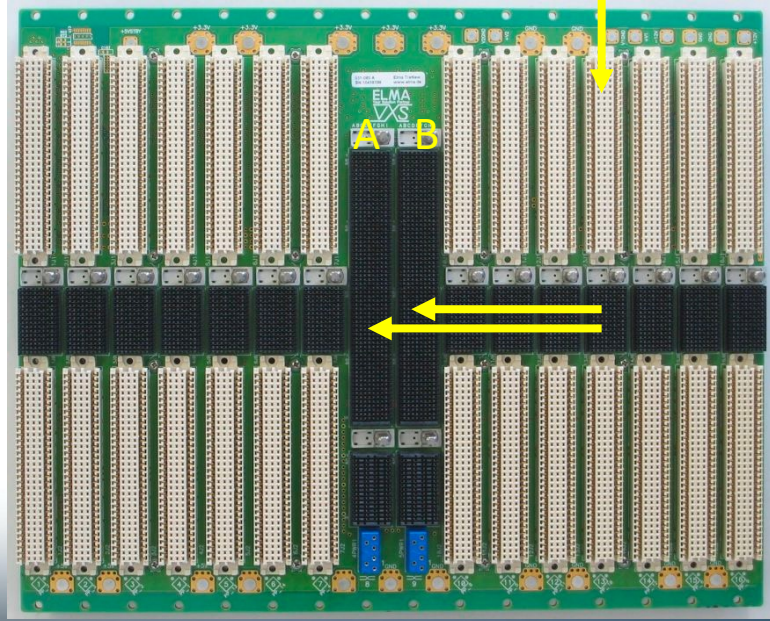
Serial Lanes from both the VXS backplane and the Front panel  
4GB DDR3 RAM



JLAB 250MHz FADC



16 Chan



Electron-Ion Collider

# DAM Option - Front-End Link Exchange (FELIX)

- Originally developed for ATLAS at CERN
- Design team is based at Brookhaven
  - Current version in use at BNL for sPHENIX
- New board being prototyped now for ATLAS HL-LHC running.

- All three sPHENIX tracking detectors use streaming readout
- Completed construction of sPHENIX FELIX DAQ interface (~50)

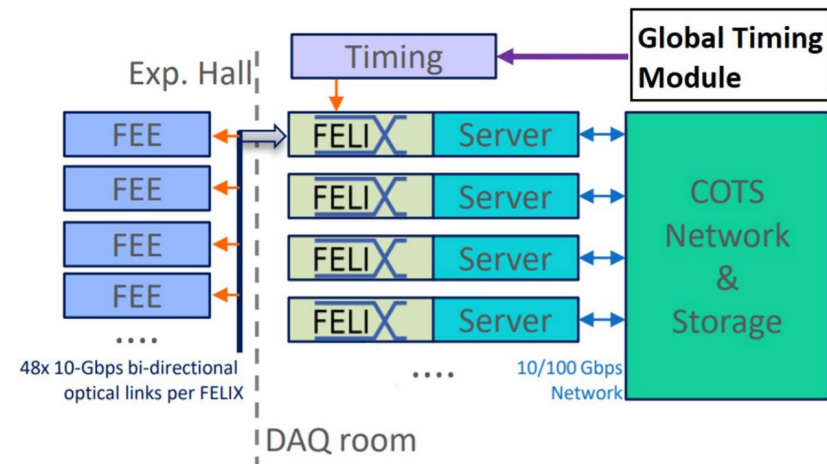
MVTX RU



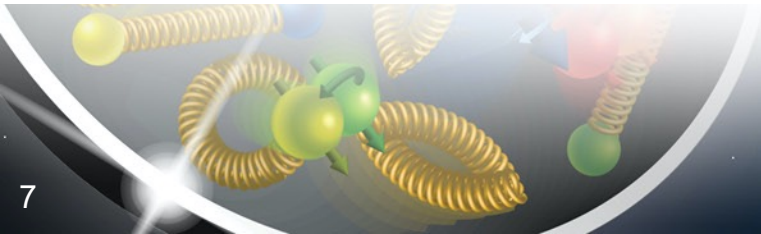
INTT ROC



TPC FEE



Architecture of sPHENIX streaming DAQ



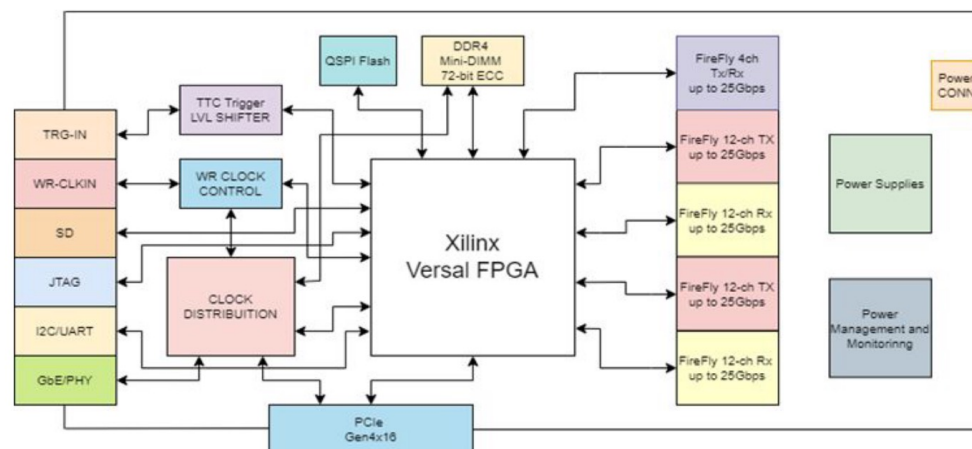


# Next Generation FELIX

## Prototype: FLX-182

FPGA: Xilinx Versal Prime XCVM1802-1MSEVSVA2197  
production device

- PCIe Gen4 x16: PL and CPM compatible
- 24 FireFly links with 3 possible configurations
  - 24 links @25 Gb/s
  - 24 links @10 Gb/s (CERN-B-Y12)
  - 12 links @25 Gb/s + 12 links @10 Gb/s
- 4 FireFly links with 2 possible configurations
  - LTI interface
  - 100GbE
- Electrical signals on front panel
  - 3 inputs and 3 outputs
- 1 DDR4 Mini-UDIMM
- USB-JTAG/USB-UART



Block diagram of FLX-182

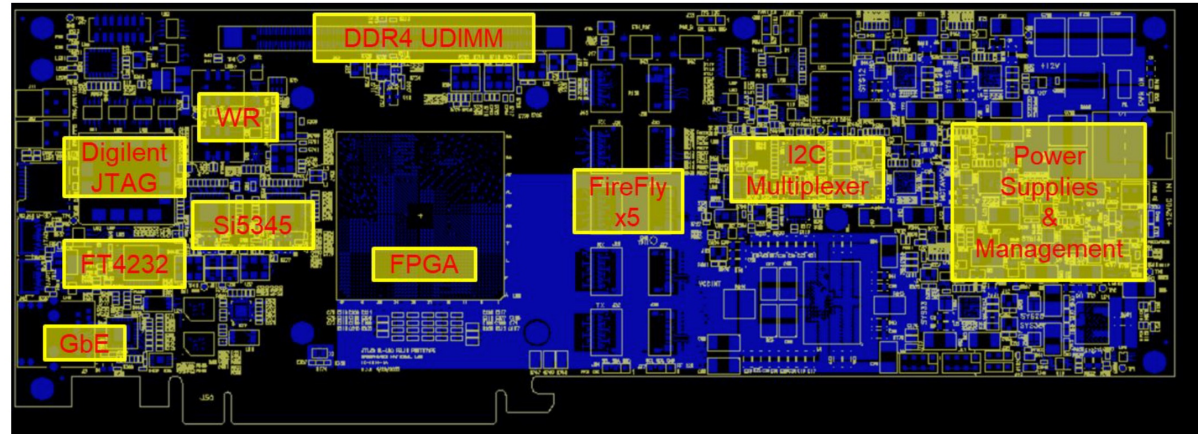
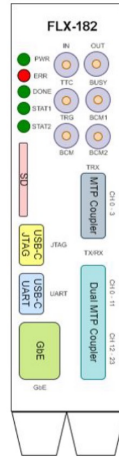
**Notes:** The Xilinx Versal Prime is a SoC.- Dual Core ARM Cortex  
Power usage ~133W. No power through PCIe.  
Can be implemented as a stand alone device (no Server)



# FELIX timelines

7 boards to be produced by the end of 2022.

More production possible when the FPGA is generally available.



General technical support for the FELIX Hardware should be available through the end of HL-LHC operation – i.e. into the late 2030s for Run 5.

## Plan for 48-ch FELIX

- FPGA: Versal Premium, e.g. VP1552
- Transceivers: Up to 100+ GTYP/GTM
- PCIe Gen 5 up to 16 lanes
- If FPGA is available as planned, design will start in Q1 of 2023, first board is expected to be available in Q3 2023.

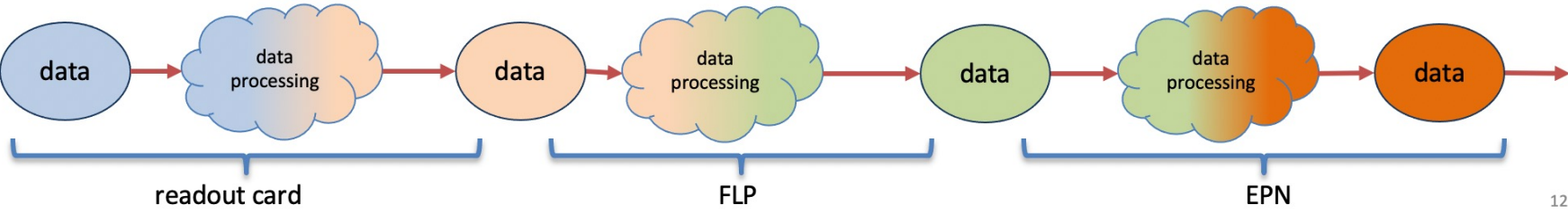
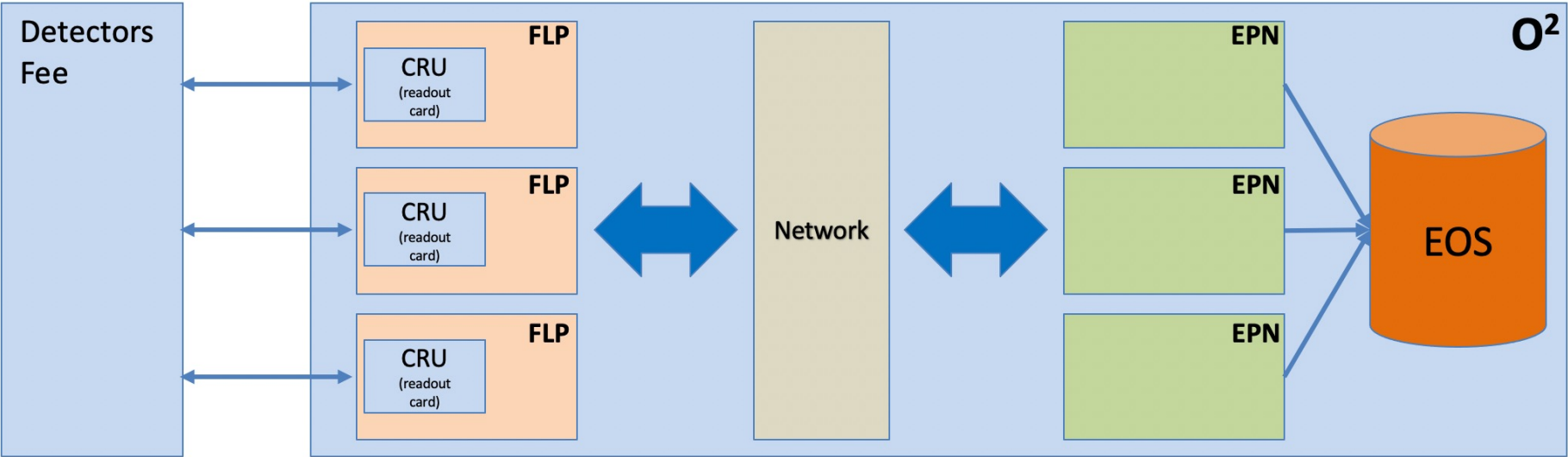
Thanks to Hao Xu from BNL for this information

# Proposed EIC DAQ has been done already at the LHC

A Large Ion Collider Experiment



## CPU USAGE



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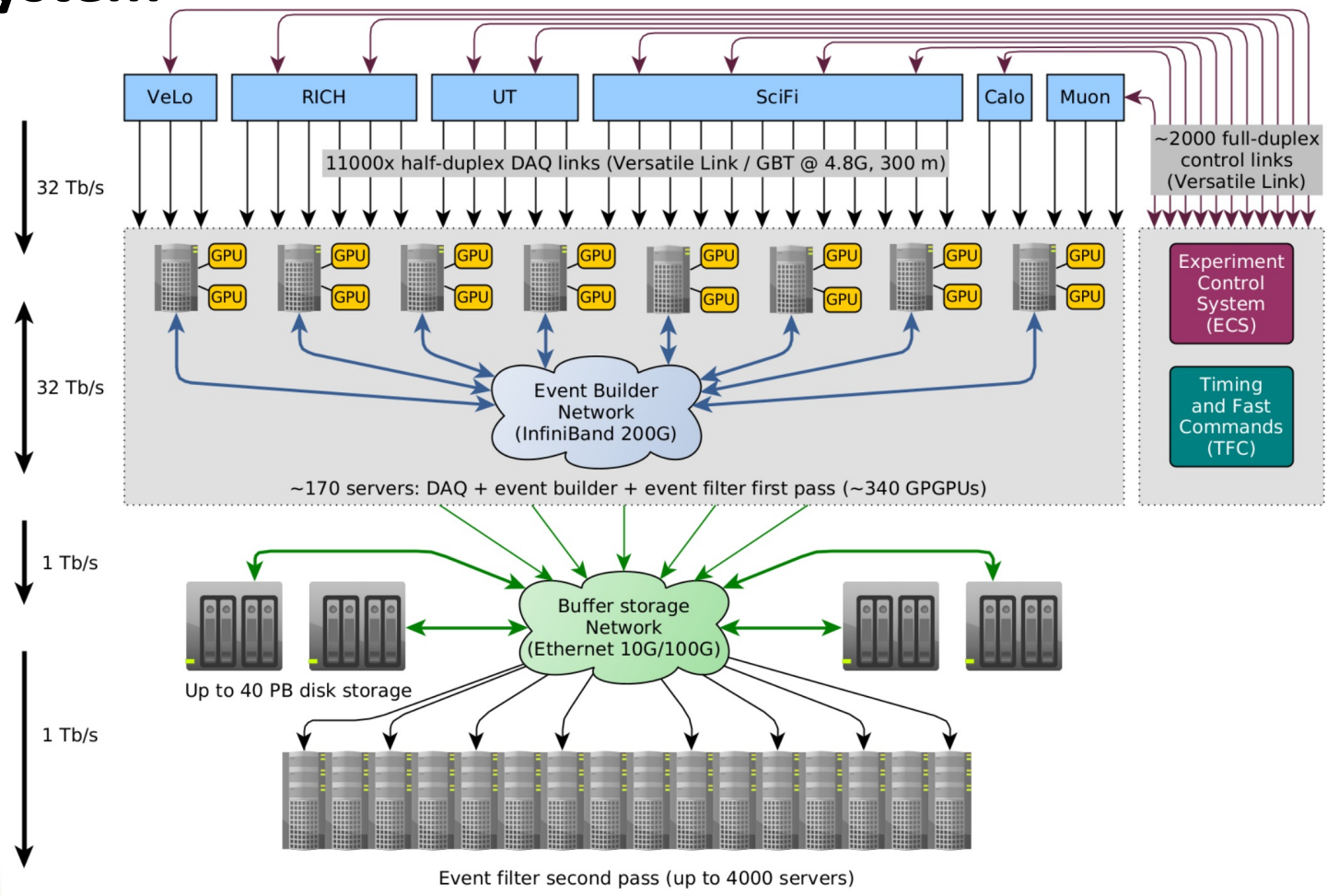
*Slide courtesy of Fillipo Costa from the ALICE collaboration*

And here as well...

# LHCb DAQ System

And at a ~5X  
larger scale than  
ePIC

Through the  
Streaming Readout  
workshops we have  
been in regular  
contact with both  
both ALICE and LHCb  
DAQ teams

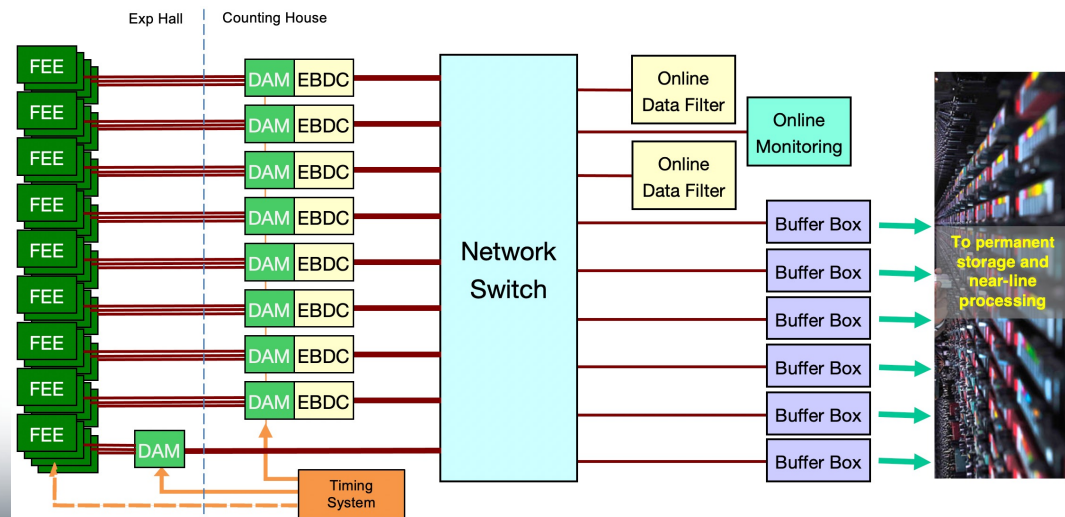


Slide courtesy of Niko Neufeld from LHCb



# Scale of the Task

- EIC minimum bias collision rate  $\sim 500\text{kHz}$ 
  - Expected real physics data from the detector  $< 100\text{Gbps}$
- Background/Noise is the wild card.
  - Synchrotron radiation, Beam Gas, Detector/electronics noise
  - Try to keep below the level of the physics signal.
  - DAQ processing will focus on Event ID and reducing the background
- Front-End (DAM Boards) - will support total bandwidth  $O(50\text{Tbps})$ 
  - 3000+ fibers(streams) off the detector (nominally  $10\text{Gbps}$  links)
  - $\sim 110$  DAM Boards
- Online DAQ/Computing (over  $100/400\text{Gbps}$  network)
  - $\sim 200$  nodes
  - GPU/FPGA processing options
  - Data Monitoring
  - Staged disk storage (Buffer Box)

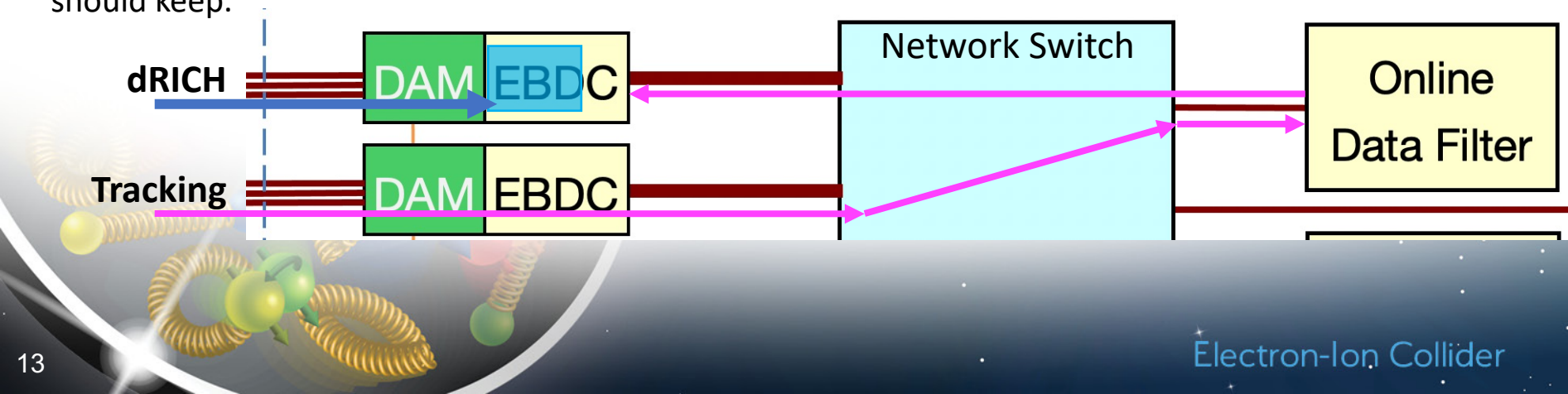


# Potential “Hot spots”

- In general the high fiber counts coming to the DAM boards are not bandwidth driven, but the expected numbers of FEEs needed to instrument the ePIC detector. **However...**
- Detectors using SiPM readout at thresholds sensitive to single photons
  - Dark current rates will increase over time due to radiation damage.
  - E.g. dRICH could eventually generate ~1800Gbps data rates
- Backwards detectors can generate excessive tracks associated with high electron bremsstrahlung rates. (**estimates ~100Gbps**)

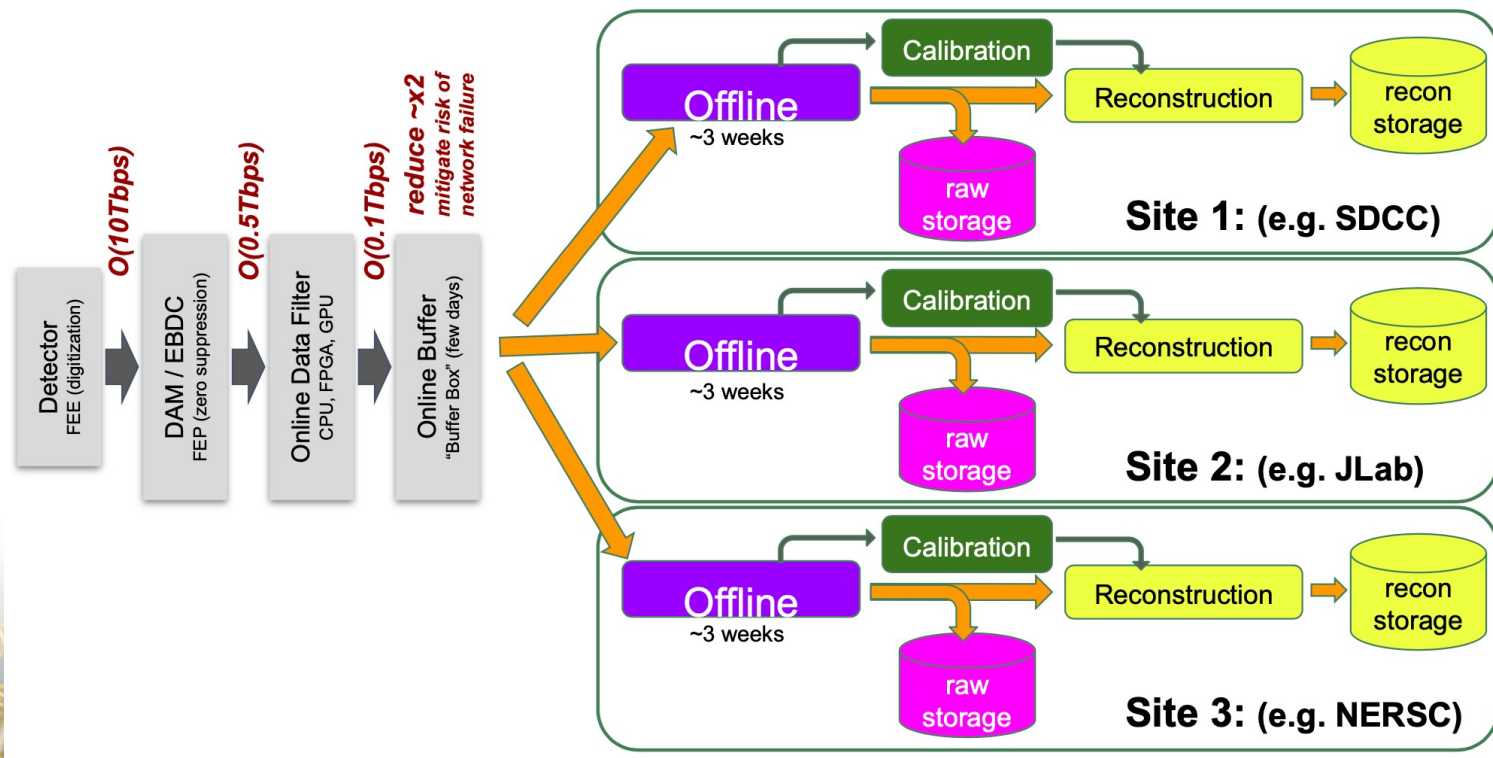
## Example:

Use some EBDC (Event Building/DataCompression) servers as a RAM buffer until Event ID processing can identify time windows that are important. Then filter data from the high rate detector we should keep.



# Boundary between Online and Offline

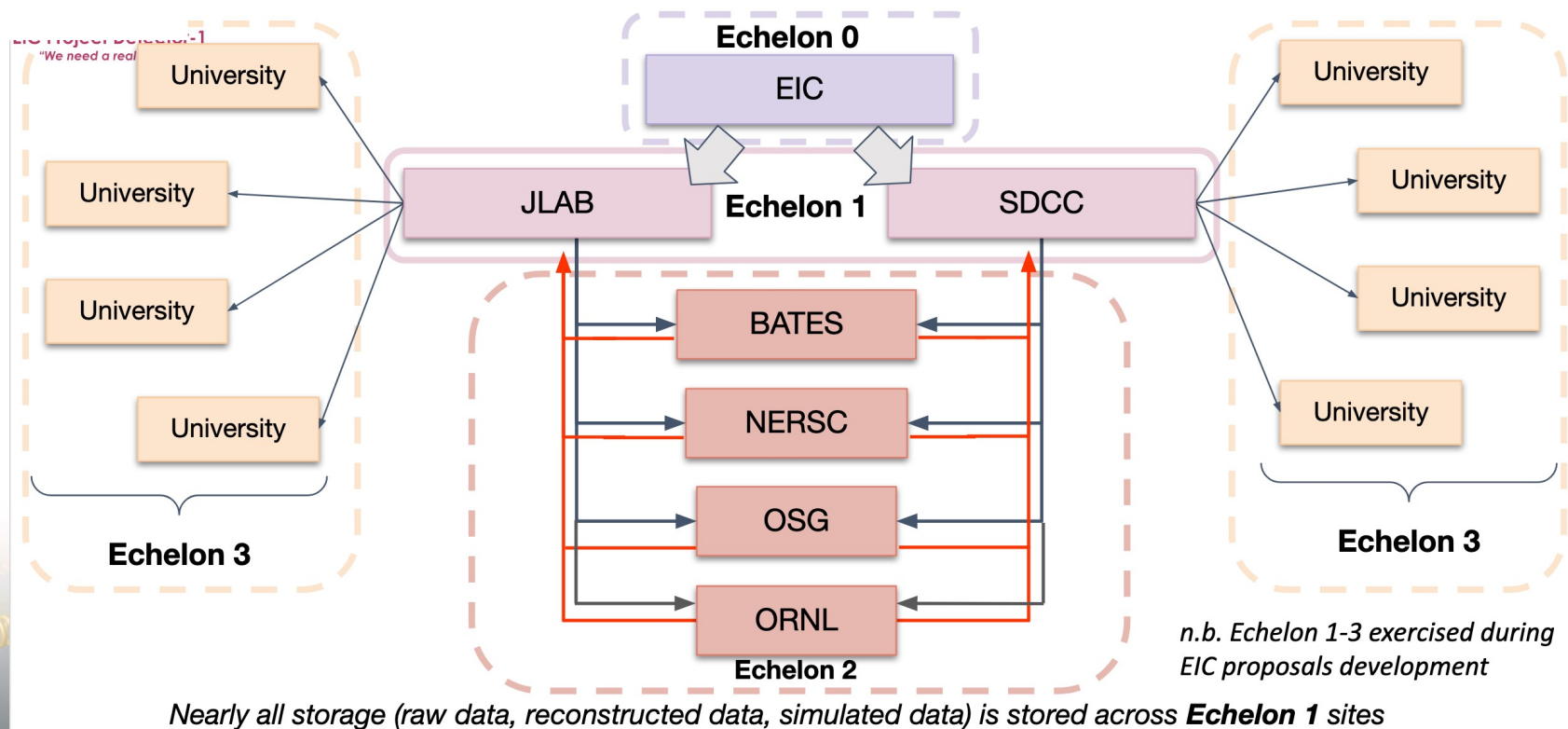
- Full understanding of the Online processing responsibilities and physical make-up is still being hashed out.
- We still require elements of the Offline Computing framework within the Online
- Online Storage (Buffer Boxes) are intended as a “pause” and a decoupling with further Offline processing .
- Offline buffering will allow several weeks for calibration and reconstruction.





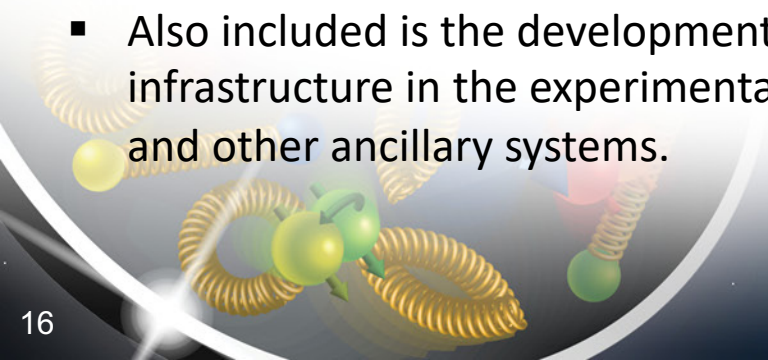
# Offline – EIC Butterfly Model

- Focus primary storage on Echelon 1 sites
- Reduces single points of failure
- Dynamically adjusts resource location depending on demand



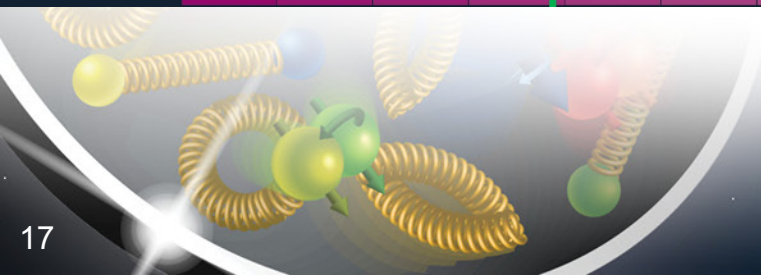
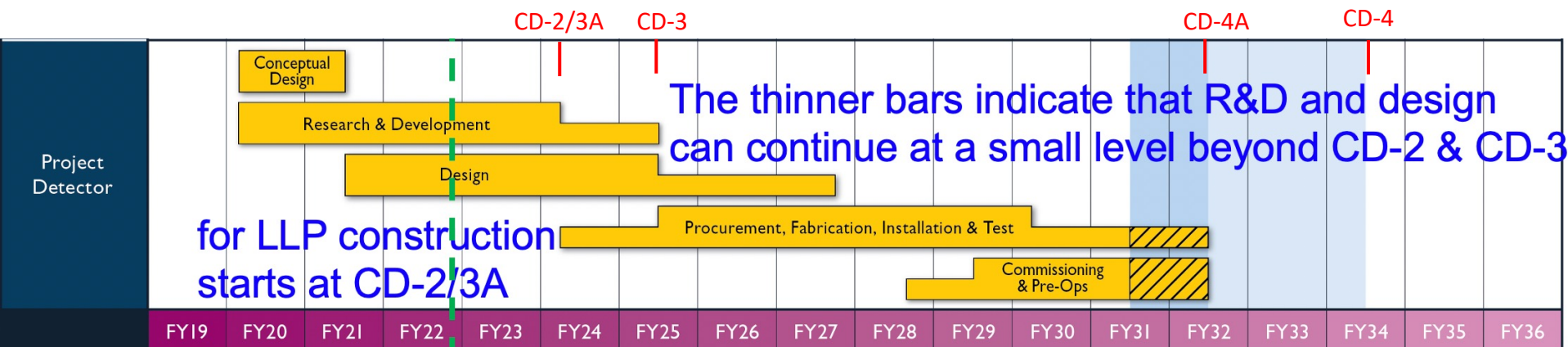
# Slow Control Integration

- There will be many slow control and monitoring systems associated with the EIC collider and ePIC detector subsystems.
  - BPMs, magnets, detector biases, HV, gas flows, temps, pressures, etc...
- Design and implementation of these control systems driven primarily by the relevant subsystems.
  - We want to coordinate ePIC slow control as much as possible with the collider approach (still not finalized) – some SCADA type system.
  - sPHENIX currently supports Ignition and WinCC using UPC-UA.
- DAQ/Computing has defined responsibility for SC Integration (L4 WBS 6.10.09.2)
  - Databases for maintaining SC data for calibrations and online/offline processing
  - Manage SC data readout to synchronize with the physics stream data
  - Maintain Software tools and libraries
- Also included is the development and implementation of a general network infrastructure in the experimental hall and counting house to support slow controls and other ancillary systems.



# EIC DAQ/Computing schedule

- The DAQ and computing schedule is planned to be somewhat accelerated in relation to the full detector construction.
- A functional DAQ will be necessary for small scale detector testing as well as commissioning and pre-ops.
- Some consideration should be given to shifting procurements of COTS computing hardware (CPUs, GPUs etc.) to ensure we get the best we can for production operation.





# Summary

- A general picture of the scope, scale and technologies we expect to need for the EIC data acquisition and online computing reasonably clear at this stage.
- Most of the DAQ/Online will be COTS-based procurements
- We have a viable candidate for Front-end interface and stream management hardware (FELIX)
- We will benefit from an engaged community as well as existing systems being developed and in operation today.

