Ecal WG meeting summary

August 25th 2022

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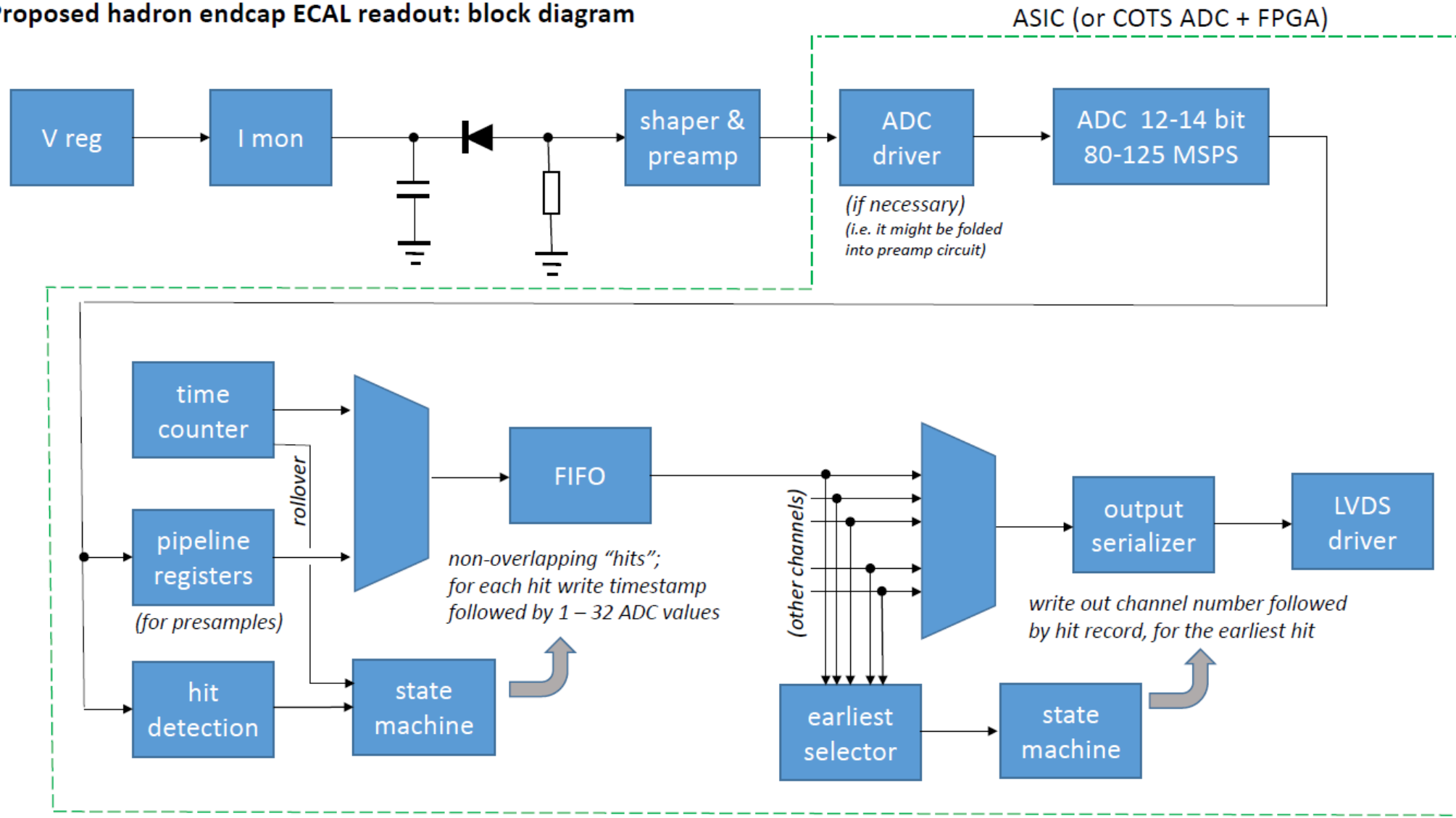
Summary

- 2 talks about readout of calorimeter
  - STAR FCS based (Gerard Visser) https://indico.bnl.gov/event/15817/contributions/67322/attachments/42938/72182/hadron_endcap_ECAL_readout_20220824.pdf
  - HGCROC based https://indico.bnl.gov/event/15817/contributions/67323/attachments/42939/72184/20220824CalReadout.pdf

STAR FCS upgrade

Proposed hadron endcap ECAL readout: block diagram



ASIC option

Realization with ASIC (perhaps)

Pacific MicroCHIP Corp.

A 32 Channel ASIC for X- and Gamma-Ray Energy and Timing Measurement

Keywords: Event building, Streaming readout, X-ray detector readout, Gamma-ray detector readout

Technical Summary

Pacific Microchip Corp. has developed a power efficient 32-channel ASIC (1st generation) for X- and gamma-ray energy and timing measurement with a digital event building back-end.

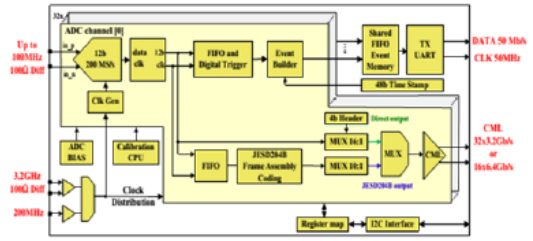


Figure 1. A block diagram of the ASIC.

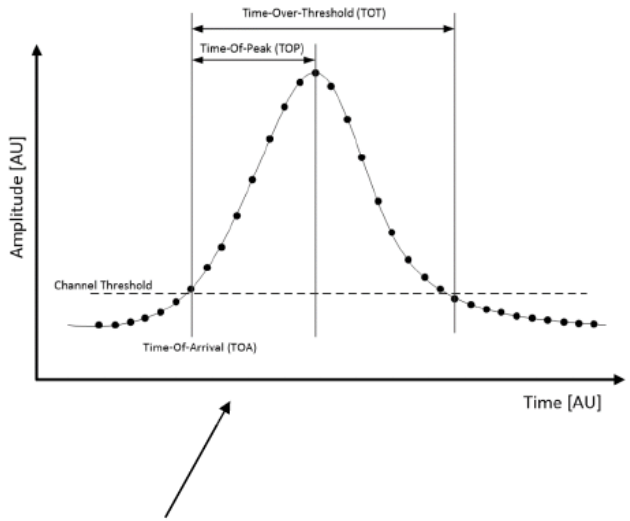
Figure 2. A chip photo (left), BGA package (center) and the

Targeted Operational Capabilities

The ASIC offers low power consumption (4.5mW/ch) combined with complex functionality required for signal digitizing and extracting of event related data (time of arrival, threshold, time of peak, peak value, time over threshold, etc.). This data is assembled into packets and shipped out through an UART interface. Specific parameters/capabilities:

- 32 independently operated channels
- Programmable sampling rate of 200/100/50 MS/s
- 1Vpp differential input swing
- Digitizing ENOB > 10-bit
- Input signal bandwidth > 0.2GHz
- Integrated 32ch event-building digital back-end
- Optional direct ADC output through JESD204B interface
- Event data packet output through UART interface
- Power consumption < 4.5mW/channel (JESD204B is off)
- Total power with ADC data interface 880mW.
- I2C interface for ASIC control
- Chip layout footprint 7.8mm^2
- 15mm x 15mm 324 ball BGA package

Development Objectives & Milestones



- Price $39 /ch
- Output bandwidth 6.25 MB/s (not enough probably)
- Data clock sent separately (we rather have embedded)
- Hit record (in current design) 126 bits, comparable to our expectations. [Assume → buffering is about right.]
- All controls by I^{2}C – nice!

- In current design, samples are NOT stored except for peak value. They do time, TOT, and peak value/time. This is probably **not** good enough for us.
- There's a 2 month window (i.e. To ~Nov. 1st) to try to influence feature changes for new version of the chip. They are already thinking about BW improvement.

COTS option

Proposed hadron endcap ECAL readout: Cables / interfaces / mechanical

Clock/data cable per FEE board

- Four pair, some kind of thin ethernet cable (Ø 3.5mm)
  1. output data bit 0
  2. output data bit 1
  3. clock & sync input
  4. extra/tbd (or fast control, if needed; can be used for sync)
     - OR can be used for slow controls if not on power cable

Power & control multidrop cable (bussed up to 16 FEE boards, maybe more)

- 10, 14, or 20 wire standard 0.05" ribbon cable, IDC connectors
  - SDA and SCLK (to be optoisolated at remote I^2C master)
  - power (details TBD…)
  - external voltage reference (TBD/likely) for bias regulators at least

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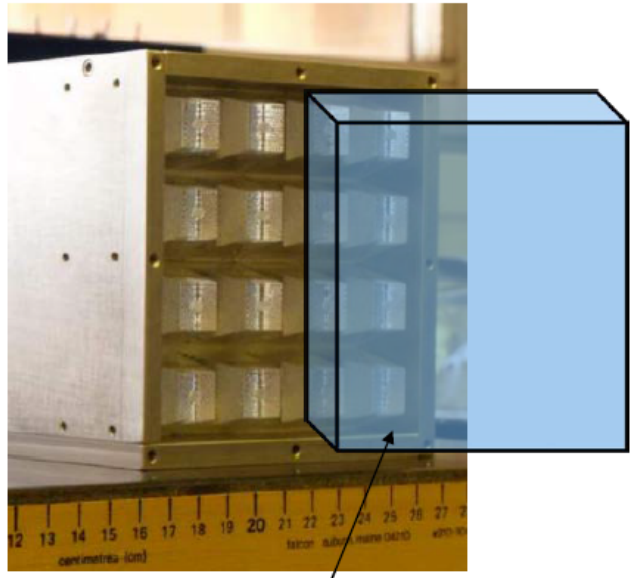
Acceptable power dissipation on FEE board?
100 mW/ch may be achievable with COTS implementation.
20 mW/ch may be achievable with optimal ASIC.
300 – 2000 W range for total power ~16k ch, will need liquid cooling but for this the power is reasonable



16 channel FEE assembly *(including SiPM carriers, interconnect, FEE PCB(s), **cooling**, and cable connectors and **cable space**)*

9.9 × 9.9 × 7? cm

My questions on our requirements…

live master table (Oleg)

EIC_Readout_Calo_v2

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Detector	Sub-system	T	Minimal Energy YR Table 10.6	Minimal Practical	Maximum Energy YR Inclusive	Signal Range	Capacitance	Single Channel Rate Maximum
Calorimetry								
	n-Hcal (KLM type) (10 la	(	500 MeV	300 MeV	20 GeV	10-200 pixels	60 pF (1.3 x 1.3 mm)	0.5 kHz
	p-EMCal	(	100 MeV	5 MeV	100 GeV	5-60k pixels	5.2 nF 4 SiPMs (6 x6 n	50 kHz
	LFHcal	(	500 MeV	300 MeV	100 GeV	50-20k pixels	2nF 6 SiPMs	50kHz
	p-HCal insert	(	TBD	TBD	100 GeV	10-200 pixels	60 pF	50 kHz
	b-Hcal (KLM Type) (5 lay	(	500 MeV	300 MeV	10 GeV	10-200 pixels	60 pF (1.3 x 1.3 mm)	1 kHz

https://docs.google.com/spreadsheets/d/18Cl2xWAC8HqhZmD1MT8JZWSVGm_WZQN2PT92f5KjNaE/edit#gid=2090491516

Assuming the basic context that we simply shape the pulse and sample N points on a waveform

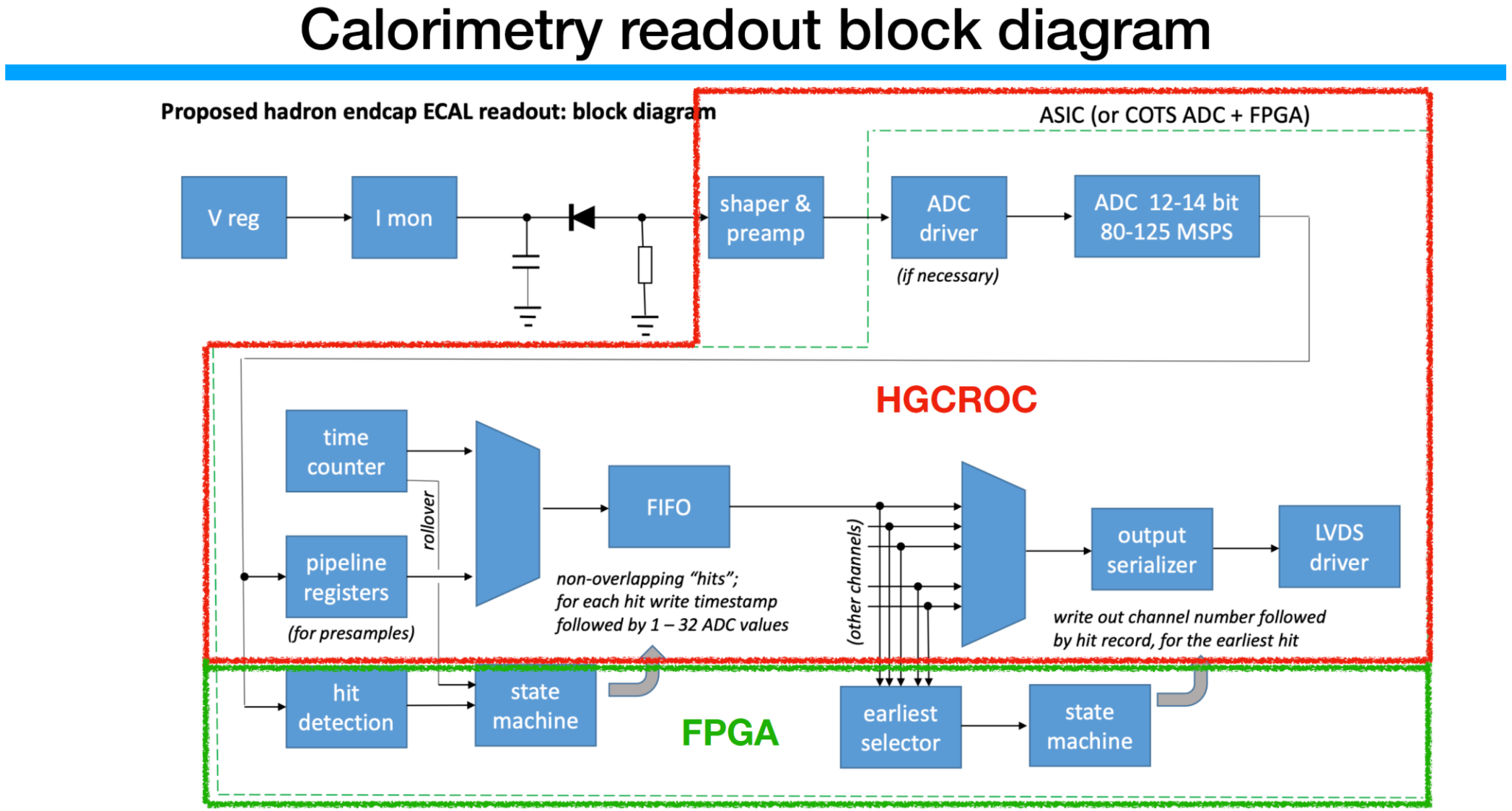
1. *How many samples should be used?* (What's the experience from FCS analysis, other experiments?)
2. Shall the sampling clock be related to bunch crossing clock 98.5 MHz (e.g. /2 is perhaps nice)?
   - Probably not essential. But *using a related clock avoids having to cross-reference timestamps* downstream, though that should be feasible.

More general questions

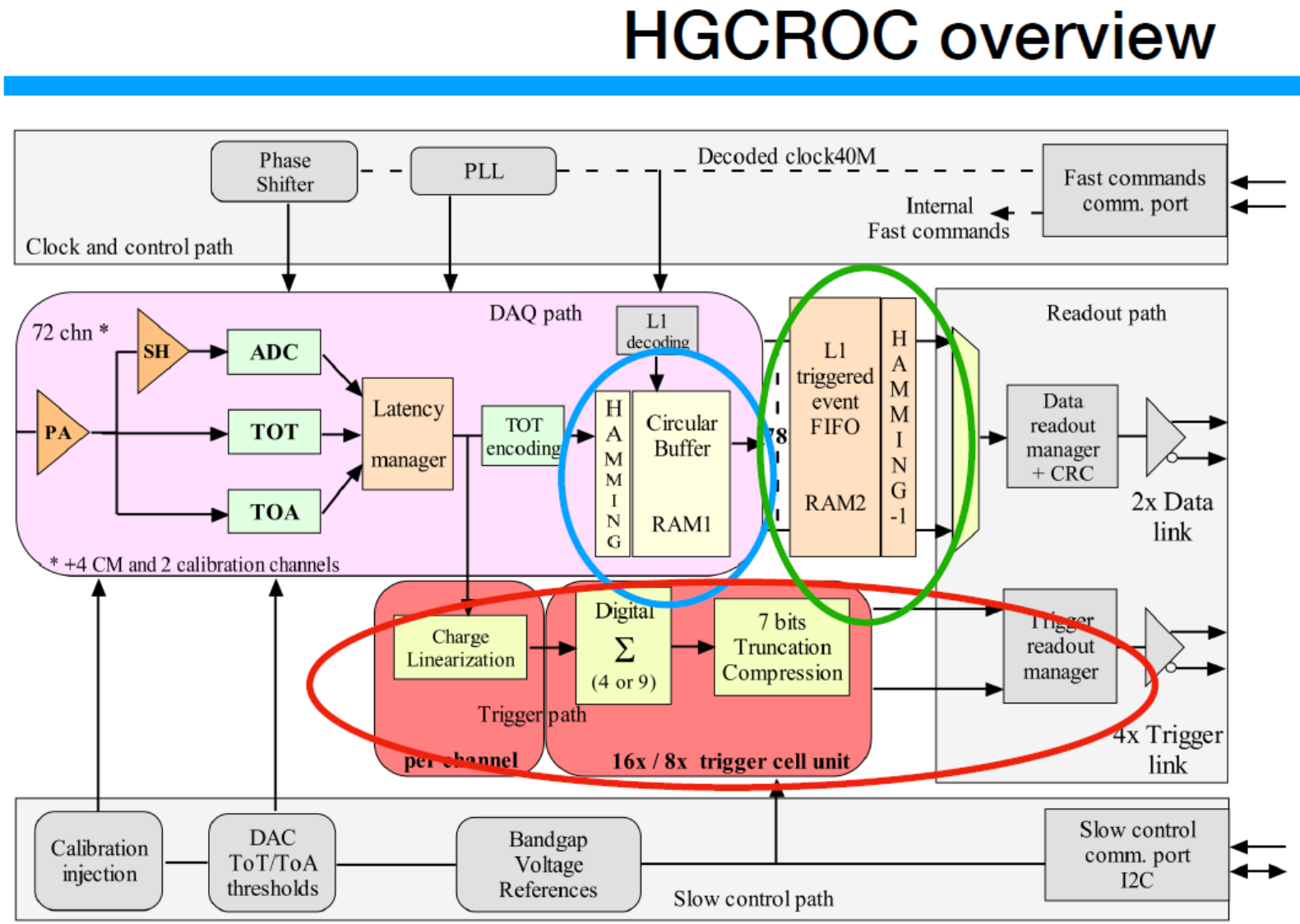
Note: 20 log10(100GeV/5MeV) = **86** dB
Even 14-bit ADC will not do that in one sample…

3. *What linearity is needed?* Is better than 1% simply overkill?
4. The signal range has been specified (5 MeV to 100 GeV). But *what is the acceptable electronics noise contribution?* In particular this question covers what bit resolution for digitizing. Is 14 bits relevant, if it is affordable?
5. How many bits of timestamp need to be sent from FEE to DAQ (i.e. on the fiber link)?
   - Note, the on-detector timestamp may [will] be shorter and augmented on the "Off-detector FE" board
6. *Does 7 cm space for SiPM + FEE + cables sound good enough?*

HGCROC based



HGCROC



Trigger data:
- 4 or 9 channels are summed up
- Sent as a 64-bit word out on 4 trigger links

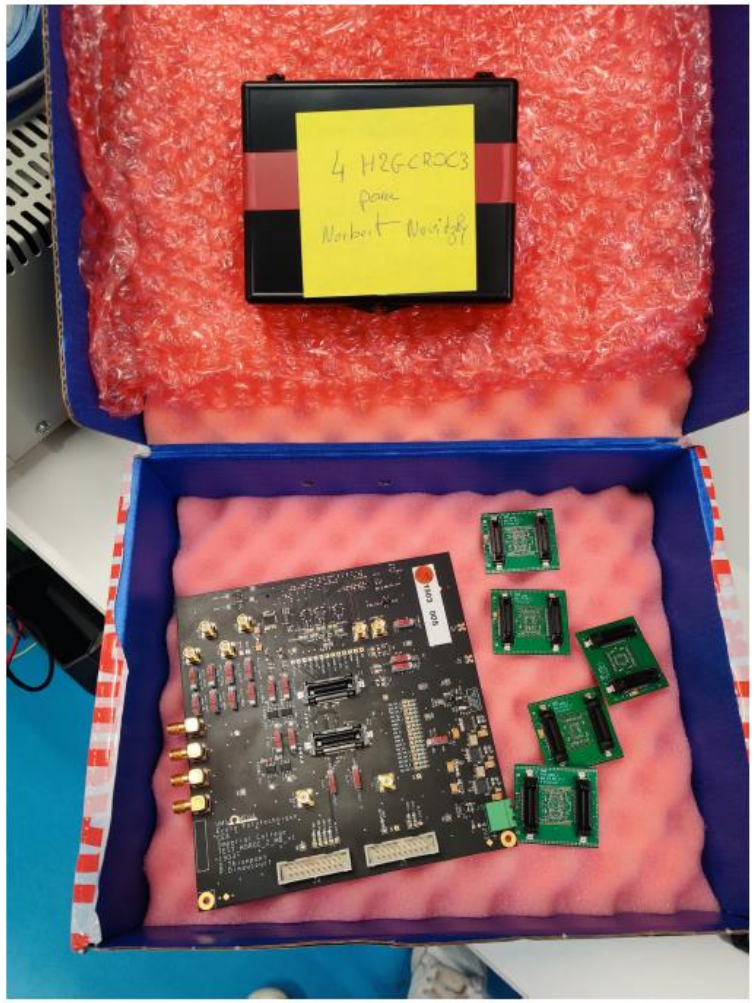
RAM1:
- Circular buffer of 512 samples
- 512 x 25 ns = 12.5 µs total
- L1 needed to shift to the RAM2
  - We can shift 3-4 samples

RAM2:
- Circular buffer of 32 samples
- Space for 8-10 events
- Max readout speed 960 kHz

Expected hit rate is 50kHz in forward region, with 4 samples it would be 200 kHz readout speed (1/4 of the capability)

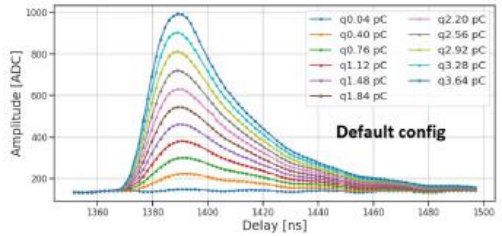
Running at 100 MHz

Signal shape



Received the sample of the HGCROCv3

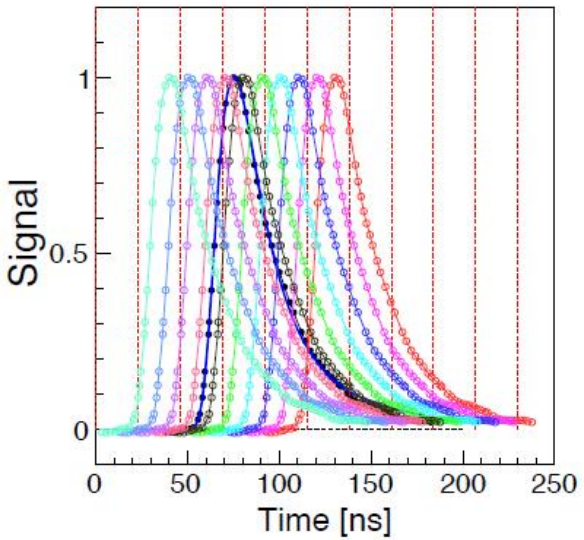
- Testboard
- 4 Chips



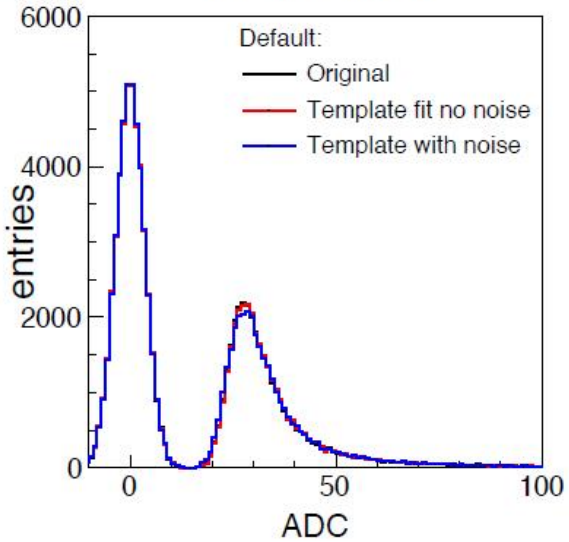
Collisions can happen every 10 ns:

- HGCROC samples at 40 MHz clock speed (25ns)
- Realistic noise added

Strategy is to collect 3-4 samples of the default shape



3 Samples could sufficiently reconstruct the MIP peak



Summary

ADC solution	ASIC solution
Streaming	(Virtual) Streaming
60 mW/ch (ADC) + FPGA	4-20 mW/ch
6-10$/ch (ADC)	1-2$/ch (Hgc), 40$/ch (PacC)
1000 small FPGA	~80 FPGA
Is it RadHard? 15 year?	RadHard, PacChip?
What cables are needed?	What cables are needed?

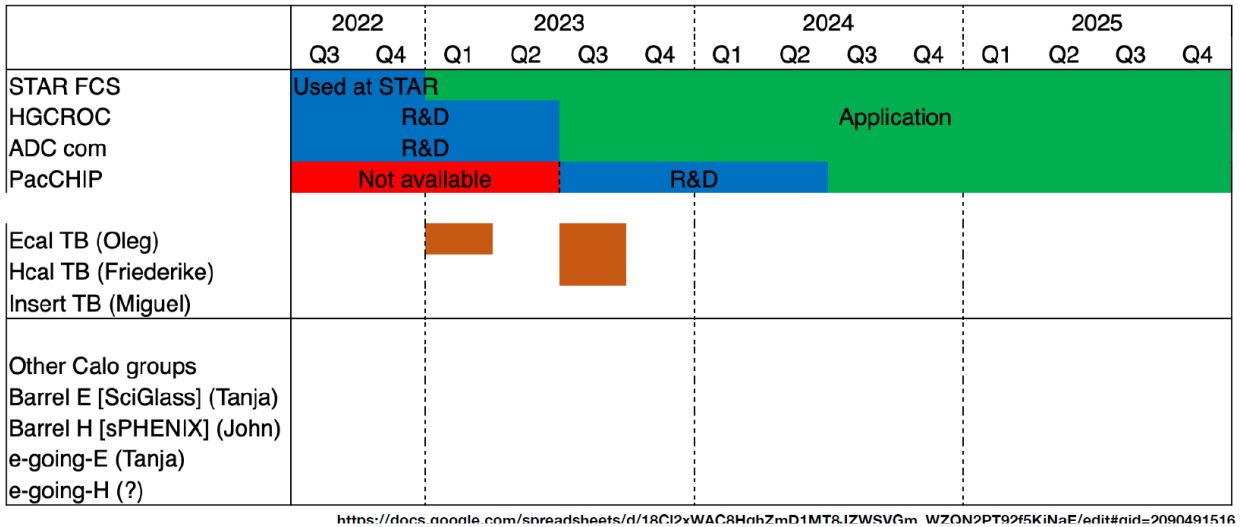
Possibility to have also outside readout card solution for calorimeters

We will collect the needs and wishes for other calorimeters readouts also

We probably need two parallel R&D developments in the RD109:

- ADC + FPGA on a small board on detector:
  - Cooling
  - RadHard
- HGCROC + FPGA:
  - 40 MHz clock
  - Shaper setup if needed
- PacChip:
  - Availability
  - Modifications, additions

We further investigate other ASIC possibilities, VMM, from Panda, etc.



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Energy range

able

EIC_Readout_Calo_v2

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	b-Hcal (KLM Type) (5 lay	(	500 MeV	300 MeV	10 GeV	10-200 pixels	60 pF (1.3 x 1.3 mm)	1 kHz
Update needed	h-Ecal (SciFi part)	(	50 MeV	2.5 MeV	50 GeV	00-40k pixels	5.2 nF 4 SiPMs	1 kHz

m/spreadsheets/d/18Cl2xWAC8HqhZmD1MT8JZWSVGm_WZQN2PT92f5KjNaE/edit#gid=2090491516

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Can put like 3 pixels for EMCAL ? Increase gain for others with 200 pixels

Discussion

- Alphacore ?
- NALU HDSOC cost comparison
- VMM ? Bit resolution 11 bit only
- SALSA ?

- R&D plan from Oakridge, what is process to get money ? How does eRD109 work (is eRD109 only ASIC ?)

Conclusion

- 2 options
  - FCS upgrade
    - Safe option
    - More space
    - Cables
    - Power
  - ASIC
    - HGCROC possible candidate (seems working for imaging calorimeter too – TBC)
    - ASIC development more risky
      - Lower power
      - Less cables
- Two path for R&D, E&D, other options (HDSOC, EICROC…) : how funding works (eRD109 or calorimeter)? Might have guidance after DAQ electronics / review