Discussion of on-detector digitizing readout for hadron endcap ECAL (and possibly others)

Potential recipe…

1. Take STAR FCS readout as a starting point
2. Shoehorn it onto the detector (either with or w/o ASIC’s)
3. Make it stream

G. Visser
Indiana University
8/24/2022 EPIC Calor. Meeting

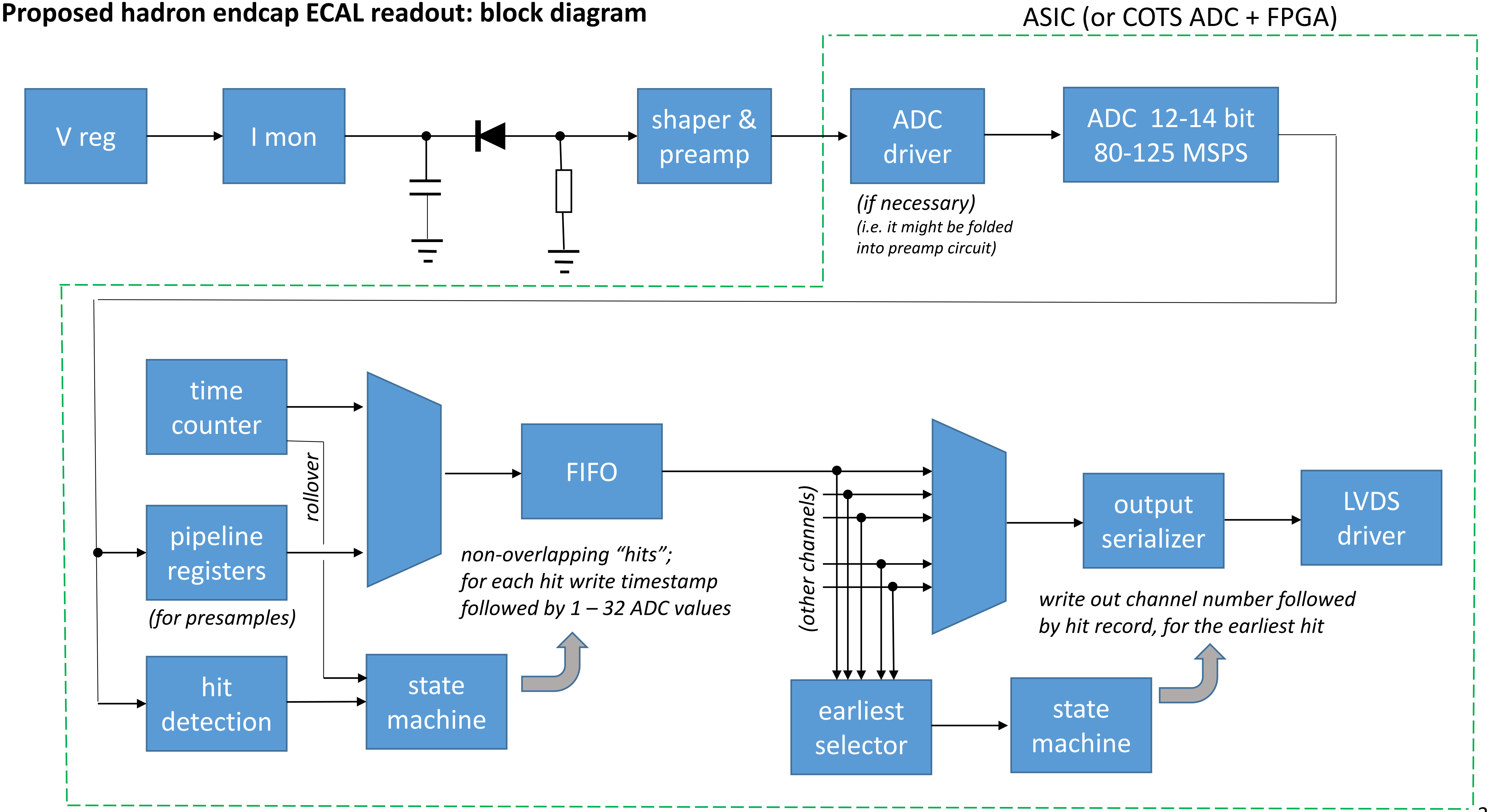
FCS readout essentials in one slide (for some detail see backup slides)

- Integrated precision SiPM bias and temperature compensation – stable gain
- Low impedance loading of SiPM – stable and linear gain
- Some shaping before amplification – stable and linear gain
- Low noise preamp
- Fully DC coupled – stable baseline
- Digitize waveform (in particular 12 bit 80 MSPS, but something similar 12-14 bits for EPIC)
- Everything then follows based only on the short (like 10 sample) waveform records of the hits
  - In STAR, triggered readout followed by ZS, then waveforms to DAQ file
  - For EPIC, streaming readout of hit records
- *Simplicity* of the hardware as much as possible
- Especially *simplicity* of the cables and interfaces on detector
  - Slow controls: Bussed I^2C to multiple FEE

The differences? (EPIC vs STAR)

- Digitize on the detector, to reduce the size (especially) and cost of cables
- *If feasible,* use an ASIC, *expecting* cost and power to be superior

Proposed hadron endcap ECAL readout: block diagram



Proposed hadron endcap ECAL readout: data format, size, rates

Output data format (per hit)

1. Timestamp (24? bits)
2. Channel number 4 bits
3. ADC data N*12 bits (N*14), 1≤N≤32 (N≤10 for physics running)

Hit is fixed length, say 148 bits or less for physics running
If no hit to send, send a suitable variable-length idle sequence on output link to be dropped by receiver; idle format designed so that next hit data start is identifiable.

Having the timestamp first simplifies (IMHO) merging data downstream in time-ordered way.

Hit rate up to 50 kHz average on all channels simultaneously.
→ Output data rate up to 118.4 Mb/s (14.8 MB/s).

Two "lanes" LVDS running 75 Mb/s should be fine to support that.
Possibly some simple scheme with embedded clock.
Possibly/likely also using 8B/10B encoding. That will support up to 120 Mb/s.

No buffer is needed on output of FEE, it *never* waits to send.
Per-channel buffers only need to remove fluctuation in rates. How deep they need to be to avoid dropping hits is a simple calculation. (I haven't done yet though.)
Of course, we also have to mark if we dropped any hits (add at least one more bit in datastream for that).

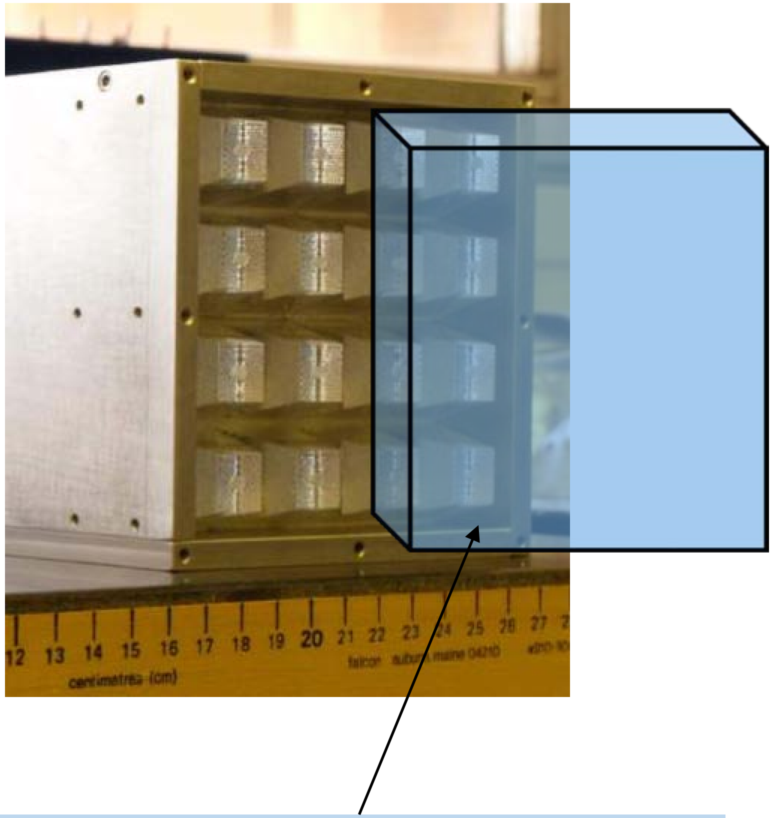
Proposed hadron endcap ECAL readout: Cables / interfaces / mechanical

Clock/data cable per FEE board

- Four pair, some kind of thin ethernet cable (Ø 3.5mm)
  1. output data bit 0
  2. output data bit 1
  3. clock & sync input
  4. extra/tbd (or fast control, if needed; can be used for sync)
     - OR can be used for slow controls if not on power cable

Power & control multidrop cable (bussed up to 16 FEE boards, maybe more)

- 10, 14, or 20 wire standard 0.05” ribbon cable, IDC connectors
  - SDA and SCLK (to be optoisolated at remote I^2C master)
  - power (details TBD…)
  - external voltage reference (TBD/likely) for bias regulators at least



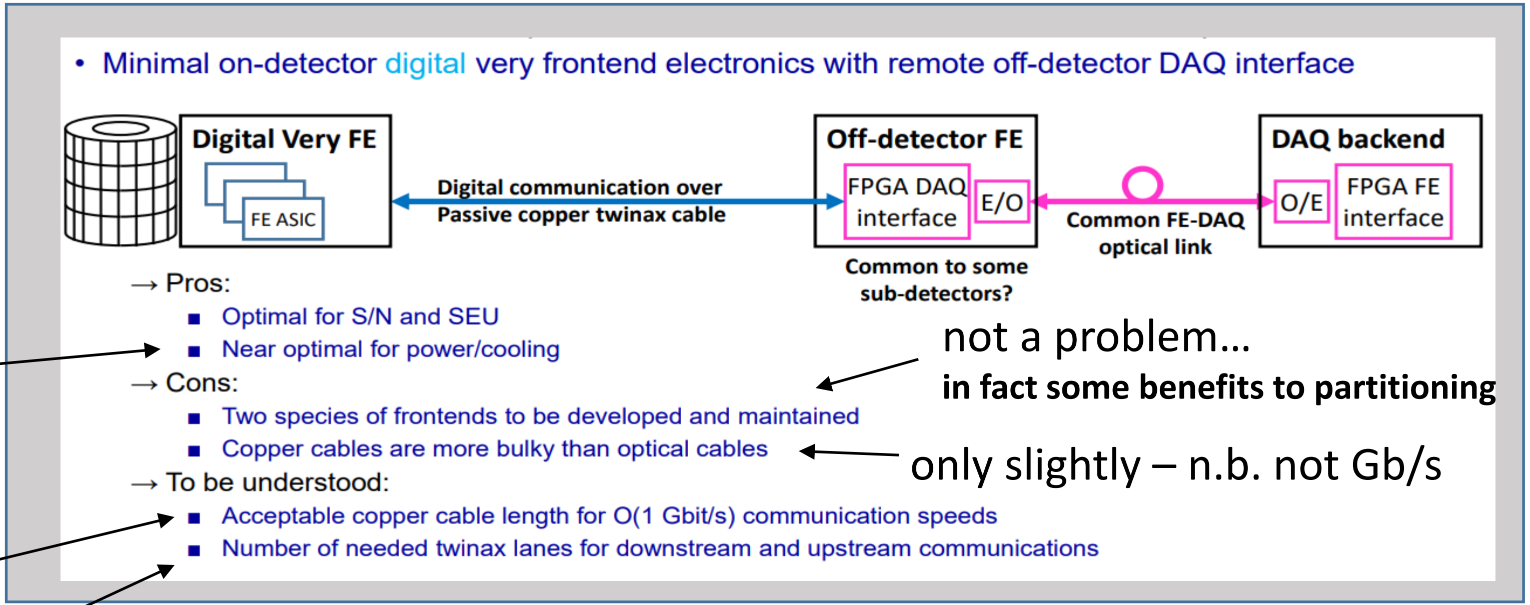
Acceptable power dissipation on FEE board?
100 mW/ch may be achievable with COTS implementation.
20 mW/ch may be achievable with optimal ASIC.
300 – 2000 W range for total power ~16k ch, will need liquid cooling but for this the power is reasonable

16 channel FEE assembly *(including SiPM carriers, interconnect, FEE PCB(s), **cooling**, and cable connectors and **cable space**)*

9.9 × 9.9 × 7? cm

Proposed hadron endcap ECAL readout: How does this fit in the plan?

(Jeff Landgraf, DAQ WG report 6/24)



This is very important!

not a problem…
in fact some benefits to partitioning

only slightly – n.b. not Gb/s

100 ft should work
n.b. it's not Gb/s
15 MB/s per FEE

2 – 3 per FEE
4690 for H E ECAL
use 98 "Off-detector FEE" boards (16 FEE each), 98 optical links (running 237 MB/s each)
[In 8/18 DAQ WG meeting, JL shows 400 links… we're within plan scale]

Slow controls: Through "Off-detector FEE" board. Either bussed on power cable or point to point through data cable, TBD. Either way is feasible.

Feature extraction or other data reduction in "Off-detector FEE" if it is needed.

Realization with standard COTS ADC + FPGA

$10 per channel, 10.4 mm^2 PCB area per channel
same chip as on STAR DEP

Octal, 12-Bit, 40/80 MSPS, Serial LVDS, 1.8 V Analog-to-Digital Converter

Data Sheet **AD9637**

FEATURES 60 mW/ch 71.5 dB SNR

- Low power: 60 mW per channel at 80 MSPS with scalable power options
- SNR = 71.5 dBFS (to Nyquist)
- SFDR = 92 dBc (to Nyquist)
- DNL = ±0.4 LSB (typical), INL = ±0.5 LSB (typical)
- Serial LVDS (ANSI-644, default)
  - Low power, reduced signal option (similar to IEEE 1596.3)
- Data and frame clock outputs
- 650 MHz full power analog bandwidth
- 2 V p-p differential input voltage range
- 1.8 V supply operation

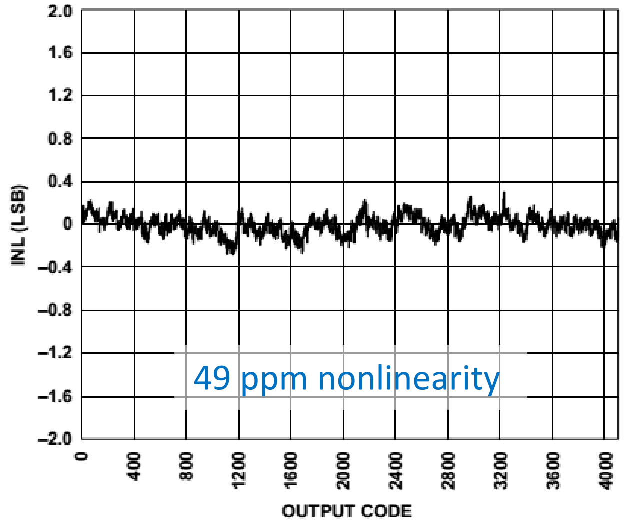
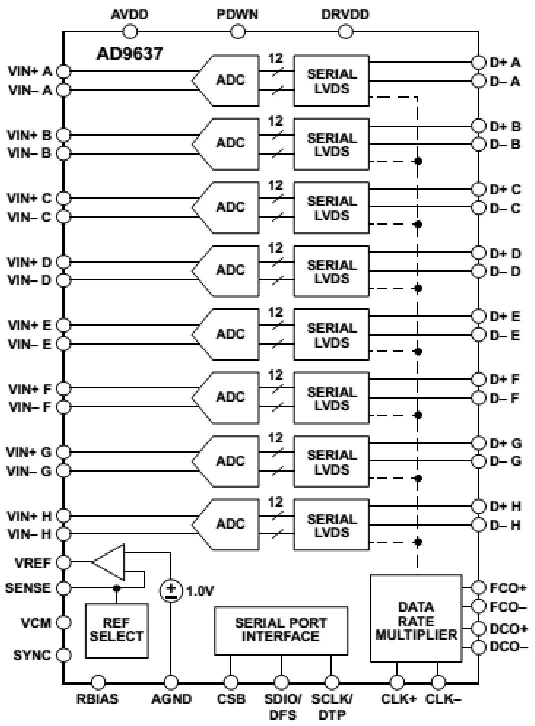


Figure 19. INL, f_{IN} = 9.7 MHz, f_{SAMPLE} = 80 MSPS

FUNCTIONAL BLOCK DIAGRAM



$10 per channel, 6.4 mm^2 PCB area per channel

16 Channel, 14-Bit, 65 MSPS, Serial LVDS, 1.8 V ADC

Data Sheet **AD9249**

FEATURES 58 mW/ch 75 dB SNR

- Low power
  - 16 ADC channels integrated into 1 package
  - 58 mW per channel at 65 MSPS with scalable power options
  - 35 mW per channel at 20 MSPS
- SNR: 75 dBFS (to Nyquist); SFDR: 90 dBc (to Nyquist)
- DNL: ±0.6 LSB (typical); INL: ±0.9 LSB (typical)
- Crosstalk, worst adjacent channel, 10 MHz, −1 dBFS: −90 dB typical
- Serial LVDS (ANSI-644, default)
  - Low power, reduced signal option (similar to IEEE 1596.3)
- Data and frame clock outputs
- 650 MHz full power analog bandwidth
- 2 V p-p input voltage range
- 1.8 V supply operation

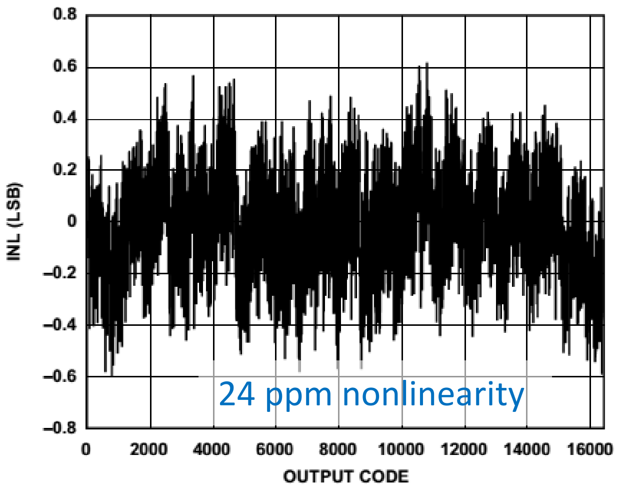


Figure 19. INL; f_{IN} = 9.7 MHz, f_{SAMPLE} = 65 MSPS

SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

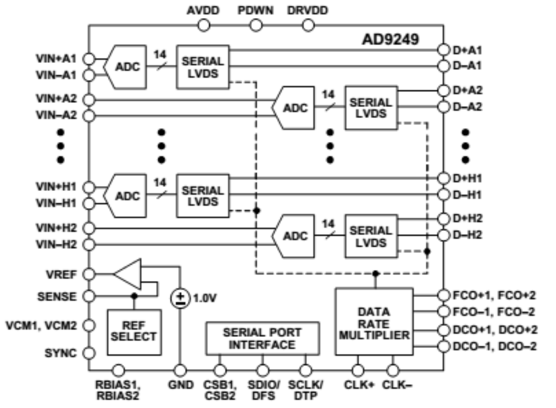


Figure 1.

Could run at ½ bunch crossing clock, 49.25 MHz
50 mW/ch

Realization with standard COTS ADC + FPGA, cont'd

$7.6 per channel, 25.2 mm^2 PCB area per channel

TEXAS INSTRUMENTS

www.ti.com

ADS5292

SLAS788B – NOVEMBER 2011 – REVISED JULY 2012

Octal Channel 12-Bit, 80 MSPS and Low-Power ADC

FEATURES

- Maximum Sample Rate: 80 MSPS/12-Bit
- High Signal-to-Noise Ratio
  - 70-dBFS SNR at 5 MHz/80 MSPS
  - 71.5-dBFS SNR at 5 MHz/80 MSPS and Decimation Filter = 2
  - 85-dBc SFDR at 5 MHz/80 MSPS
- Low Power Consumption
  - 48 mW/CH at 50 MSPS
  - 54 mW/CH at 65 MSPS
  - 66 mW/CH at 80 MSPS (2 LVDS Wire Per Channel)
- Internal and External References
- 1.8V Operation for Low Power Consumption
- Recovery From 6-dB Overload within 1 Clock Cycle
- Package: 12-mm × 12-mm 80-Pin QFP

66 mW/ch 70 dB SNR

performance not as good – but it is cheaper

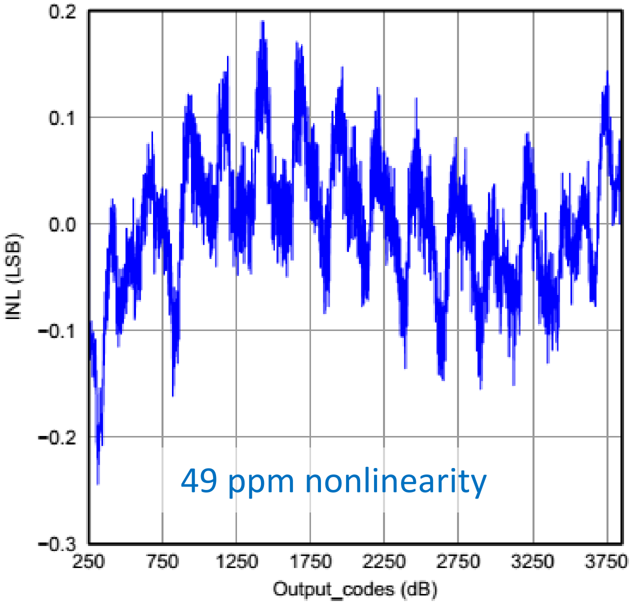
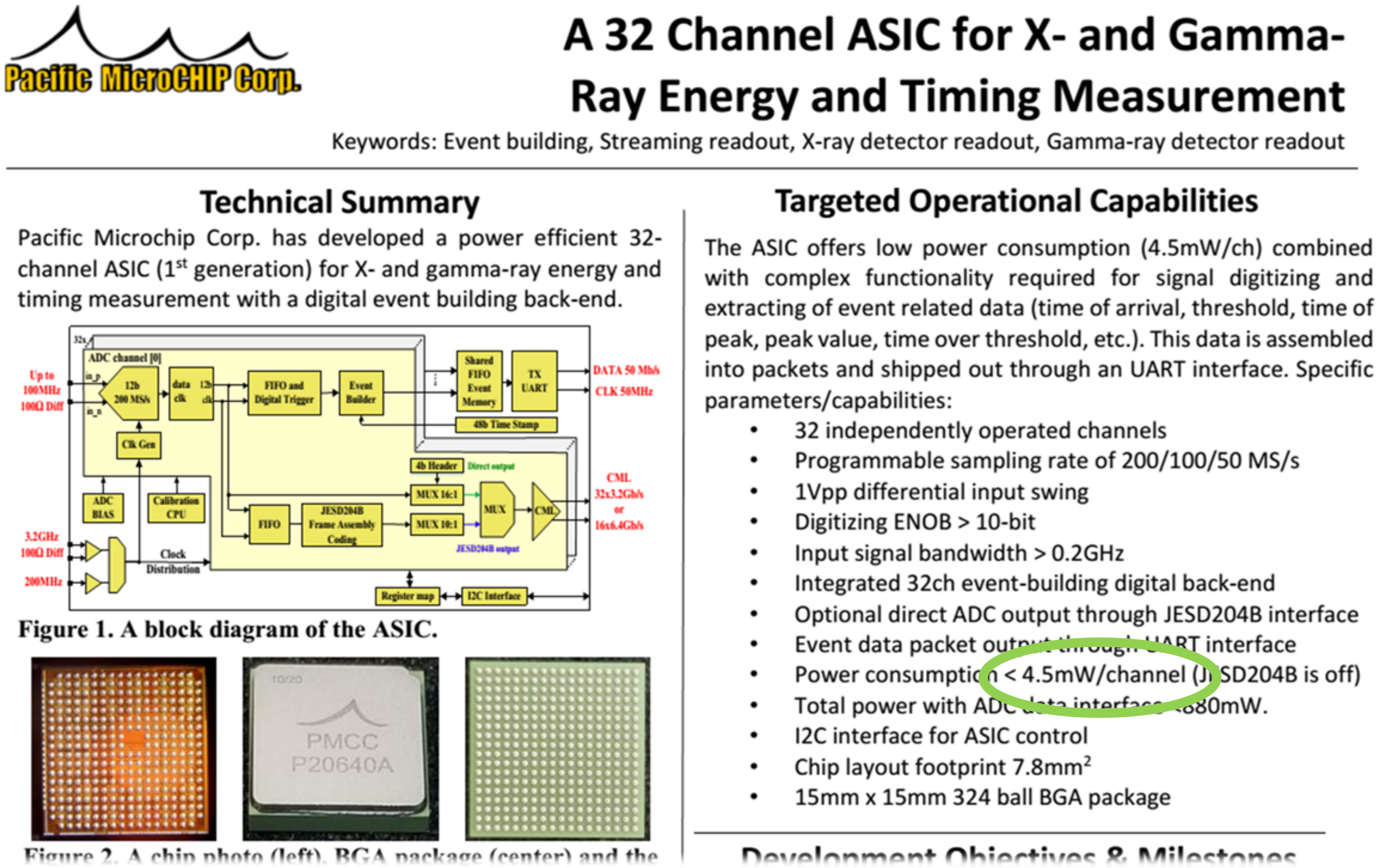


Figure 27. Integral Non-Linearity

still investigating other options, and FPGA options…

no doubt there will be new ones before we do a final design

Realization with ASIC (perhaps)



Pacific MicroCHIP Corp.

A 32 Channel ASIC for X- and Gamma-Ray Energy and Timing Measurement

Keywords: Event building, Streaming readout, X-ray detector readout, Gamma-ray detector readout

Technical Summary

Pacific Microchip Corp. has developed a power efficient 32-channel ASIC (1st generation) for X- and gamma-ray energy and timing measurement with a digital event building back-end.

Figure 1. A block diagram of the ASIC.

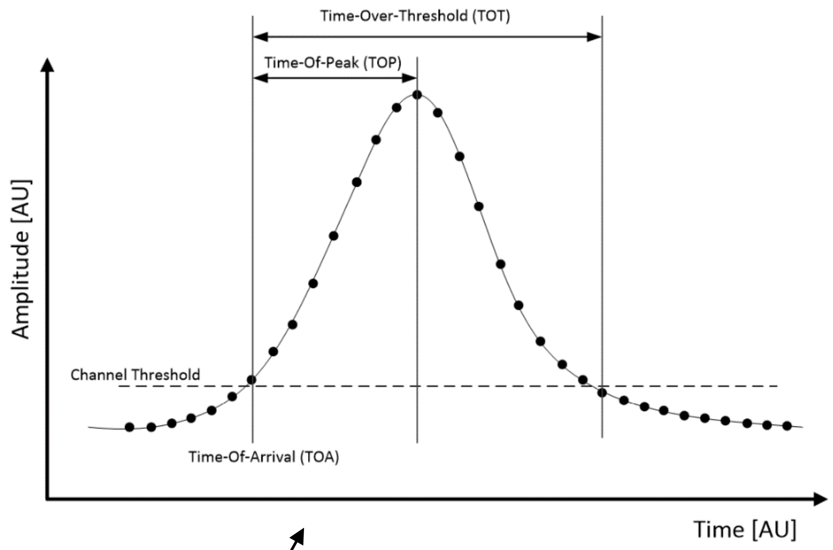
Figure 2. A chip photo (left), BGA package (center) and the

Targeted Operational Capabilities

The ASIC offers low power consumption (4.5mW/ch) combined with complex functionality required for signal digitizing and extracting of event related data (time of arrival, threshold, time of peak, peak value, time over threshold, etc.). This data is assembled into packets and shipped out through an UART interface. Specific parameters/capabilities:

- 32 independently operated channels
- Programmable sampling rate of 200/100/50 MS/s
- 1Vpp differential input swing
- Digitizing ENOB > 10-bit
- Input signal bandwidth > 0.2GHz
- Integrated 32ch event-building digital back-end
- Optional direct ADC output through JESD204B interface
- Event data packet output through UART interface
- Power consumption < 4.5mW/channel (JESD204B is off)
- Total power with ADC data interface <880mW.
- I2C interface for ASIC control
- Chip layout footprint 7.8mm^2
- 15mm x 15mm 324 ball BGA package

Development Objectives & Milestones



- Price $39 /ch
- Output bandwidth 6.25 MB/s (not enough probably)
- Data clock sent separately (we rather have embedded)
- Hit record (in current design) 126 bits, comparable to our expectations. [Assume → buffering is about right.]
- All controls by I^{2}C – nice!

- In current design, samples are NOT stored except for peak value. They do time, TOT, and peak value/time. This is probably **not** good enough for us.
- There's a 2 month window (i.e. To ~Nov. 1st) to try to influence feature changes for new version of the chip. They are already thinking about BW improvement.

My questions on our requirements…

live master table (Oleg)

EIC_Readout_Calo_v2

File Edit View Insert Format Data Tools Extensions Help

Detector	Sub-system	T	Minimal Energy YR Table 10.6	Minimal Practical	Maximum Energy YR Inclusive	Signal Range	Capacitance	Single Channel Rate Maximum
Calorimetry								
	n-Hcal (KLM type) (10 la	(	500 MeV	300 MeV	20 GeV	10-200 pixels	60 pF (1.3 x 1.3 mm)	0.5 kHz
	p-EMCal	(	100 MeV	5 MeV	100 GeV	5-60k pixels	5.2 nF 4 SiPMs (6 x6 n	50 kHz
	LFHcal	(	500 MeV	300 MeV	100 GeV	50-20k pixels	2nF 6 SiPMs	50kHz
	p-HCal insert	(	TBD	TBD	100 GeV	10-200 pixels	60 pF	50 kHz
	b-Hcal (KLM Type) (5 lay	(	500 MeV	300 MeV	10 GeV	10-200 pixels	60 pF (1.3 x 1.3 mm)	1 kHz
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

https://docs.google.com/spreadsheets/d/18Cl2xWAC8HqhZmD1MT8JZWSVGm_WZQN2PT92f5KjNaE/edit#gid=2090491516

Assuming the basic context that we simply shape the pulse and sample N points on a waveform

1. *How many samples should be used?* (What's the experience from FCS analysis, other experiments?)
2. Shall the sampling clock be related to bunch crossing clock 98.5 MHz (e.g. /2 is perhaps nice)?
   - Probably not essential. But *using a related clock avoids having to cross-reference timestamps* downstream, though that should be feasible.

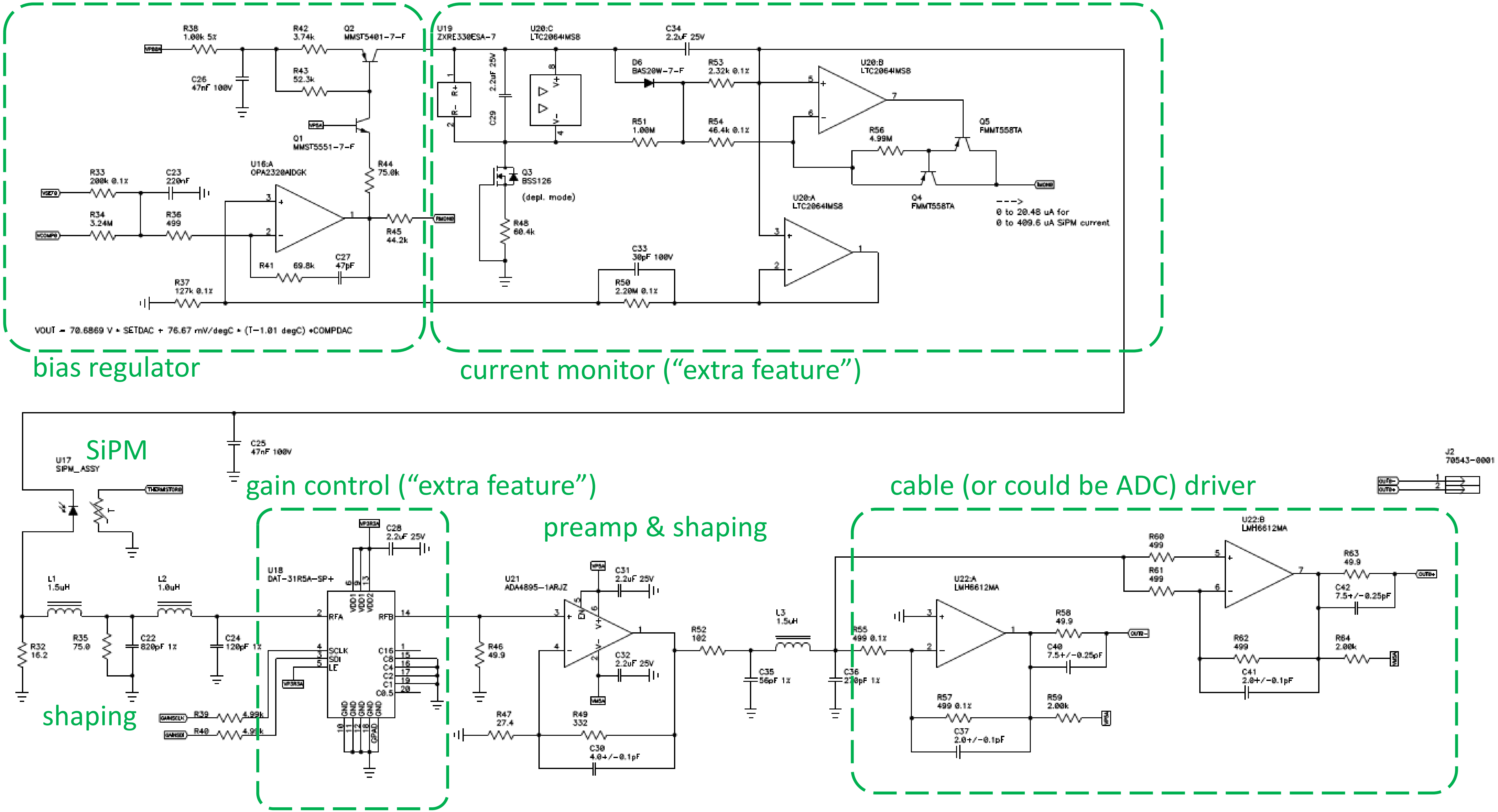
More general questions

Note: 20 log10(100GeV/5MeV) = **86** dB
Even 14-bit ADC will not do that in one sample…

3. *What linearity is needed?* Is better than 1% simply overkill?
4. The signal range has been specified (5 MeV to 100 GeV). But *what is the acceptable electronics noise contribution?* In particular this question covers what bit resolution for digitizing. Is 14 bits relevant, if it is affordable?
5. How many bits of timestamp need to be sent from FEE to DAQ (i.e. on the fiber link)?
   - Note, the on-detector timestamp may [will] be shorter and augmented on the "Off-detector FE" board
6. *Does 7 cm space for SiPM + FEE + cables sound good enough?*

BACKUP SLIDES

BACKUP – complete bias and signal schematic of one channel STAR FCS FEE



STAR FCS readout

Gerard Visser (Indiana U.)
8/3/2022

Overview of STAR FCS

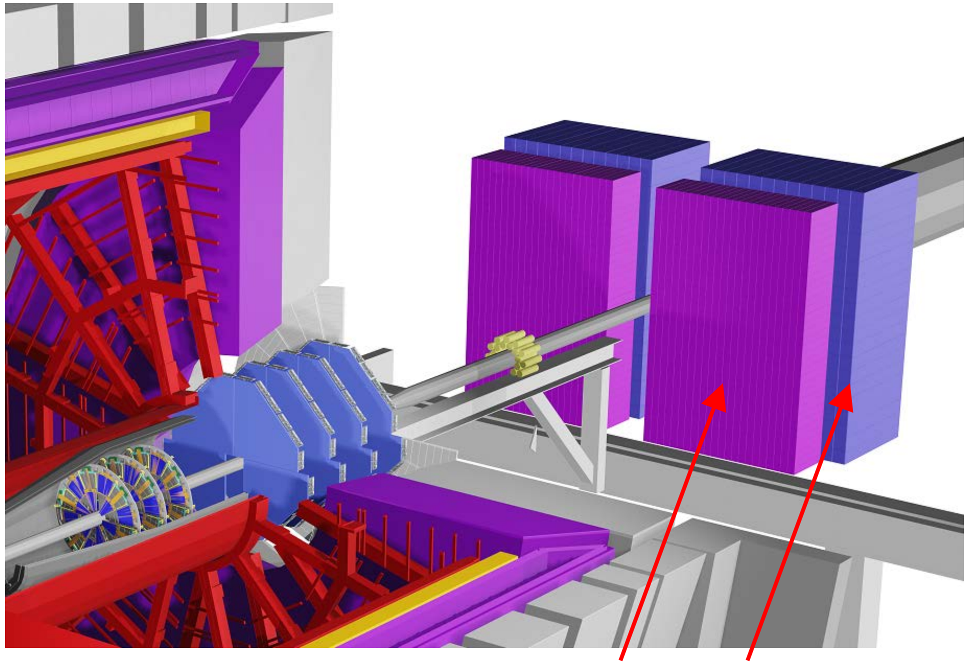
ECAL:

- 44 × 34 towers 5.6 cm square, split in two halves N/S of beampipe
- FEE boards 2 × 2 towers, 374 FEE boards (1496 ch)
- depth of readout (SiPM+FEE+cables) less than 5 cm

HCAL:

- 26 × 20 towers 10 cm square, split in two halves N/S of beampipe
- FEE boards 1 × 2 towers, 260 FEE boards (520 ch)
- depth of readout (SiPM+FEE+cables) less than 5 cm

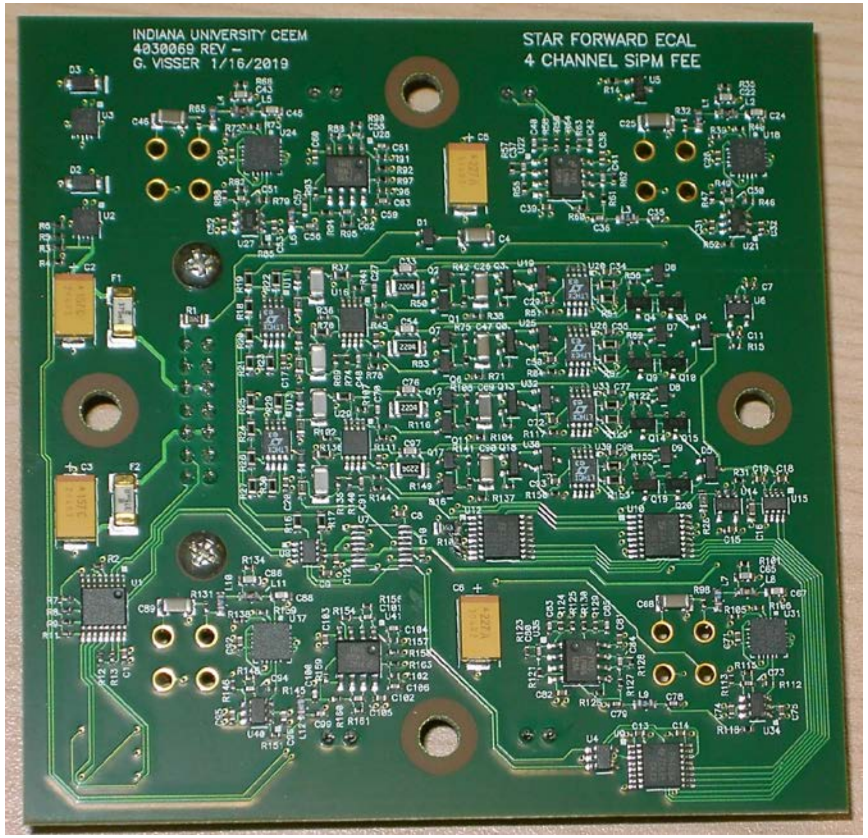
Rear view of Noth HCAL before FEE installation



Cutaway view of STAR with ECAL & HCAL

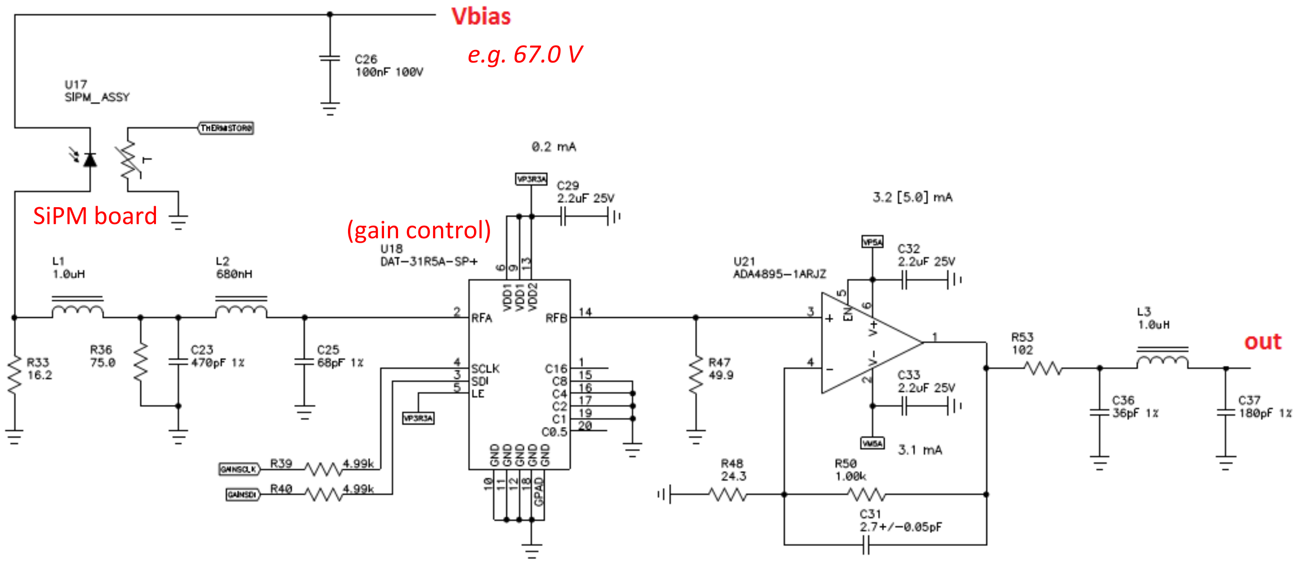
FCS readout design highlights

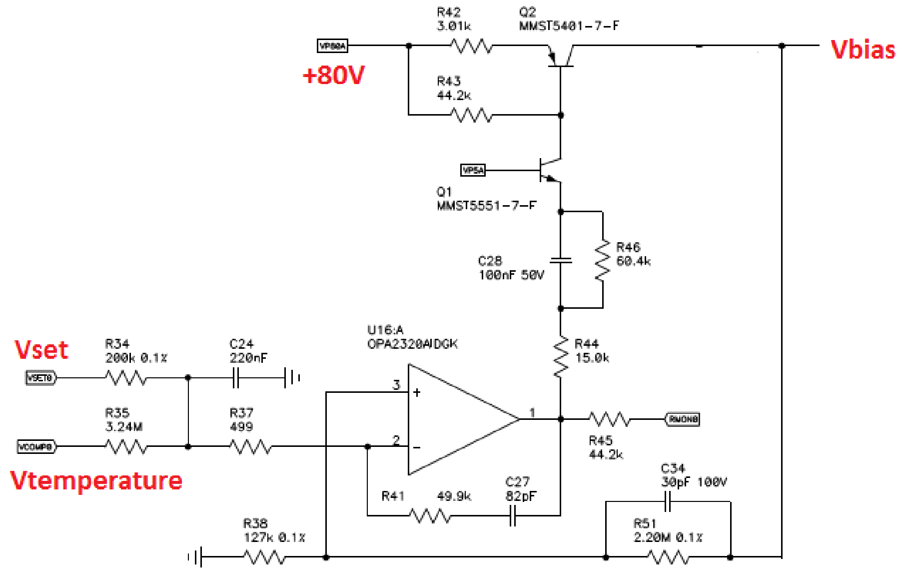
- Frontend amplifier and signal shaping on detector
- SiPM bias voltage control on detector
  - Including simple local analog temperature compensation
  - Including SiPM current monitoring
- Separate SiPM/thermistor and FEE boards
  - For ease of installation & lower cost to replace SiPM
- Services (**loosely regulated** +/-6 V, +80 V and I^2C controls) on low cost multidrop flat cable
- Differential analog signal output for reasons of size, cost, and noise immunity
  - Micro-ethernet cable on detector (~6 feet)
  - 3M loose pair CL2 cable the rest of the way to ADC’s (~80 feet)
- FEE board is magnetic tolerant – no magnetic cores used
- Waveform digitizer readout
  - “80” (75.06 = 8×RS) MSPS, 12 bits
  - Pulse arrives already shaped from FEE
    - DEP is **general purpose** (in fact we use also for preshower)
    - Shaping the pulse on detector makes best use of driver/cable dynamic range
  - Simply triggered readout (w/ ZS) in STAR – however DEP is **also intended as a development platform for streaming readout**



FEE Implementation – ECAL

FCS frontend and bias



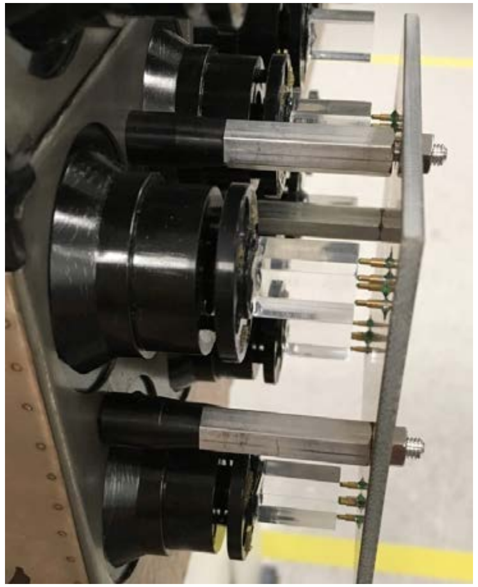


- ECAL 4×, HCAL 6× 3×3 mm^2 SiPM's
- SiPM with **small** load resistor, followed by voltage amplifier
  - for best possible linearity and gain recovery – *speed and linearity of the amplifier are not involved in sweeping charge out of SiPM*
- some shaping before amplification – so that amplifier *does not have to linearly follow pulse as fast as SiPM produces*
- more shaping after the amplifier – for noise limiting
- fully DC coupled through to ADC – *stable pedestals*
- for STAR we included gain control for better cosmic ray calibration; this could be omitted…

- simple but precise, low noise bias voltage regulator
- inherent current limiting – *no series resistor needed to protect SiPM*
  - more stable bias voltage → more stable gain
- fast recovery 3 µs to 2 mV after full scale signal pulse
- current monitor (not shown above) – optional, but useful!
- Vset and slope of Vtemperature set by DAC's

FCS FEE Connections

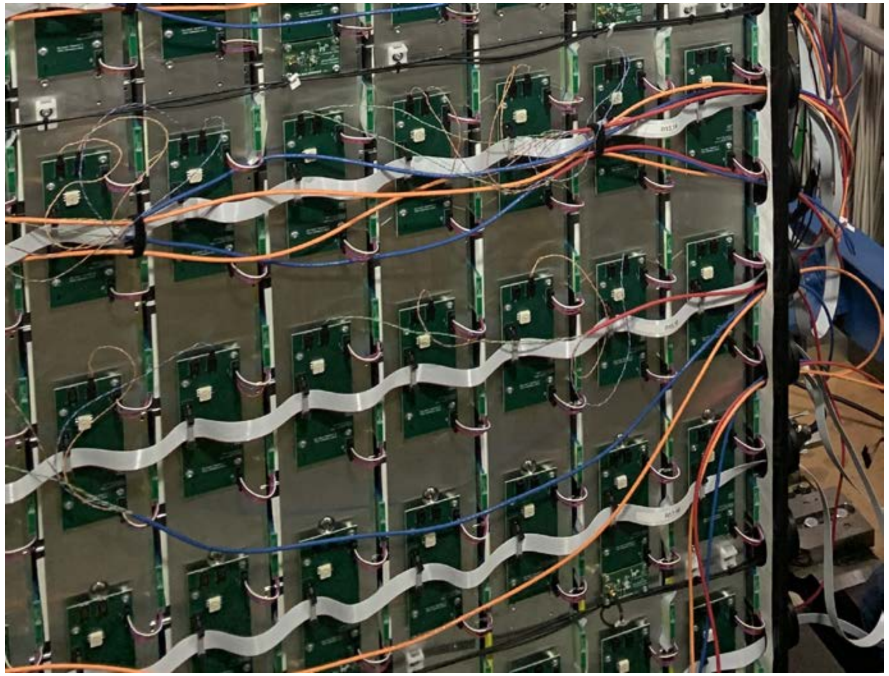
SiPM board per tower, glued to light guide. Connection from FEE by pogo pins. Large tolerance of transverse location (several mm). **Easy blind installation** (*once dimensions verified by fixture*).



Cooling of FEE: Air is drawn out from top of the enclosure. Enters at bottom, through baffles for light tightness.

Power inside detector: 180 mW/ch (e.g. ½ ECAL is 136 W)

Patchpanel boards on sides of detector: Transition to long signal cables. Group power rows into power groups. +80V power supplies.



HCAL: Same concepts, except short cable connection to SiPM board instead of pogo pin connection. Much more room than on ECAL.

DEP ADC Board – T. Ljubicic, BNL

- 32 channel 80 MSPS 12 bit ADC (4× P/N AD9637); pin compatible 14-bit available
- high CMR line receiver inputs (same design as GlueX ADC125 – G. Visser)
- FPGA on Trenz Module – easily upgraded
- 2× 3.2 Gb/s fiber links (≈ 460 MB/s effectively) to DAQ PC
- Expect ≈ 40 bits per hit for summary info (amplitude, time, etc.) for a streaming mode readout – max ≈ 2.9 MHz/channel hit rate
- This is "DEP ADC" – there is also "DEP IO" a trigger processor with fiber input instead of ADC
- DEP ADC also includes 2× opto-isolated I^{2}C masters used for FEE slow controls (on signal cable)