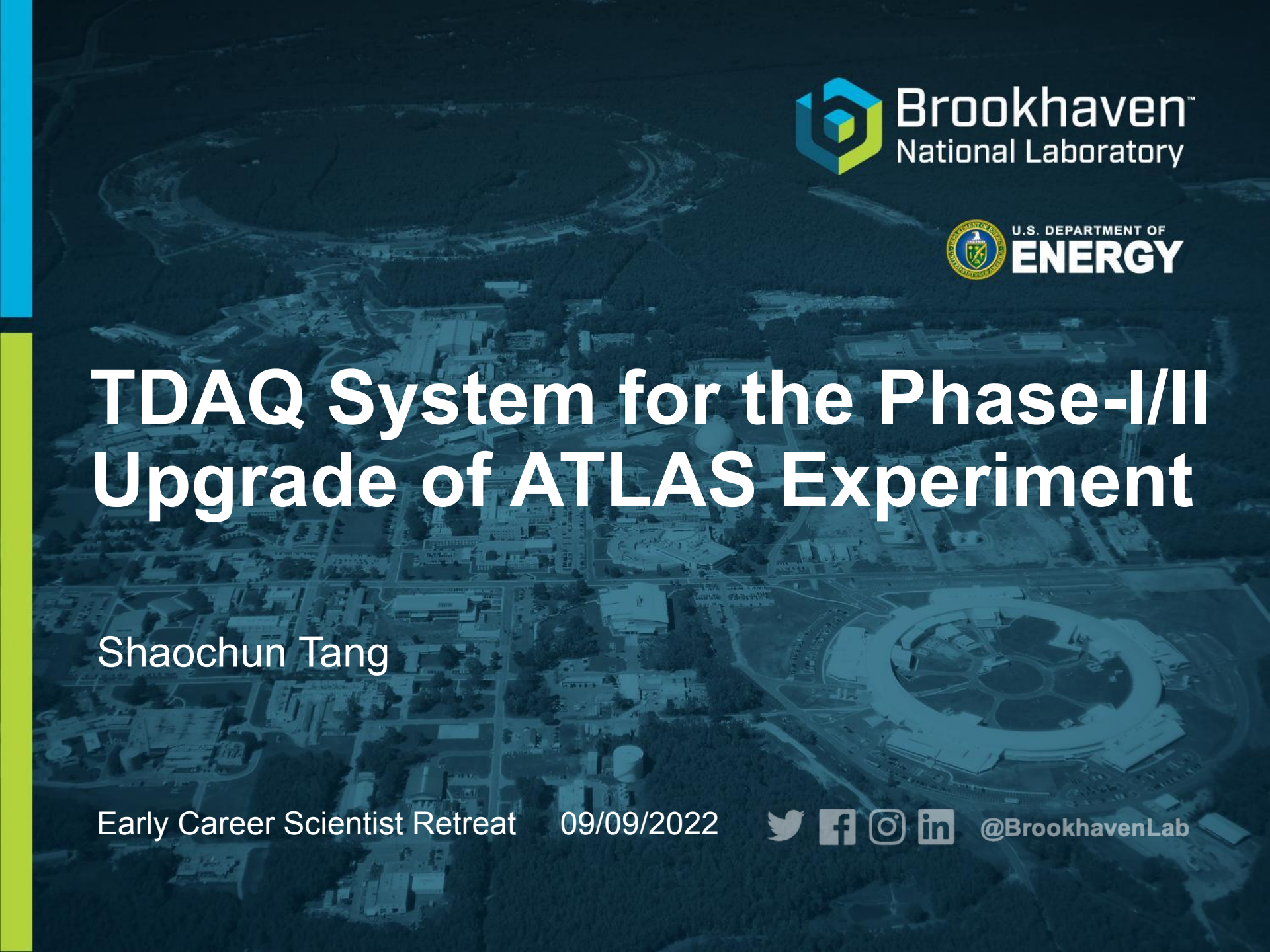


TDAQ System for the Phase-I/II Upgrade of ATLAS Experiment

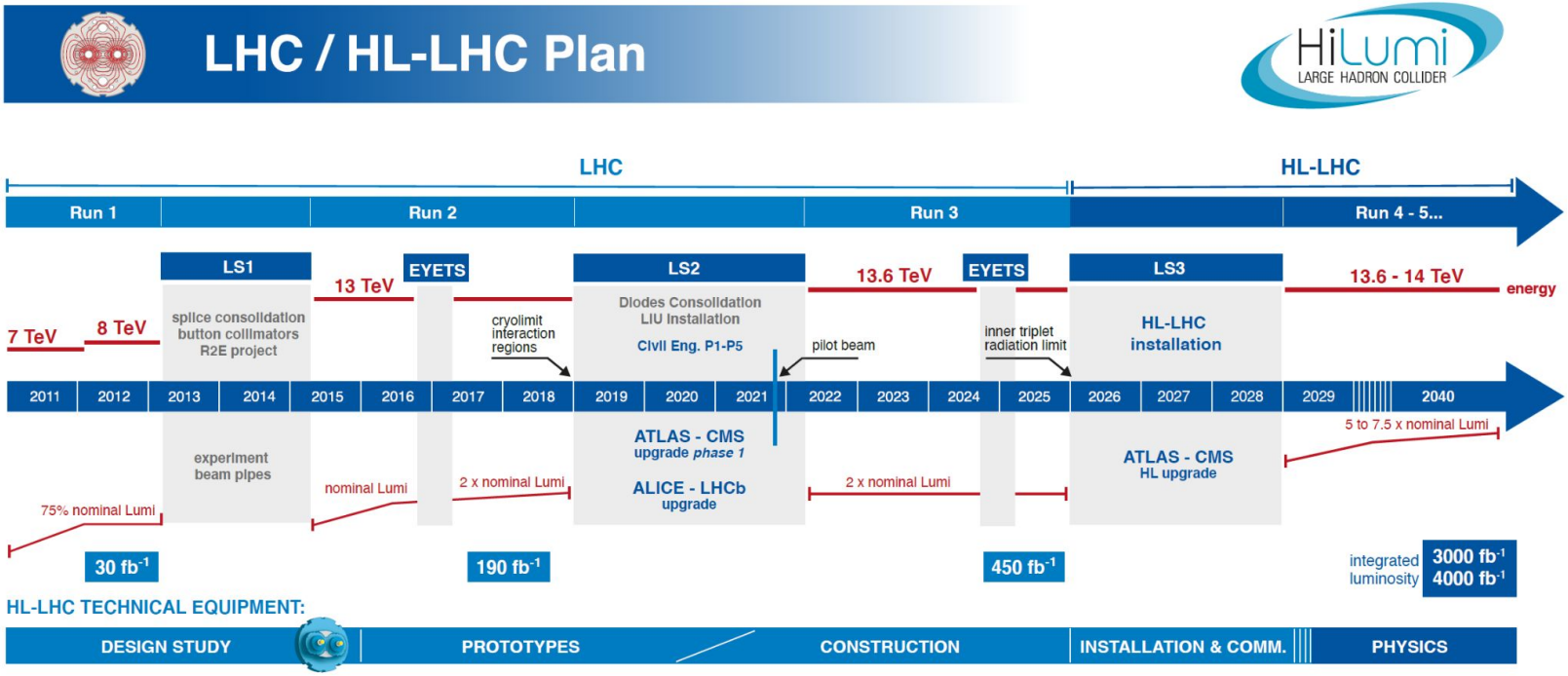
Shaochun Tang

Early Career Scientist Retreat 09/09/2022 @BrookhavenLab

Outline

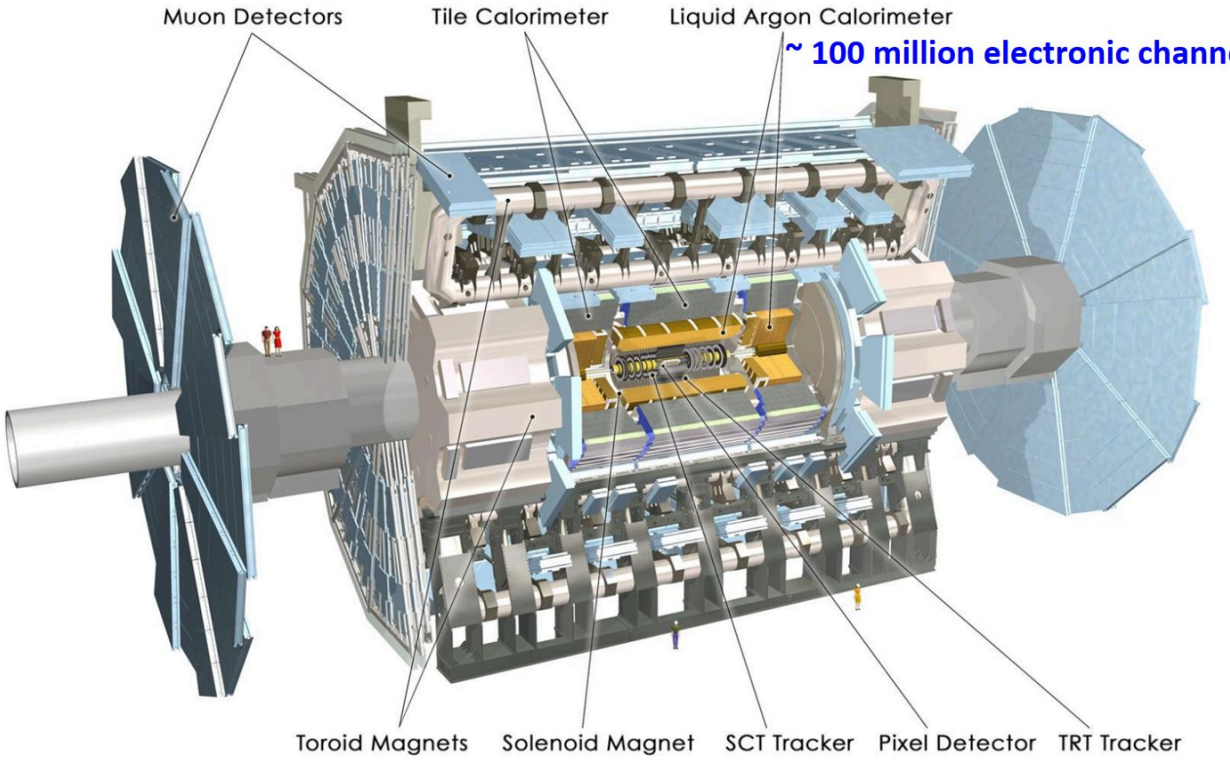
- LHC/HL-LHC Introduction
  - ATLAS Experiment
- ATLAS Phase-I Upgrade Researches
  - FELIX Phase-I Hardware Design
  - ATLAS L1Calo Trigger - gFEX Hardware Design
  - NSW ADDC Production Design and Testing
- ATLAS Phase-II Upgrade Researches
  - Global Common Module (GCM) Hardware Design
  - FELIX Phase-II Demonstrator Design
  - FETBv2 Hardware Design

The Large Hadron Collider: LHC/HL-LHC



- The world's largest and most powerful particle accelerator
- Physics motivation: Higgs particles (2013 Nobel Prize in Physics)/Dark matter and dark energy/Supersymmetric particles
- The Phase I upgrade has been installed, and now in the Run 3 stage.
- The Phase II upgrade will be installed in the Long Shutdown 3 (2026-2028).

The ATLAS Experiment

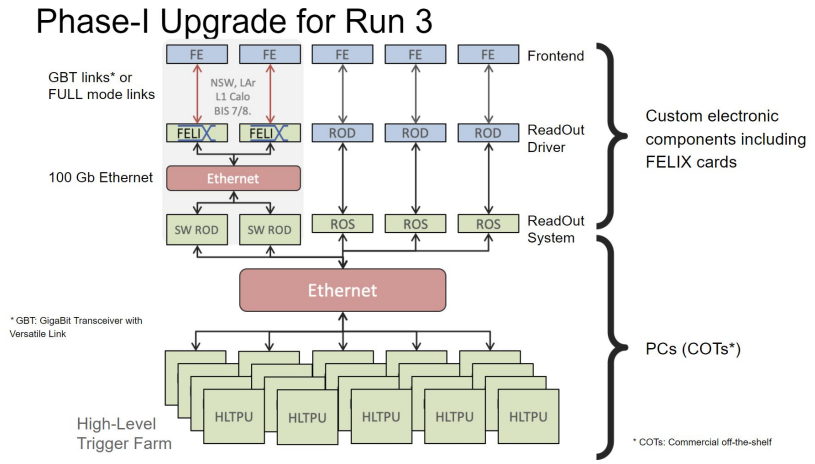


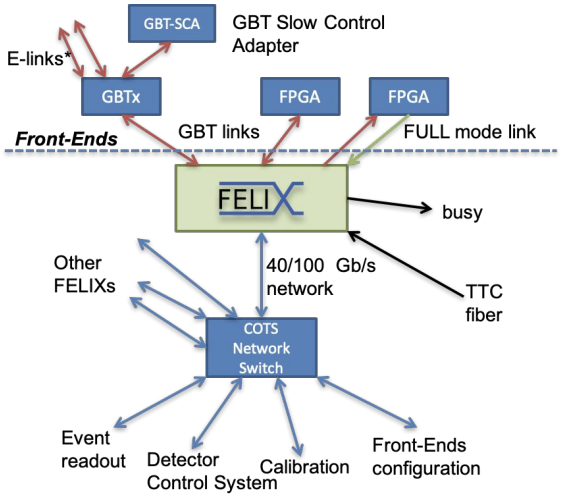
ATLAS is one of the four experiments on the LHC/HL-LHC. It follows the same upgrade steps as LHC/HL-LHC. It consists of several sub-detectors.

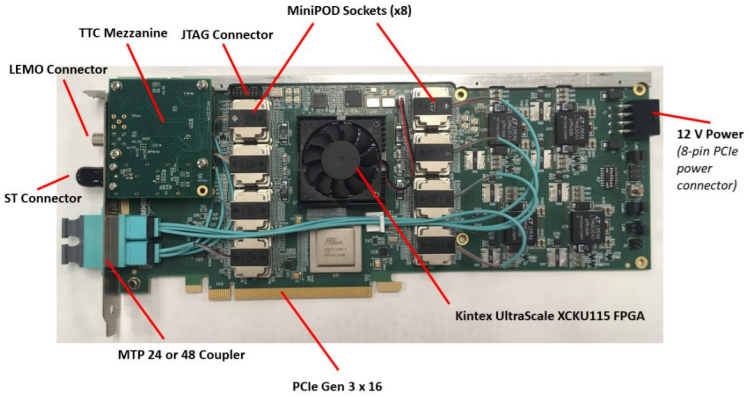
- Inner Tracker
- Tile Calorimeter
- **LAr Calorimeter**
- **Muon**

ATLAS Phase-I Researches

The Front End Link eXchange (FELIX) Phase-I Hardware Design

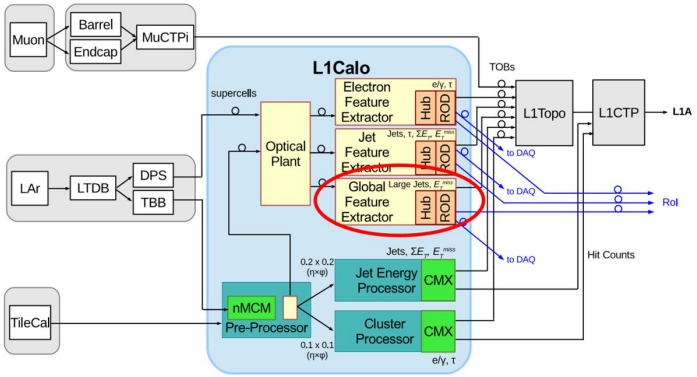


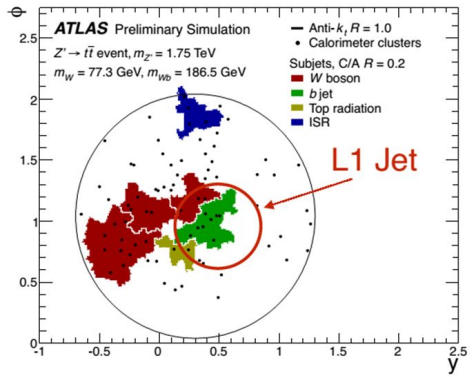


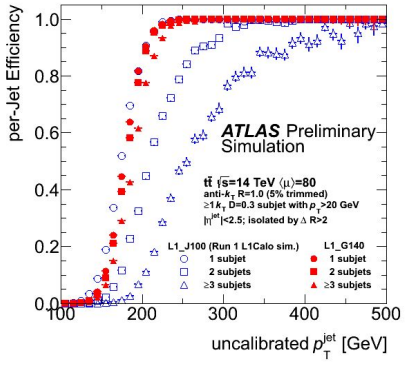


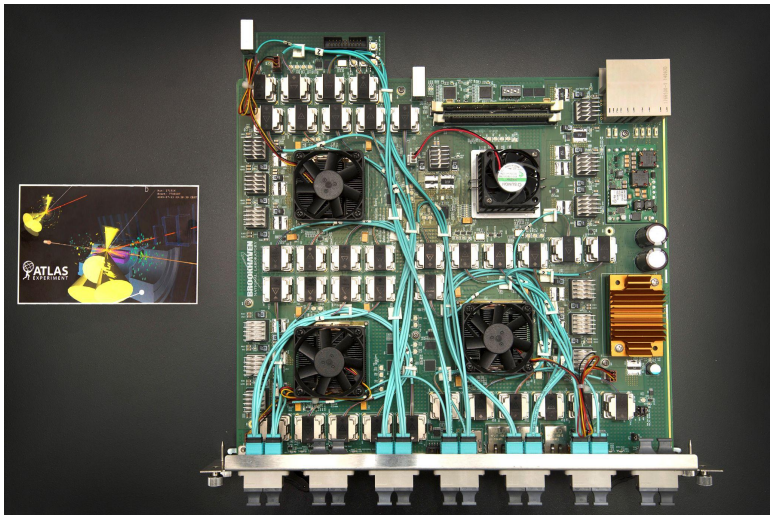
- FELIX is a router between front-end serial links and a commodity network, which separates data transport from data processing.
- Routing of detector control, configuration, calibration, monitoring and detector event data
- TTC (Timing, Trigger and Control) distribution integrated
- Configurable E-links in GBT Mode
- Detector independent
- 225 pcs have been produced at CERN.

Global Feature Extractor (gFEX) Hardware Design





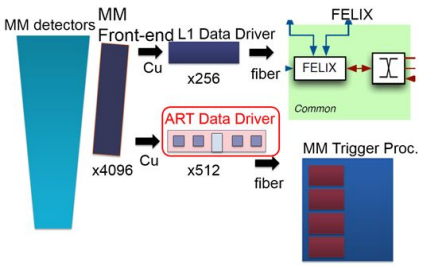


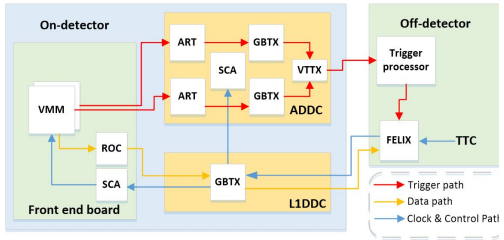


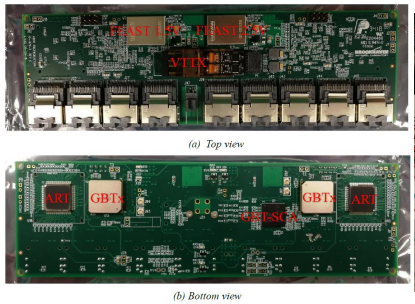
gFEX is part of the Level-1 LAr Calorimeter Trigger system of ATLAS Phase-I upgrade.

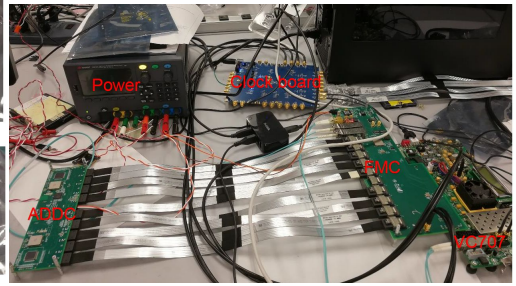
- It will improve the acceptance for large radius (large-R) jets
- Left picture is the production board of gFEX which has been installed at CERN since 2018.
- It has four large Xilinx FPGA and about 300 optical links at 11.2 Gb/s data rate.

ADDC Production and Testing for Muon Detector









ADDC Functionalities:

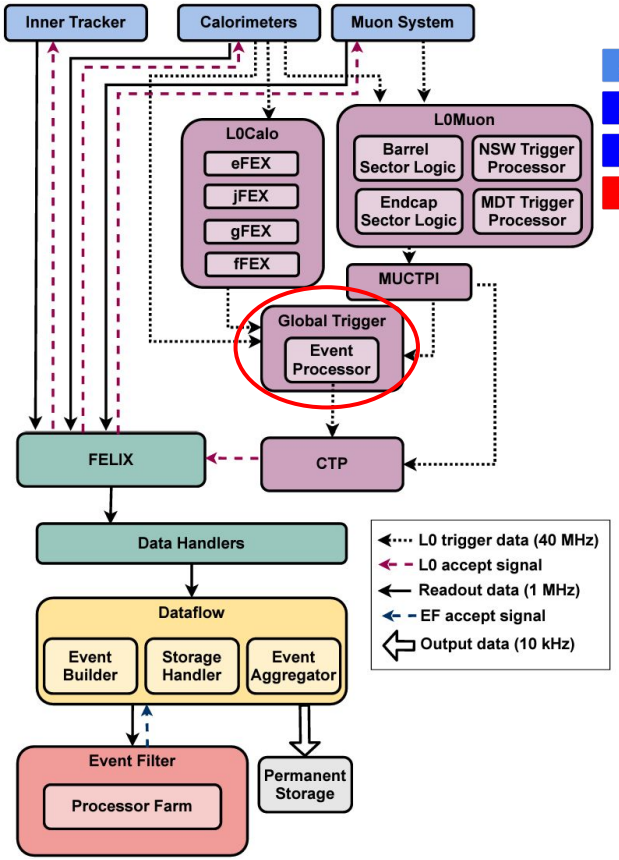
- process and transmit the trigger data from the front-end ASICs
- transfer the ART signals to the trigger processor for the trigger decision.
- Installed on the detector, several custom ASICs are adopted to meet the radiation and magnetic field environment requirement.

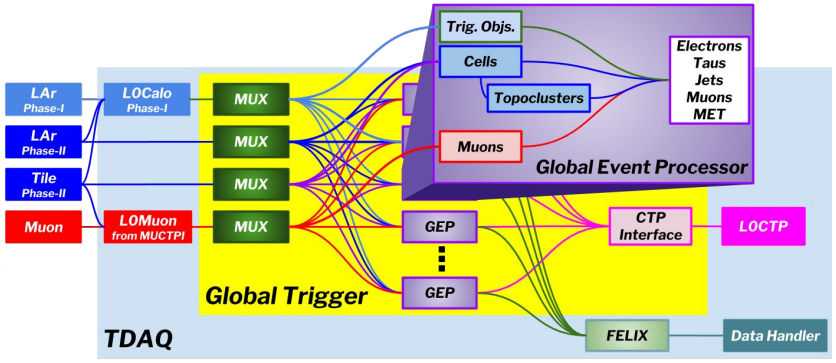
ADDC Production and Test:

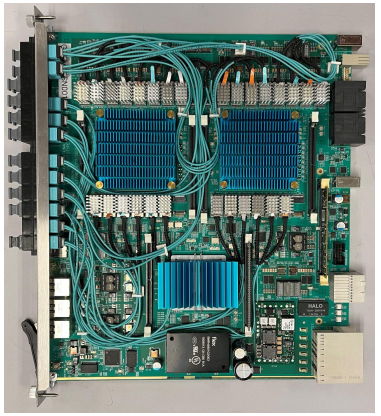
- ART chip partial Q/A were test at BNL (100 pcs).
- 600 pcs ADDC cards were fully tested at BNL before delivering to CERN.
- An automatic test setup with the hardware and software were developed.
- 512 pcs ADDC have been installed into NSW for the Phase-I upgrade.

ATLAS Phase-II Researches

Global Common Module (GCM) Prototype Design



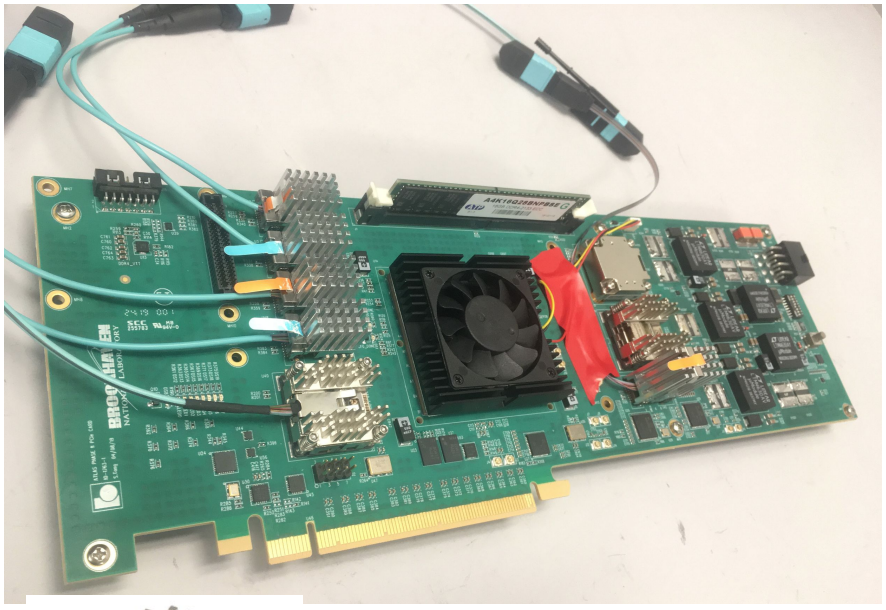


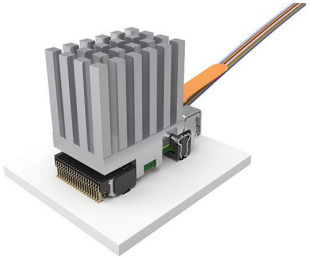


ATLAS has multiple layer trigger architecture. The Level-0 Trigger utilizes custom hardware featuring large Field-Programmable Gate Array (FPGA) for the calorimeter, muon, and central systems. The **Global Trigger** is a new subsystem

- perform offline-like algorithms on full-granularity calorimeter data
- identify topological signatures, replace and extend the functionality of the Topological (Topo) system
- receive all trigger information from legacy systems
- send processed trigger information to Central Trigger Processor (CTP) for final decision
- GCM hardware will be used for as MUX, GEP and CTPi with different firmware in the FPGA.

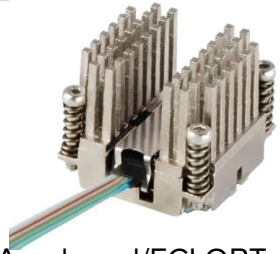
FELIX Phase-II Demonstrator



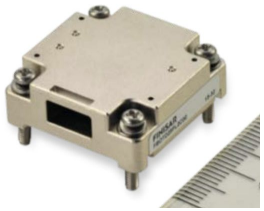


Samtec Firefly
12-ch TX or RX
16G ECUO

Samtec Firefly
4-ch duplex: can be configured as 25/28G



Amphenol/FCI OBT
12 channel duplex:
CDR 25 - 25.8G

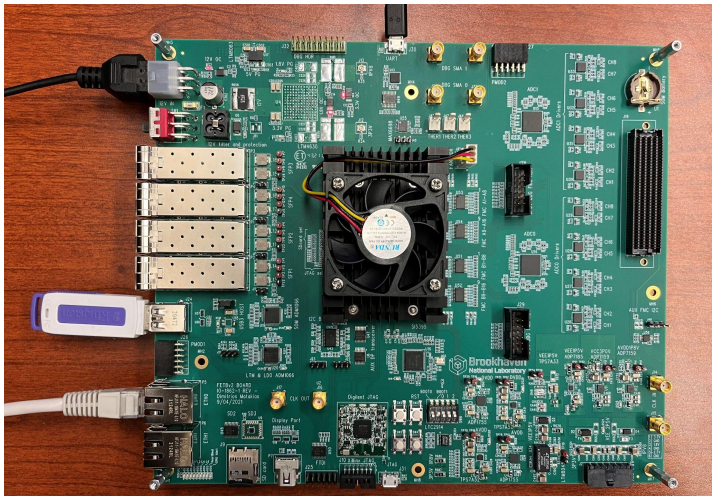


Finisar BOA
OE25-LPFN
12 channel duplex:
CDR 25 - 28.1G

FELIX Phase-II Demonstrator was designed in 2019, and served as:

- PCIe Gen 4 demonstrator and firmware design platform
- 25 Gb/s optical module evaluation

FETBv2 Hardware Design



FETBv2 was designed for ALFE2 ASIC performance and Q/A, Q/C test.

- It includes the data taking and processing part and analog Analog-to-Digital Converter (ADC) part.
  - The data taking and processing part is based on Enclustra XU1 SOM.
  - The ADC part has two TI 8-Channel 16-Bit 125-MSPS (ADS52J65).
- The FETBv2 can be used as a template for the **CaRIBOu**, or other projects.

Thanks