EICROC status and plans

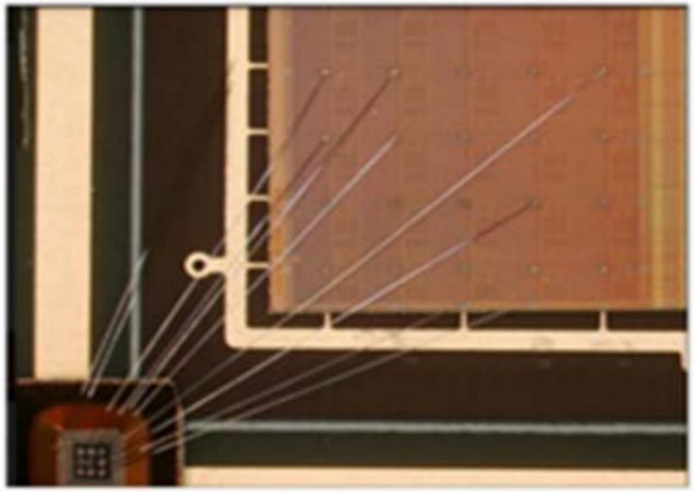
F. Bouyjou, E. Delagnes, JJ Dormard, F. Dulucq, M. Firlej, T. Fiutowski, J. Gonzalez, F. Guilloux, M. Idzik, C. de La Taille, J. Moron, D. Marchand, C. Munoz, M. Morenas, N. Seguin-Moreau, L. Serin, K. Swientek, D. Thienpont

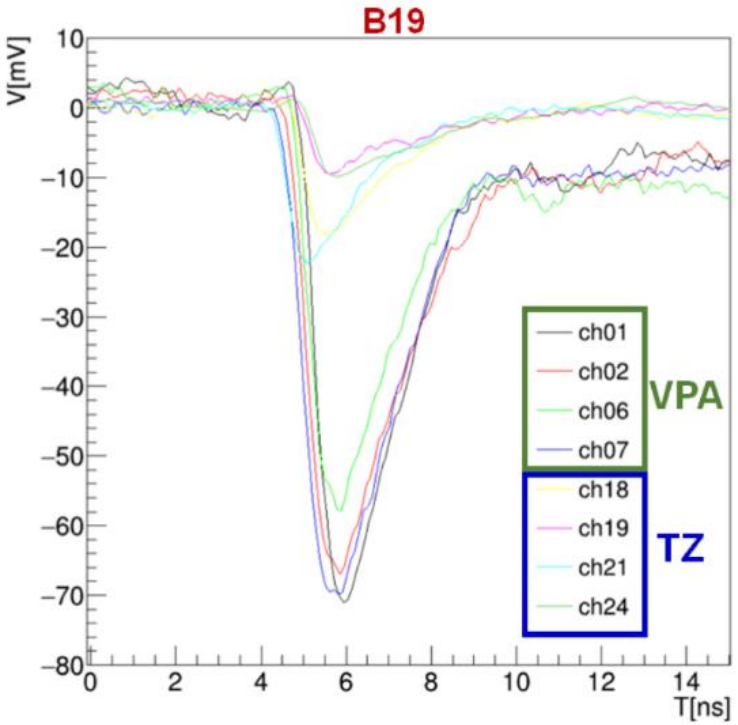
7 sep 2022

Organization for Micro-Electronics desiGn and Applications

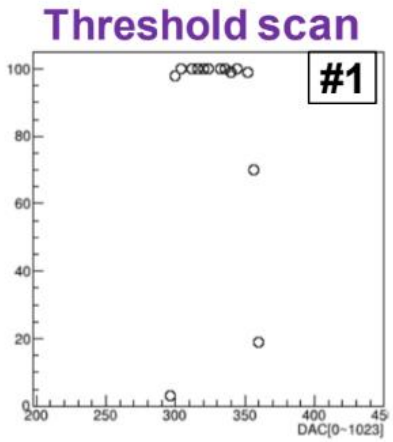
FY2022 report : AC-LGAD sensors with ALTIROC1

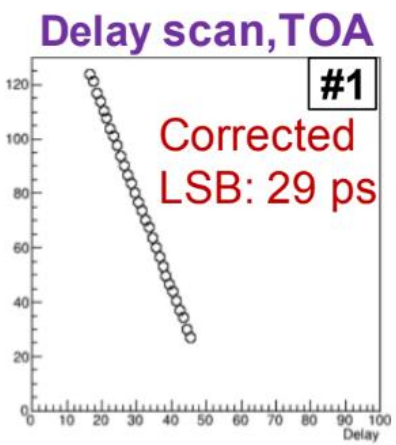
- Characterization of an AC-LGAD sensor wired-bonded to an ALTIROC1 chip

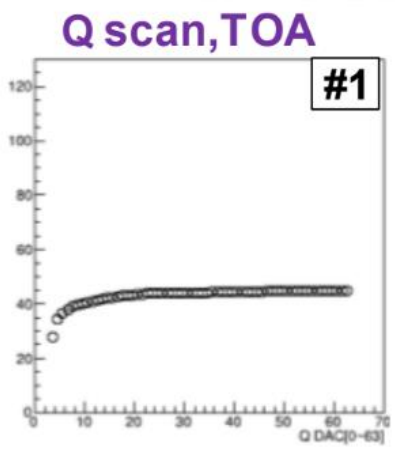


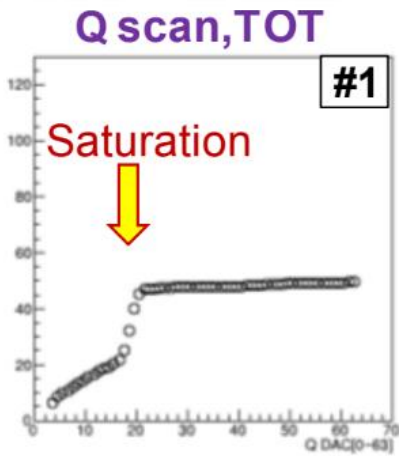


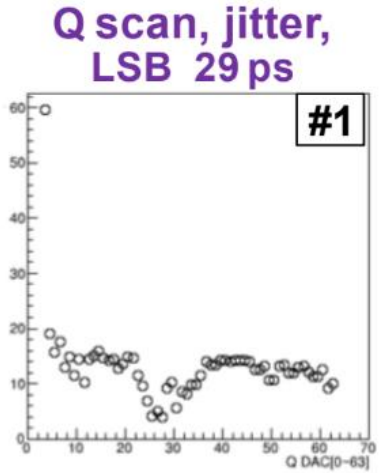
HV: -160V (I ~68nA)
DAC pulser: 10 (~8fC)





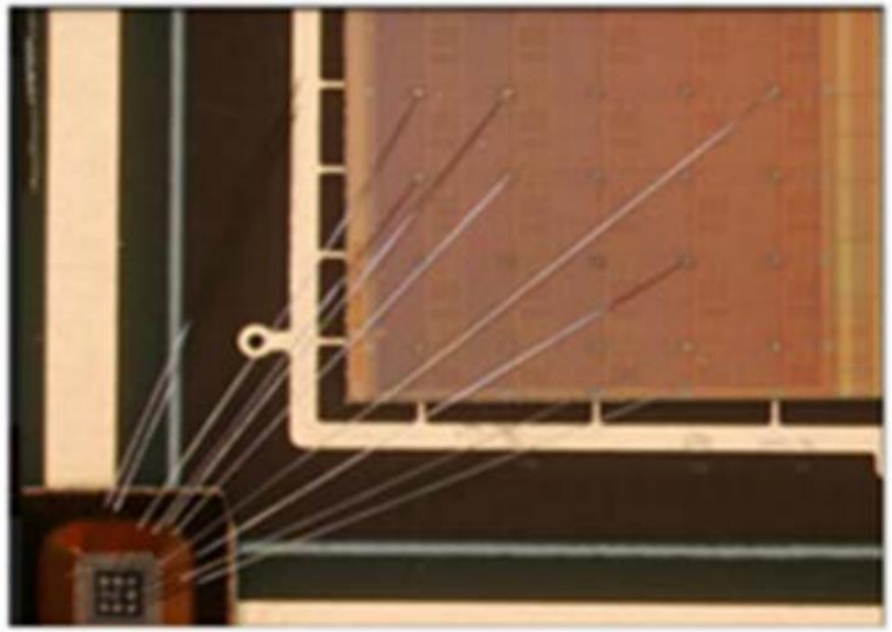


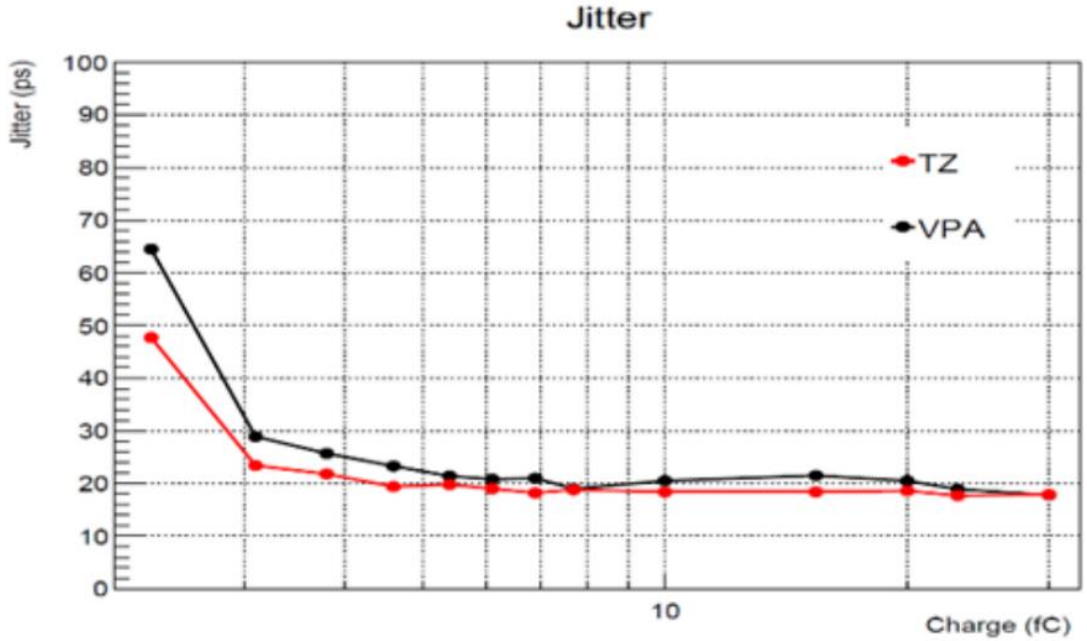




- Corrected LSB (Least Significant Bit) for each TDC channel is ~30ps
- Most channels show a saturation for Q > ~ 21 fC
- The average jitter for each channel is ~15-20ps
- Connected TDC channel performances uniform
- Study of PA amplitudes versus injected charge and charge sharing between pads on-going

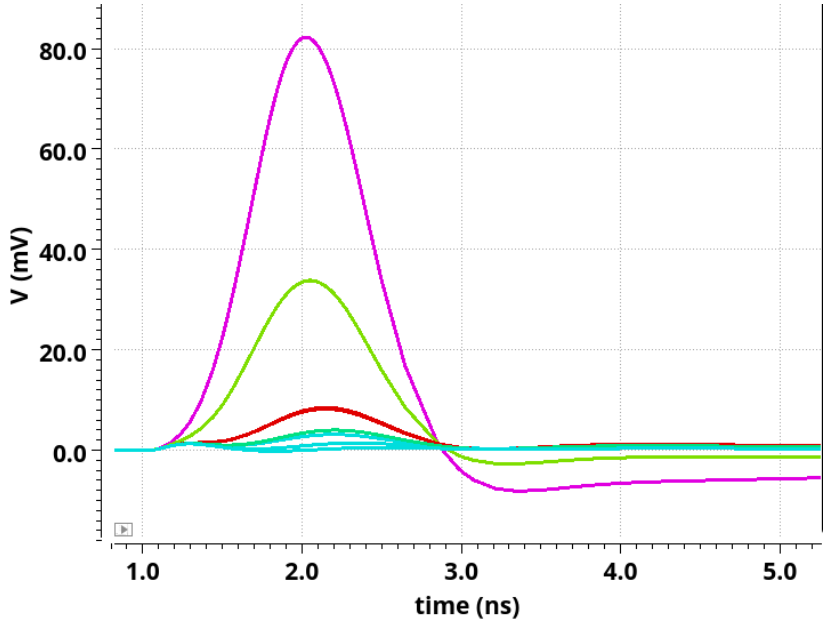
FY2022 report : AC-LGAD + ALTIROC1 time resolution



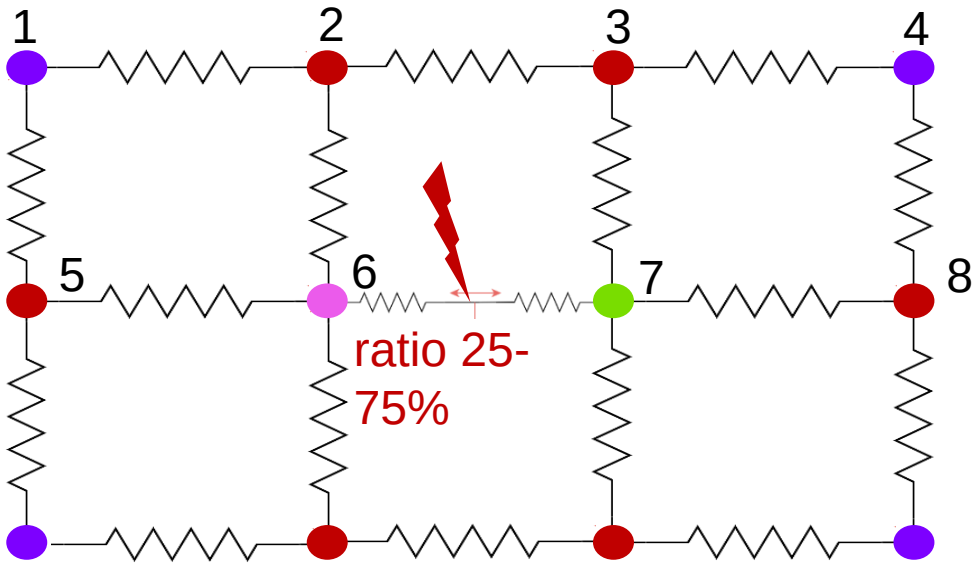


Time resolution ~20 ps for MIP (19 fC), equivalent to what was measured with DC-LGADs for HGTD

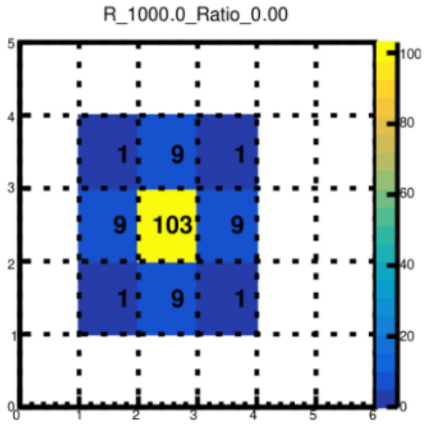
FY222 report: simulations

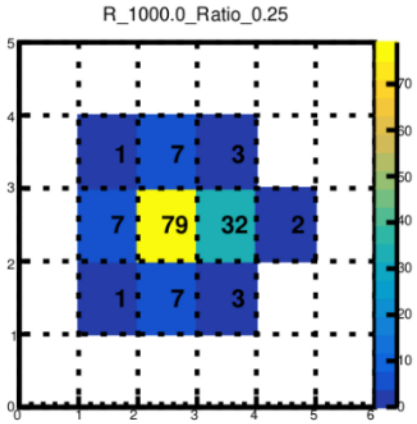


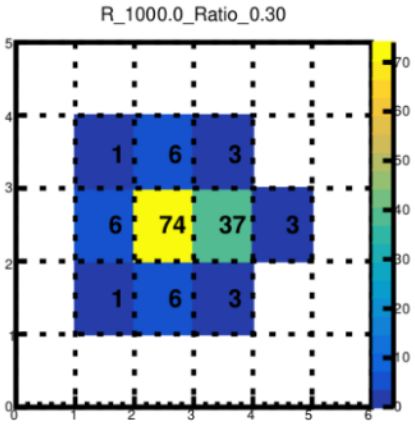
When charge deposition (19 fC) at distance ratio 25-75%

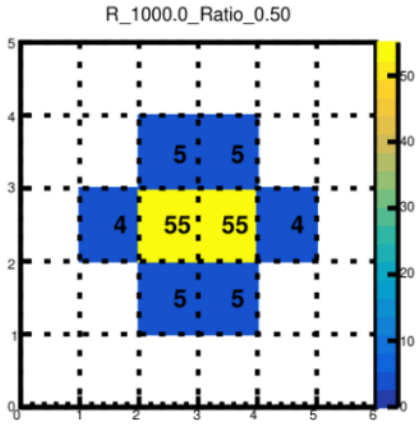


$R_{sheet} = 1\ kOhm$



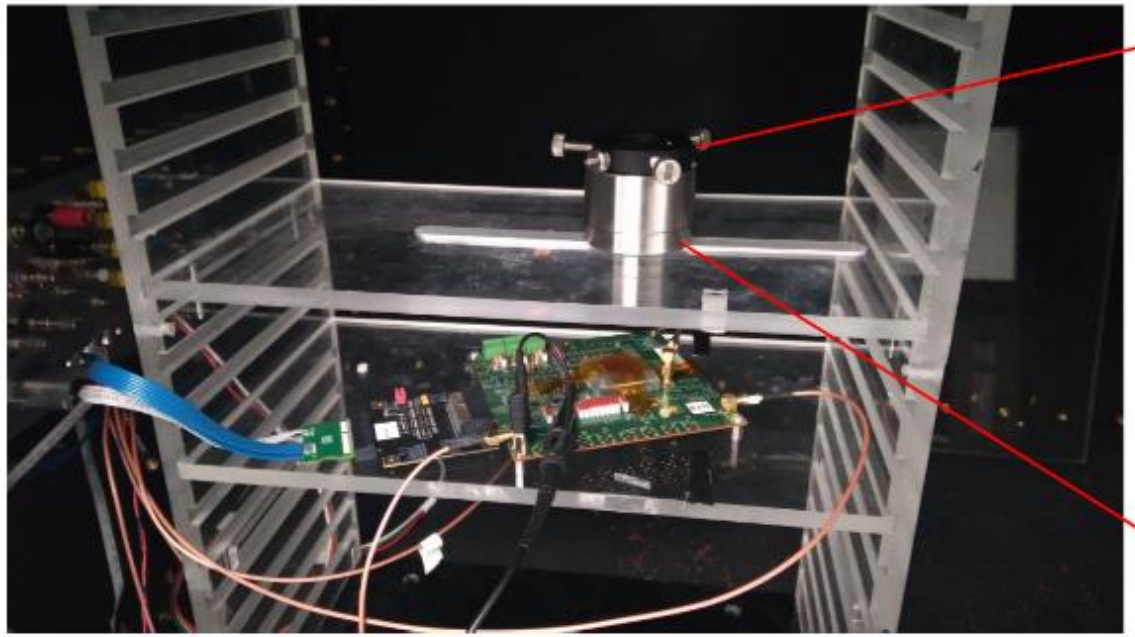


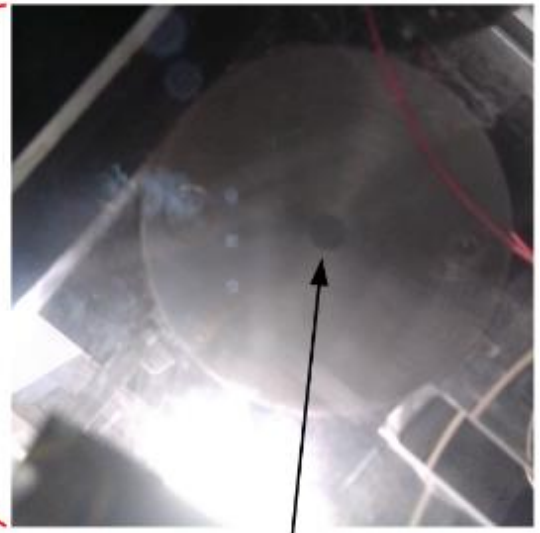




Simulation TZ, inject charge: 19pF

FY22 report: characterization with beta source



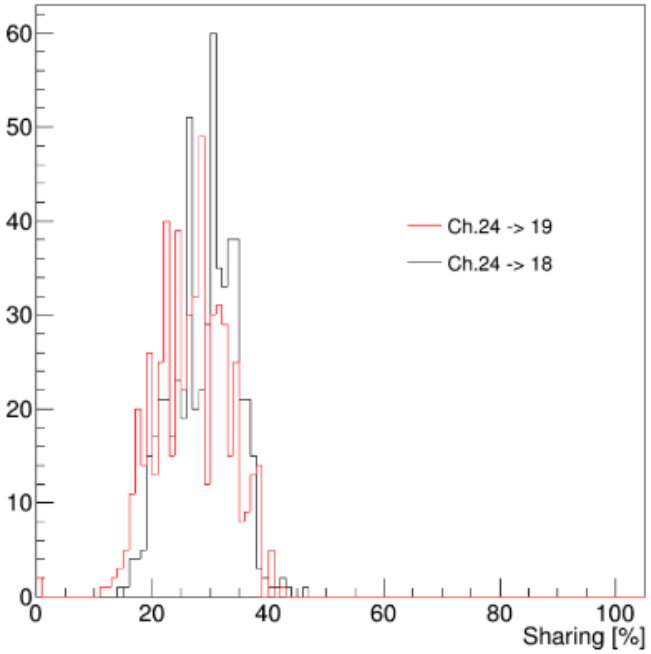


Beam hole for Sr-90 [37MBq]

1	2	7
NC	6	18
21	19	24

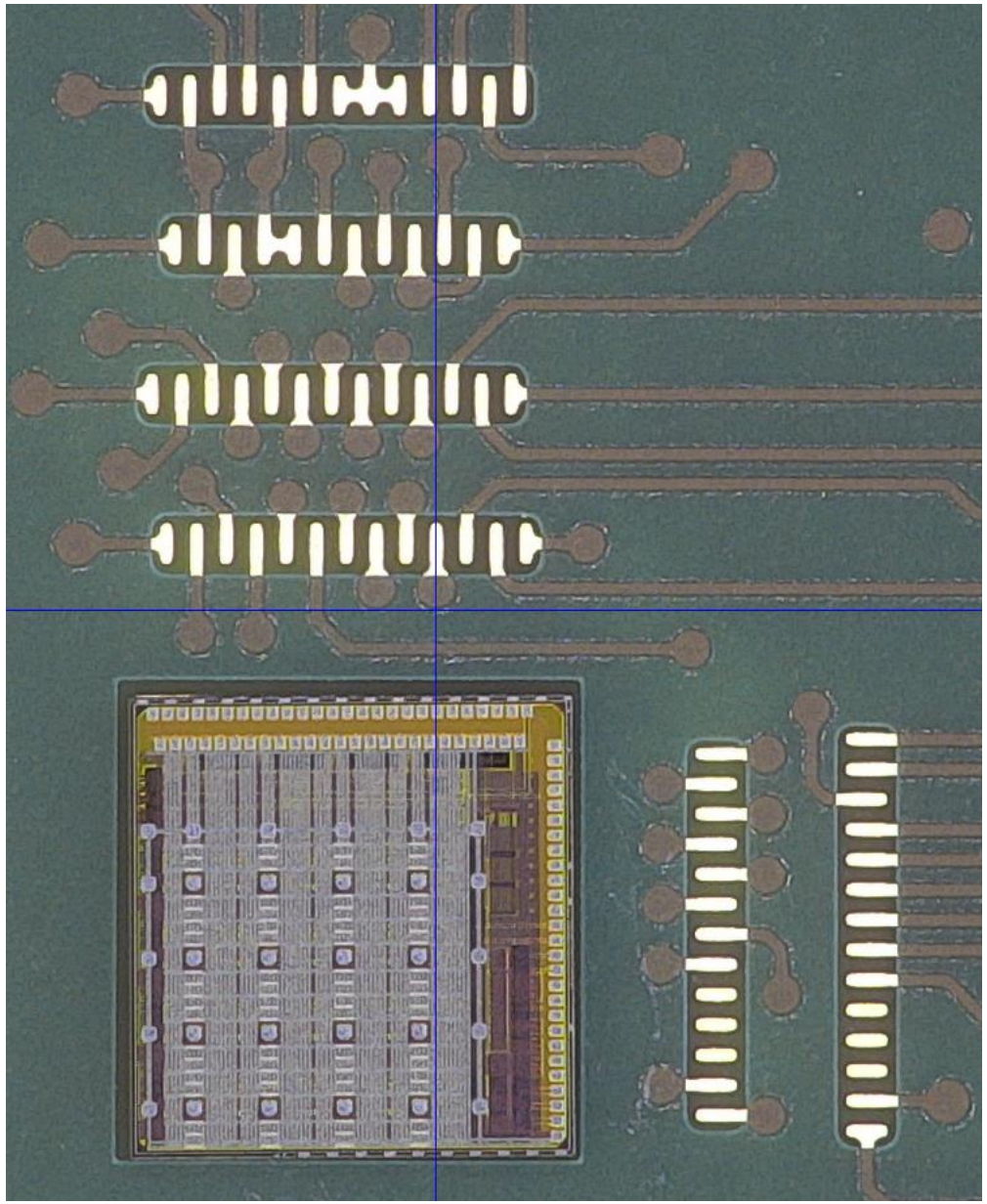
24 share to 18 and 19
$TOT_{24} > TOT_{18}$ and $TOT_{24} > TOT_{19}$

Sharing from Ch.24 to 18, 19



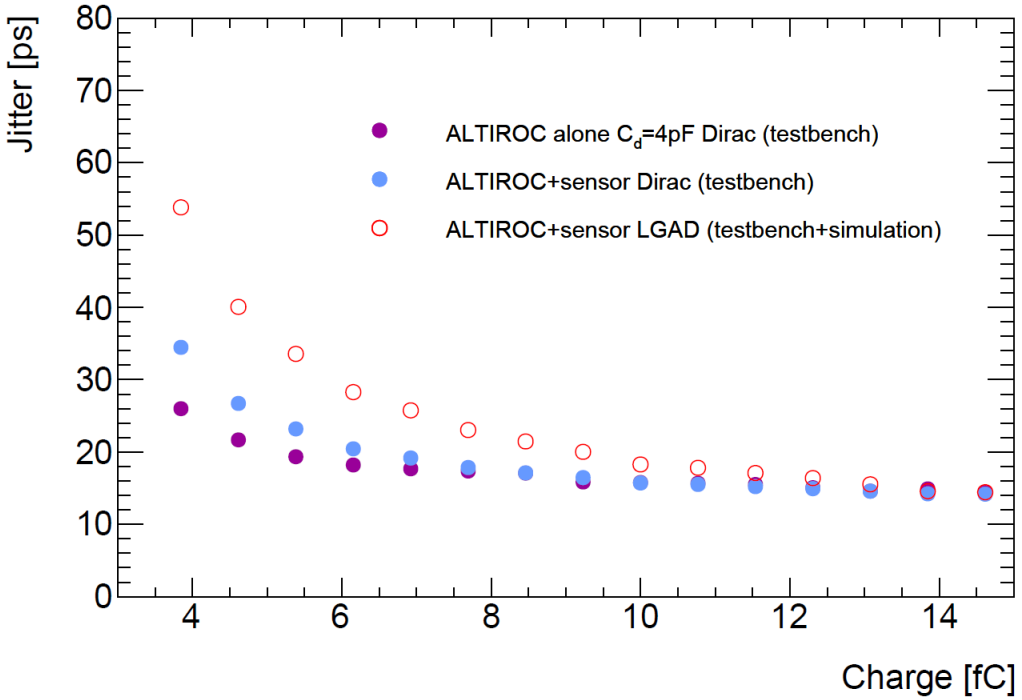
FY22 report: EICROC0 design and fabrication

- EICROC0 is a 16-channel testchip for AC-LGADs at EIC
  - Based on ALTIROC (ATLAS HGTD) front-end and HGCROC (CMS HGCAL) ADC/TDC
  - Reads 500x500 um pixels for sensor evaluation
  - Readout designed for testbeam (not EIC)
  - Fabricated in march 2022, received beg july 2022
  - now at bonding at BNL



FY22 report : EICROC design based on HGTD ASIC (ALTIROC)

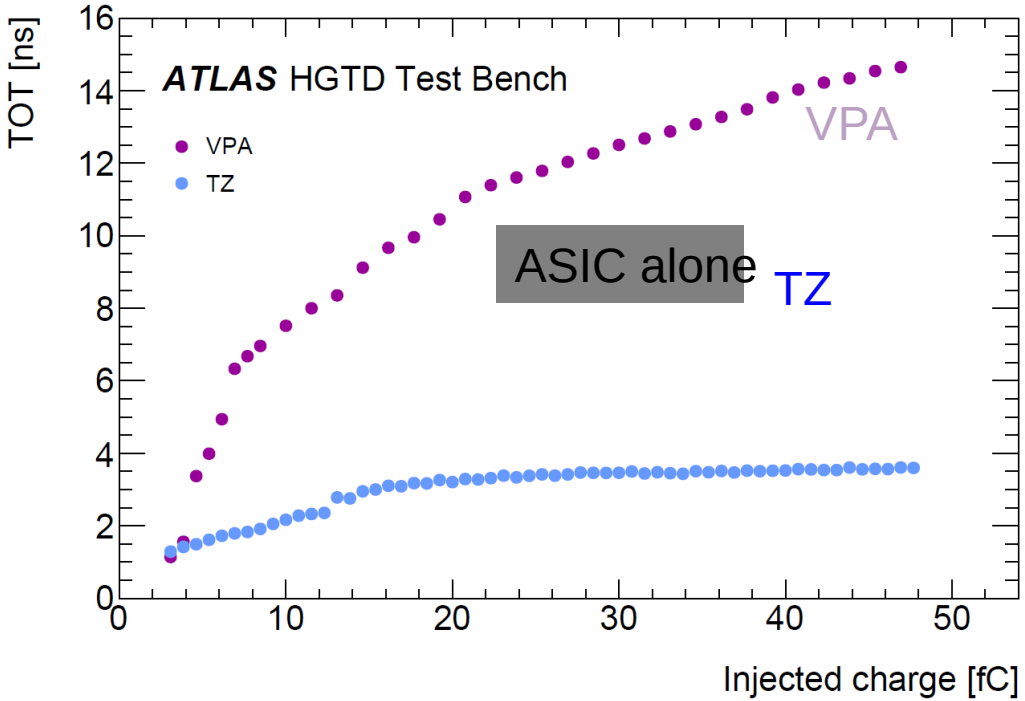
- Altiroc1 prototypes since 2018 , 25 channels (Preamp + discri + TOA and TDC TDS + SRAM) to validate front-end since 2017
  - TDC performance validated
  - TOA jitter performance validated
  - TOT performance : validated with ASIC alone, but still some concern when connected to sensor + HV connection
  - Phase shifter & PLL performance validated
- Altiroc1 bump bonded onto sensors: Very useful to understand system an integration issues

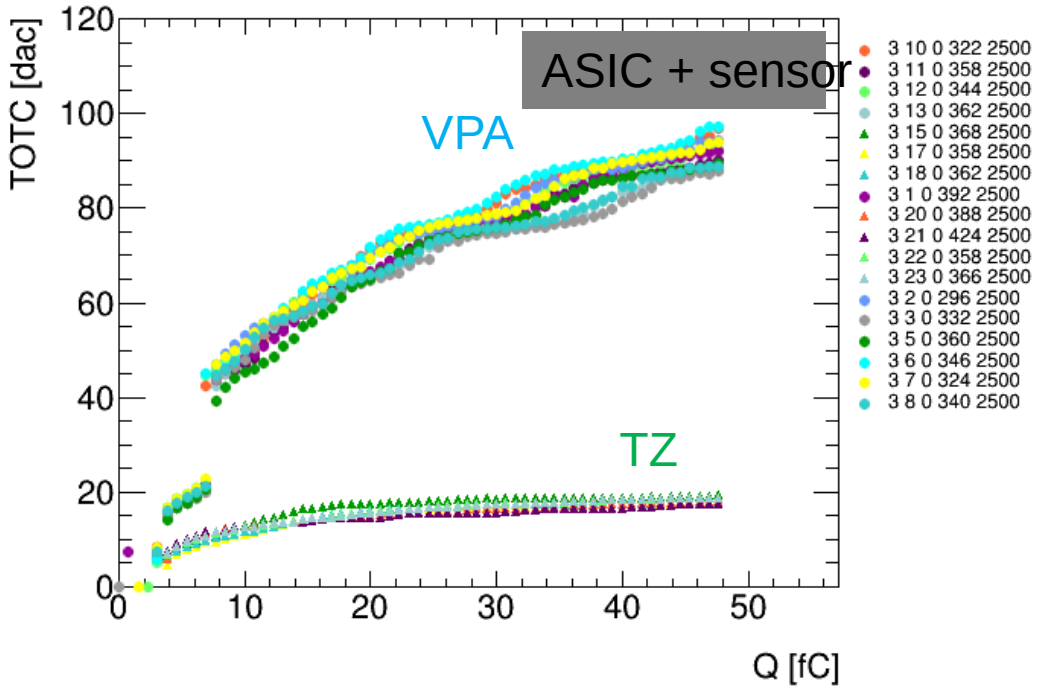


< 20 ps for Q > 6 fC dominated by clock/TDC/calib command
< 40 ps at Q=4 fC start to be dominated by noise

FY22 report: time walk correction

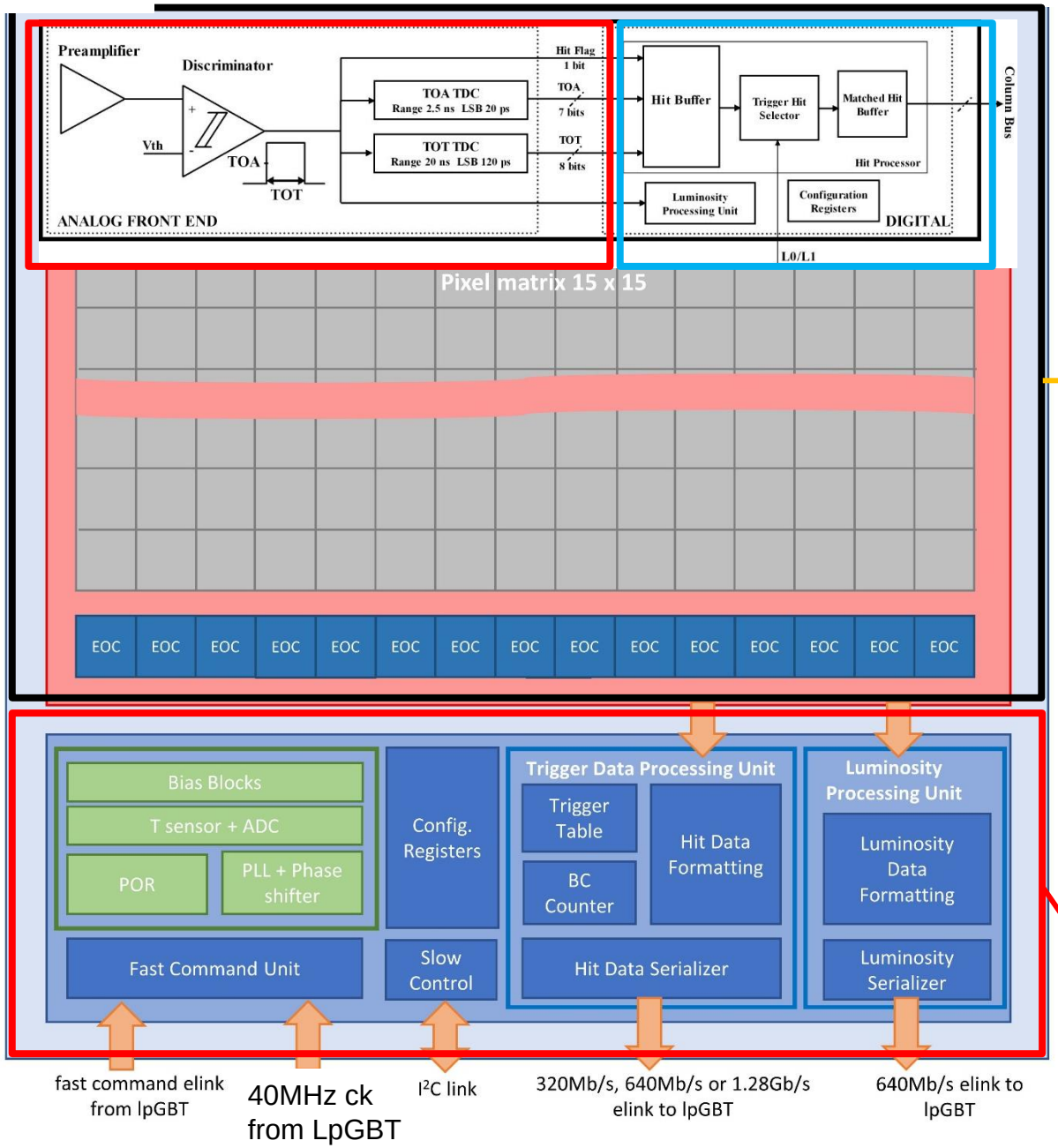
Jitter performance was ok on test bench (see TDR) but no testbeam in 2020 for validation with particles
TOT issue has been further investigated on test bench :

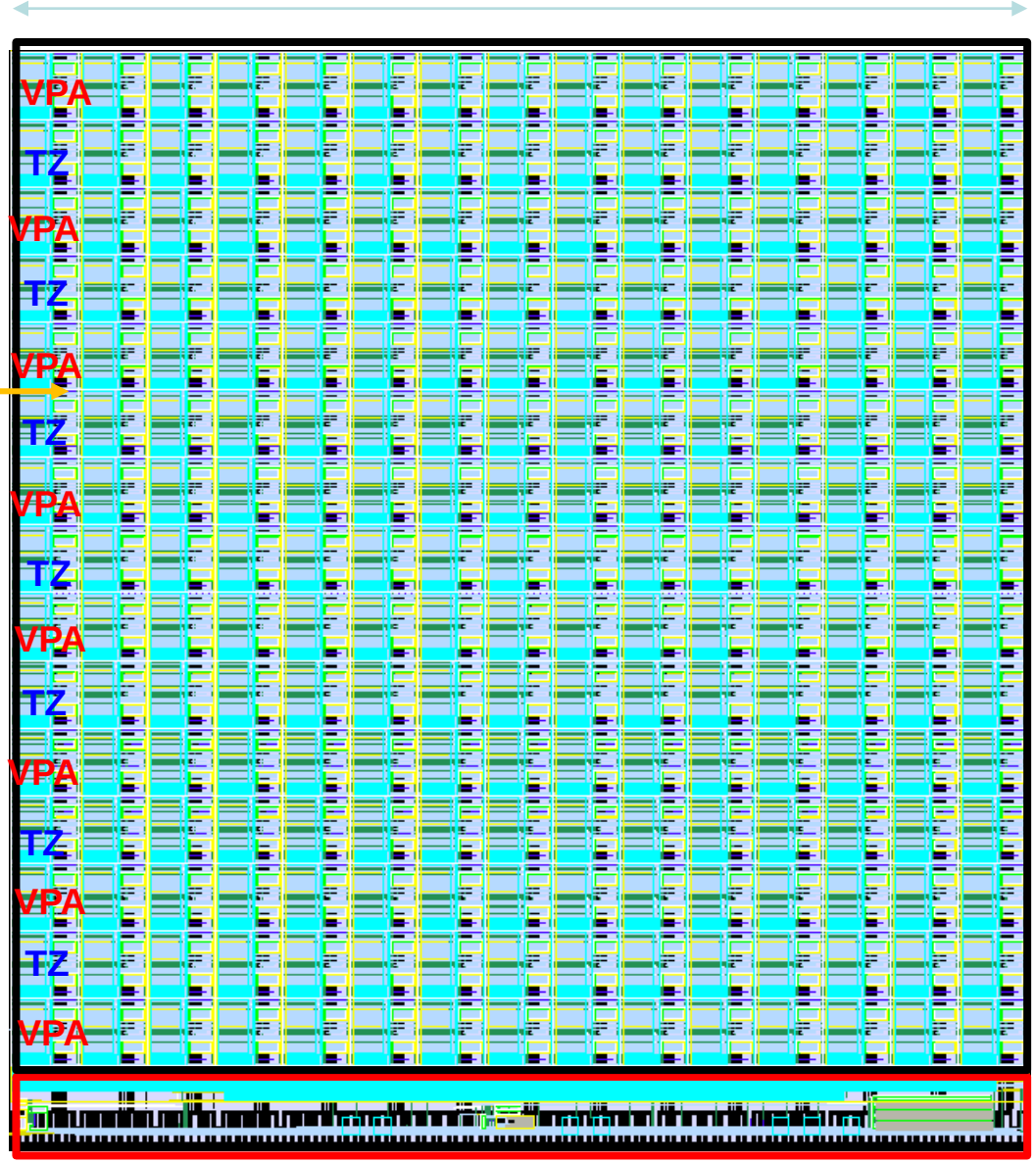




TOT behaviour fine when ASIC alone. It shows small kinks but can be used for time-walk correction
Discontinuities appear when ASIC bump bonded to sensor **AND** Bias Voltage wire-bonded….
Better behavior using Transimpedance preamp (TZ) instead of Voltage preamps (VPA)
=> integration of both preamps types in Altiroc2

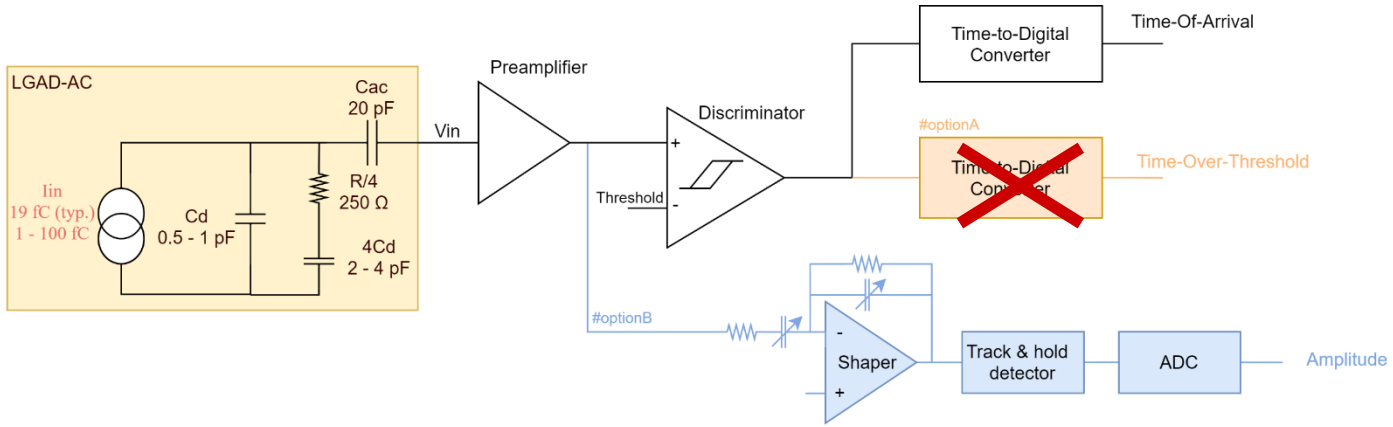
Altiroc2 full size ASIC

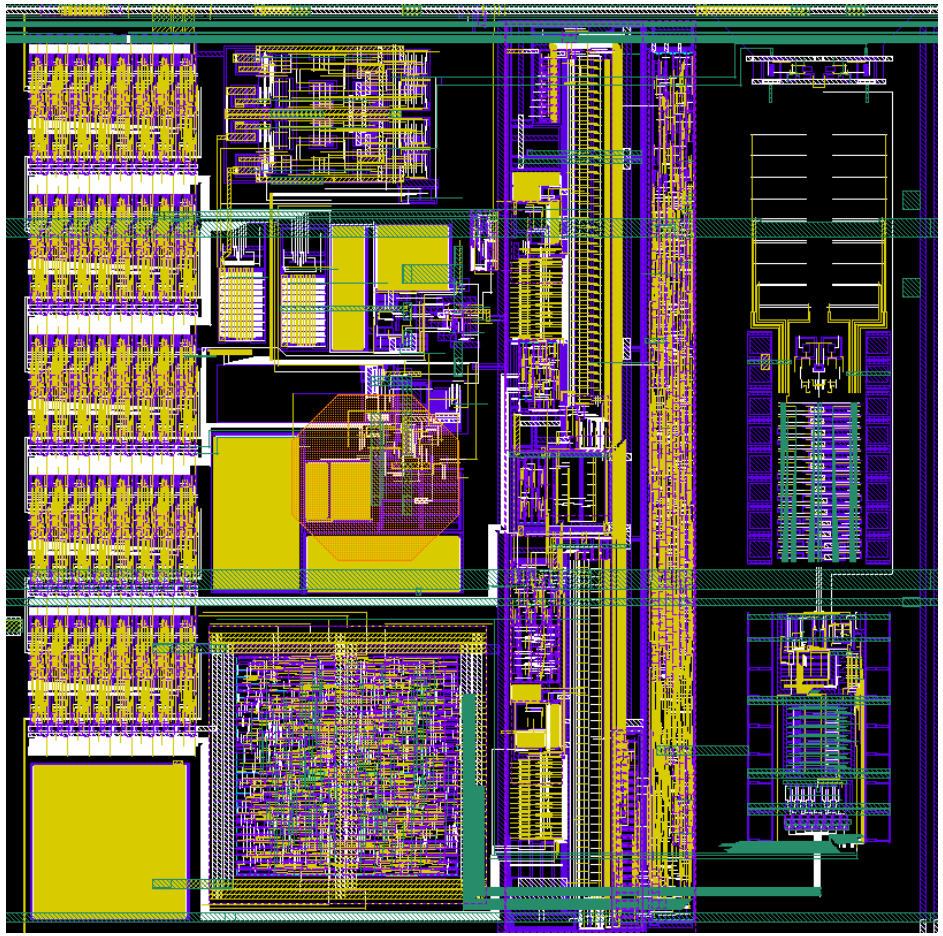




FY22: EICROC0 - one pixel overview

- One pixel design
  - Preamp, discri taken from ATLAS ALTIROC
  - I2C slow control taken from CMS HGCROC
  - TOA TDC adapted by IRFU Saclay
  - ADC adapted to 8bits by AGH Krakow
  - Digital readout : FIFO depth 8 (200 ns)
- 5 slow control bytes/pixel
  - 6 bits local threshold
  - 6 bits ADC pedestal
  - 16 TDC calibration bits
  - Various on/off and probes





Slow control

PA +discri

TOA TDC

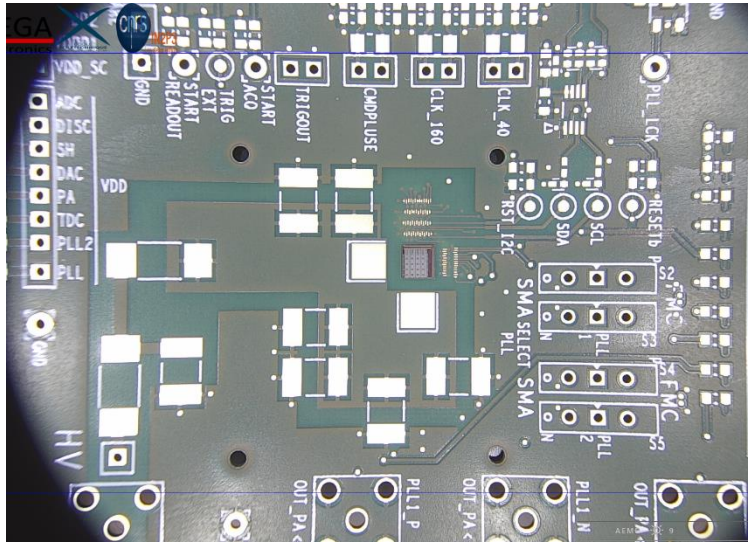
8b 40M ADC

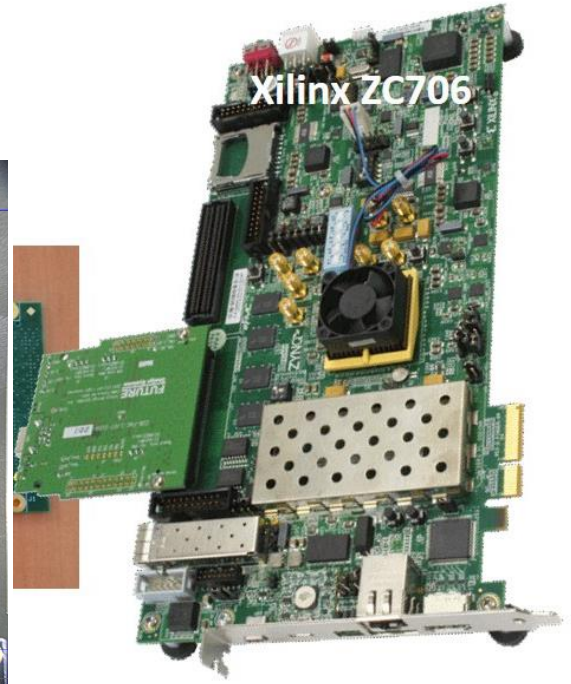
FY22 report: testboard

- Connect to KCU via FMC connector
- Level translators 1.2V – 2.5V
- Space near chip to accomodate sensor
- 4 SMAs for preamps outputs
- On-board regulators for LV

- Wirebonds in 4 rows 200um pitch

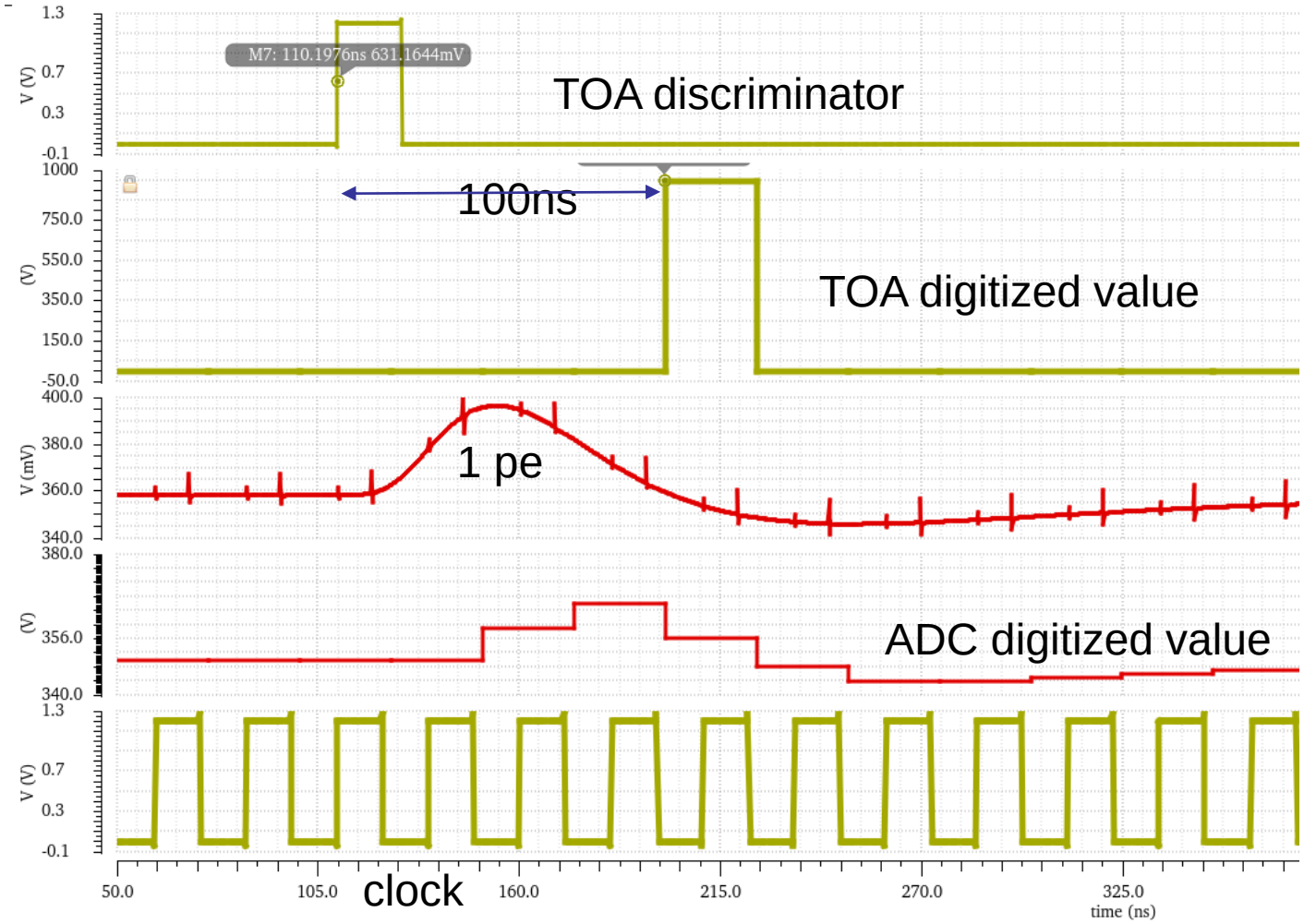
- Fabricated in june 2022
- Now at BNL for ASIC bonding





FY23 plans: EICROC1 - waveforms

- Illustration from another (similar) chip (HKROC)



FY23 plans: next steps

- EICROC1 : larger chip to study floorplanning and EIC DAQ
  - Probably with variants of columns to study different low-power front-end and digitization
  - Target 1 mW/ch (lower power ADC)
  - Study clock adaptation to EIC (100 MHz input)

Budget request for FY23: $75k

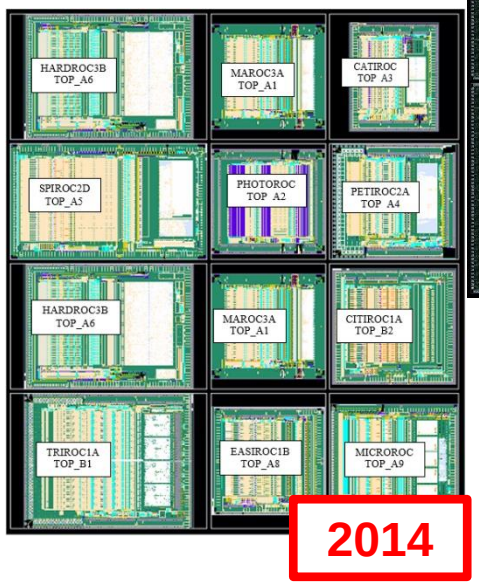
- $65k for a Multi-Project Wafer (MPW): EICROC1
- $10k for testboards and components

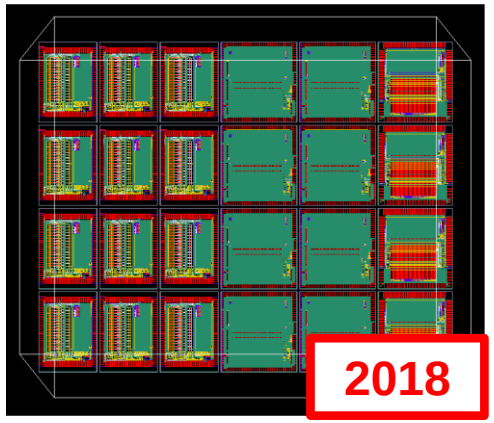
- Full size chip could be expected in FY24-25 depending on prototype results and personpower availability

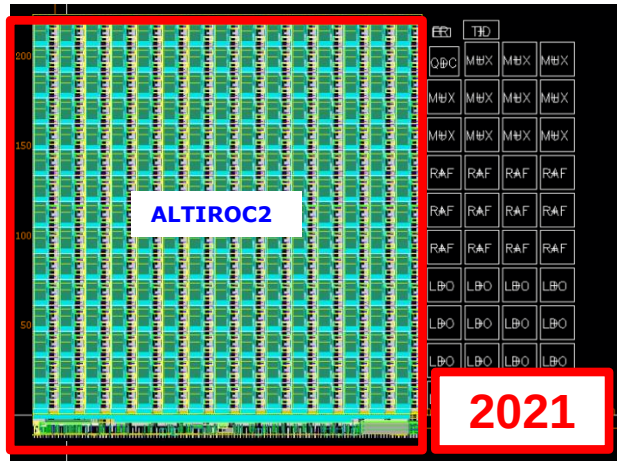
Backup

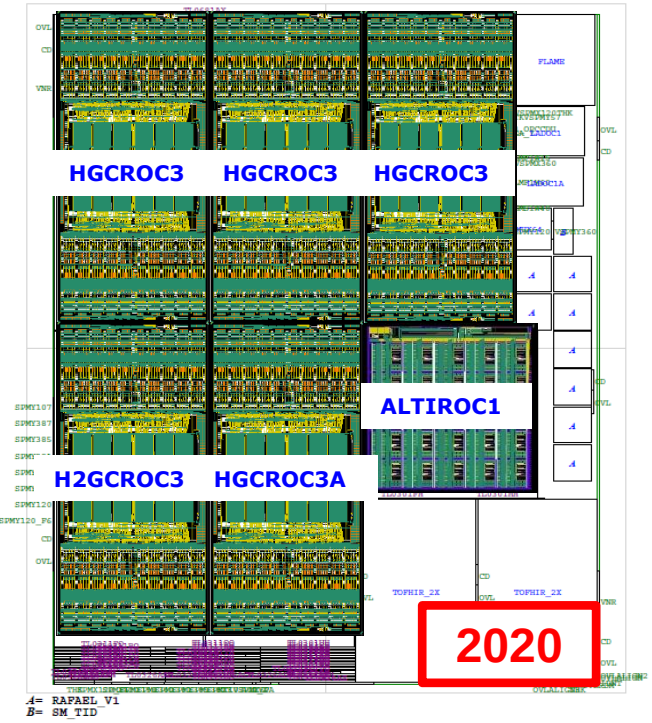
OMEGA Engineering runs

- 6 engineering runs in 8 years !
  - AMS SiGe 0,35um 2014, 2016, 2018
  - TSMc 130nm : 2019, 2020, 2021
  - 6-24 wafers 8'' and 12'' : thousands of ASICs built and used
  - Cost : 200-300 k€, shared between projects : very efficient !

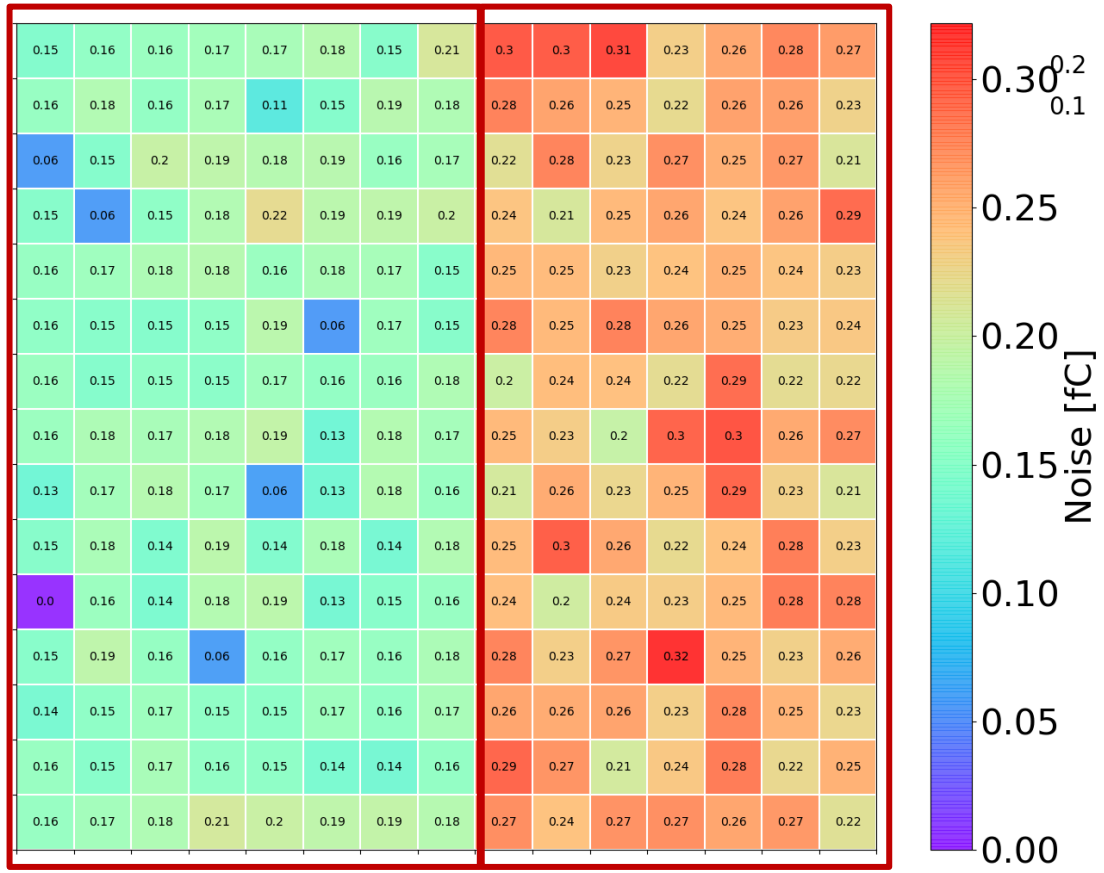








Altiroc2 preliminary measurements: B8 (ASIC alone)



VPA : pixels 0 to 119 TZ : pixels 120 to 224