

SCIPP (UC Santa Cruz) contributions to EPIC

Simone Mazza for the SCIPP group



SCIPP has a long history of involvement with the LGADs in general, and AC LGADs in particular

AC-LGAD invention at SCIPP



US009613993B2

(12) **United States Patent**
Sadrozinski et al.

(10) **Patent No.:** **US 9,613,993 B2**
(45) **Date of Patent:** **Apr. 4, 2017**

- (54) **SEGMENTED AC-COUPLED READOUT FROM CONTINUOUS COLLECTION ELECTRODES IN SEMICONDUCTOR SENSORS**
- (71) Applicants: **The Regents of the University of California**, Oakland, CA (US); **Istituto Nazionale di Fisica Nucleare**, Turin (IT)
- (72) Inventors: **Hartmut F. W. Sadrozinski**, Palo Alto, CA (US); **Abraham Seiden**, San Jose, CA (US); **Nicolo Cartiglia**, Milan (IT)
- (73) Assignee: **The Regents of the University of California**, Oakland, CA (US)

- 31/02005* (2013.01); *H01L 31/022408* (2013.01); *H01L 31/053* (2014.12)
- (58) **Field of Classification Search**
CPC *H01L 27/14603*; *H01L 27/14641*; *H01L 27/14643*; *H01L 31/053*; *H01L 31/02005*; *H01L 31/022408*
USPC 257/443, 448, 459, 461, E27.133, 257/E27.149; 250/389, 370.01
See application file for complete search history.
- (56) **References Cited**
U.S. PATENT DOCUMENTS
5,225,696 A * 7/1993 Bahraman *H01L 27/14887* 250/208.1
5,589,705 A * 12/1996 Saito *H01L 27/14643* 257/443

Areas of Past/Current Work Relevant to the EIC

- What is needed for an AC-LGAD for EIC?
 - Time resolution 25 ps per hit (sensor+chip) → almost there
 - Position resolution < 30 μm per hit (one or two directions) → achieved
 - Acceptable power consumption (electronics, 1-2 mW per channel depending on density) → ok, but can do better
- Current tentative design: 500 μm x 1 cm strips for barrel, 500 x 500 μm pixels for end cap
- Over the past couple years, **SCIPP** has directed some of its LGAD effort in directions designed to **generally or directly support EIC detector development**
 - Sensor testing/simulation and ASIC production/testing
- **Goals of SCIPP's contribution**
 - **Improve timing resolution**: exploration of thinner sensors (20 μm) and ASIC development
 - **Optimization of spatial resolution**, allowing the pixel count to be as small as possible for a given resolution target (**reduction of power consumption**): testing of sensor prototype with different geometries, TCAD simulation

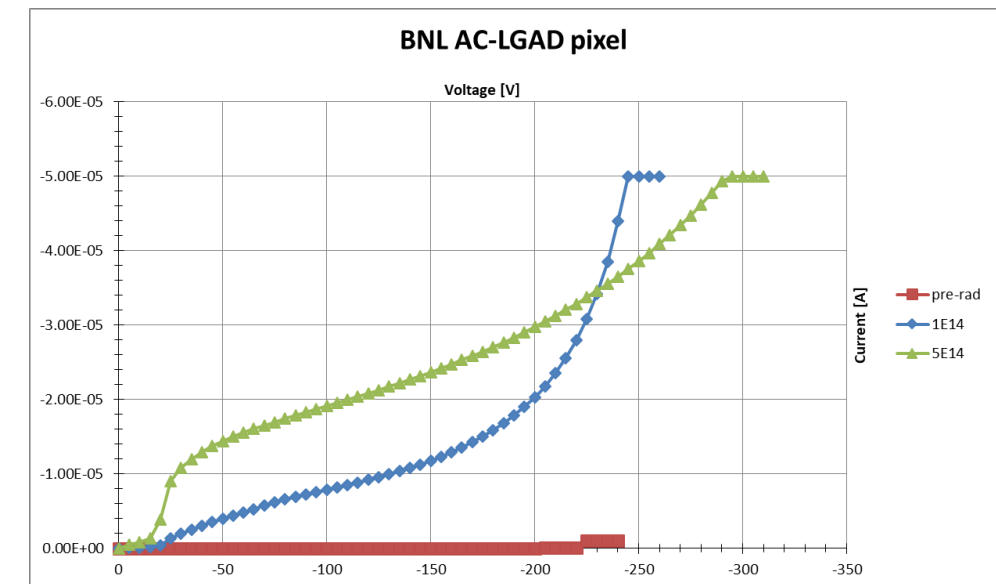
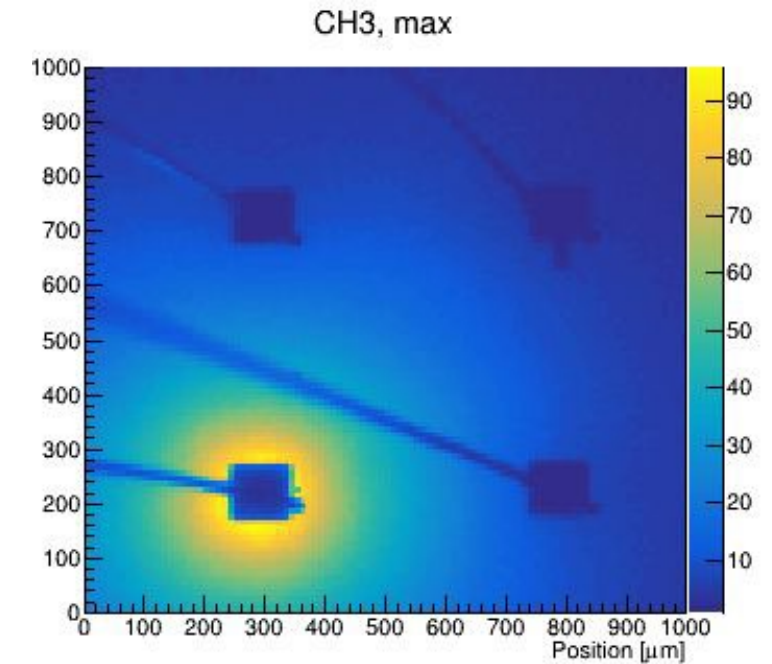
SCIPP present R&D work for EIC

- Prototype AC-LGAD sensors (from BNL, HPK and FBK) laboratory characterization and simulation
 - **IV/CV and laser characterization:** tested several devices and identified good and bad properties in AC-LGADs
 - **FNAL test-beam analysis:** study of long range sharing and sensor response homogeneity
 - **TCAD-based sensor design:** successfully reproduced AC-LGAD behavior with TCAD, followed by parameters optimization
- Electronics development
 - **ASIC design** together with external companies via SBIR funding: HP-SoC1 prototype tested, ASROC chip coming soon
 - Design of several readout boards for ASIC testing
 - **ASIC testing:** first results from HP-SoC1 are encouraging
- Prototype system assembly (LANL system)
- Some actual results shown in the next slides, **lessons learned at the end!**

AC-LGAD prototype testing

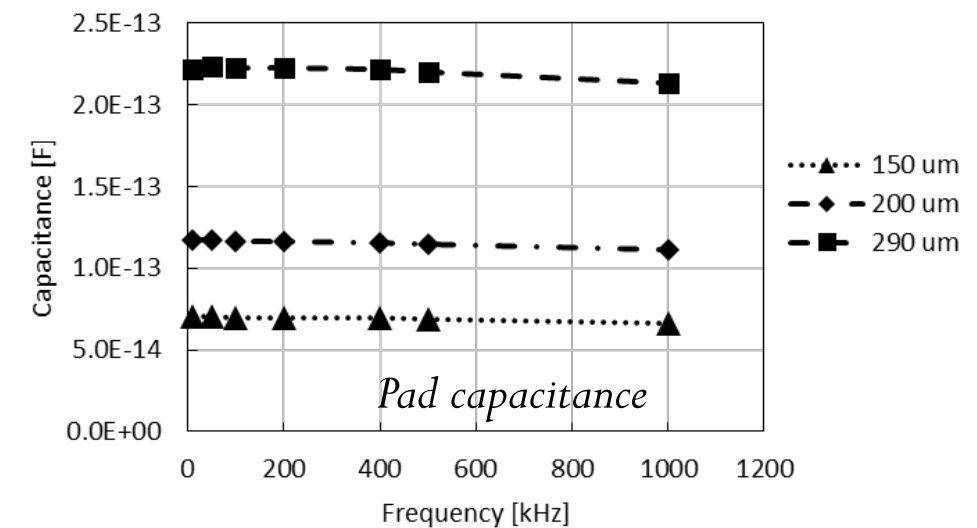
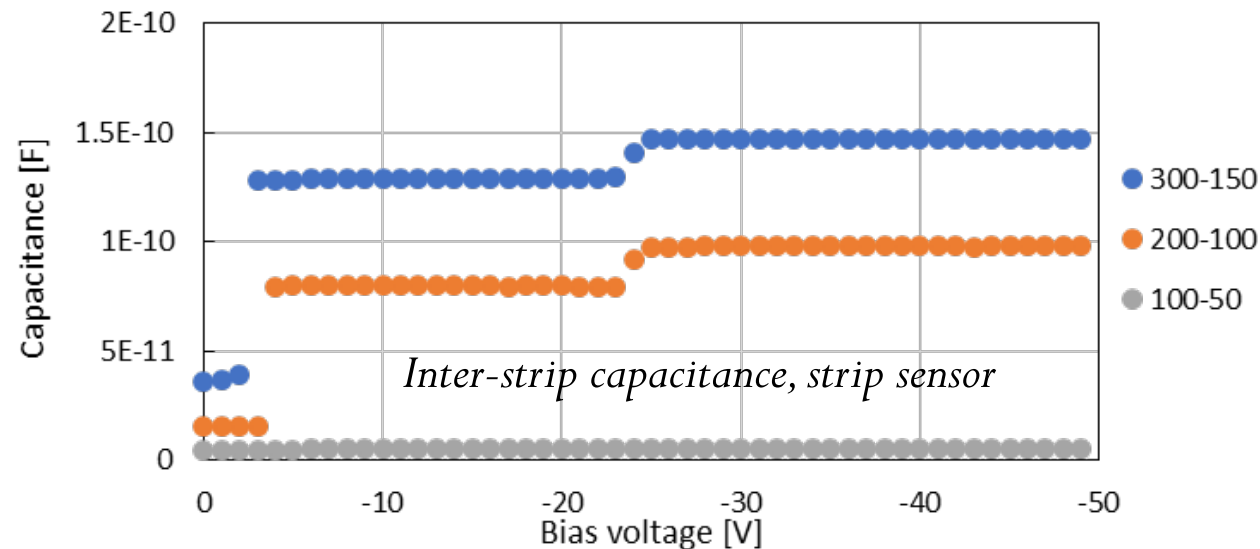
Laboratory sensor testing

- Testing of AC-LGAD prototypes produced at BNL, FBK and HPK
- **Electrical characterization** of devices (IV / CV) (J. Ott + students)
 - Check capacitance of full device, AC-pads and coupling capacitance
- Characterization of AC-LGAD with **TCT laser system** (S. Mazza + students)
 - **Test of charge sharing** for different metal geometries (strips length, pitch, width)
 - Study of gain layer homogeneity in large devices
- **Neutron irradiation campaign** of AC-LGADs in the TRIGA reactor in Ljubljana and testing afterwards
 - Irradiation at $1\text{E}14$ Neq and $5\text{e}14$ Neq of FBK, HPK and BNL devices
 - Study the effect of irradiation on gain layer and N^+ resistivity

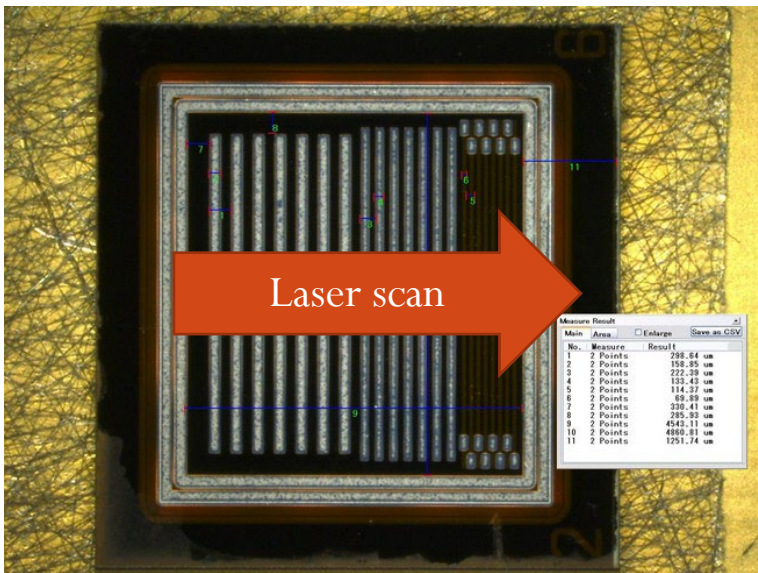
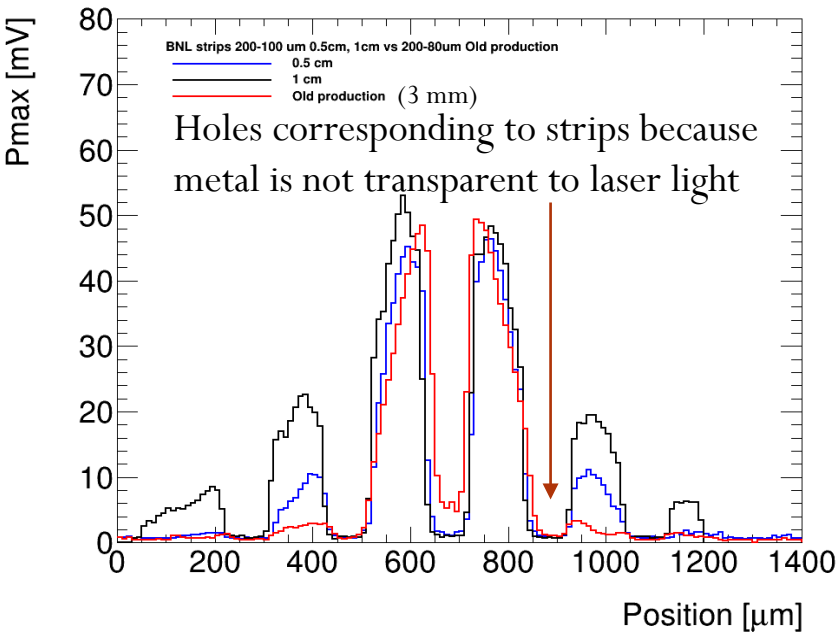
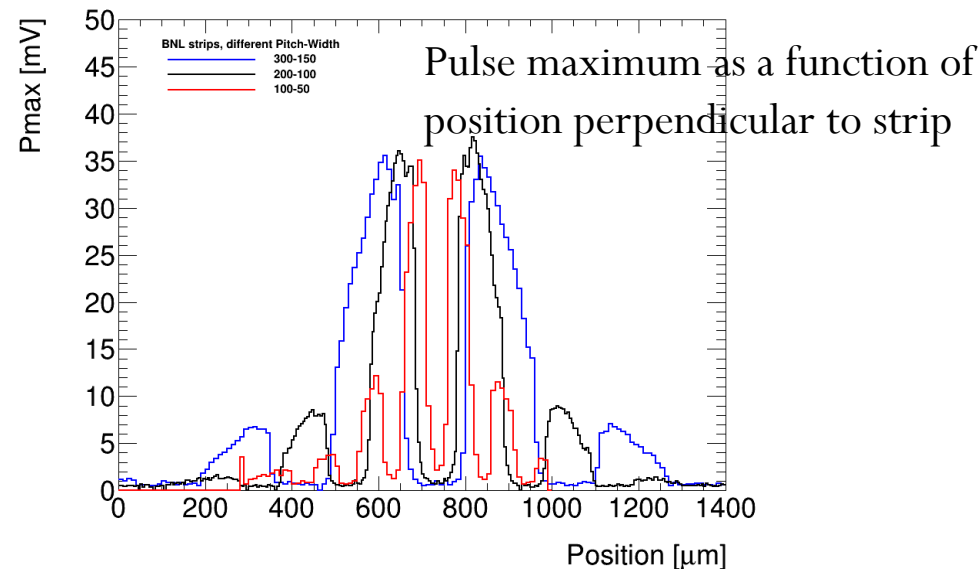


C-V and I-V measurements

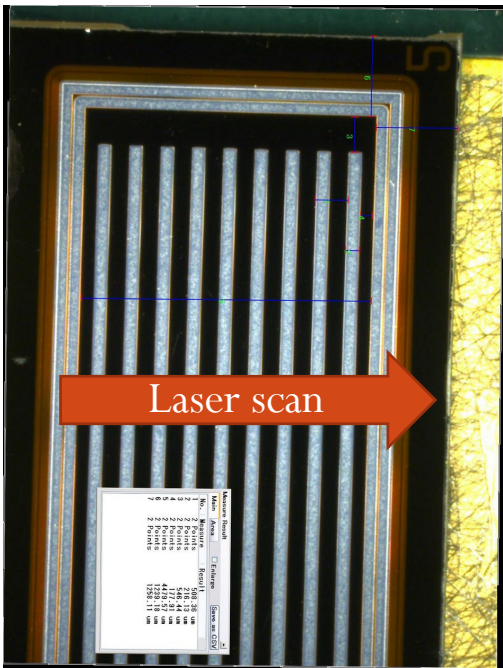
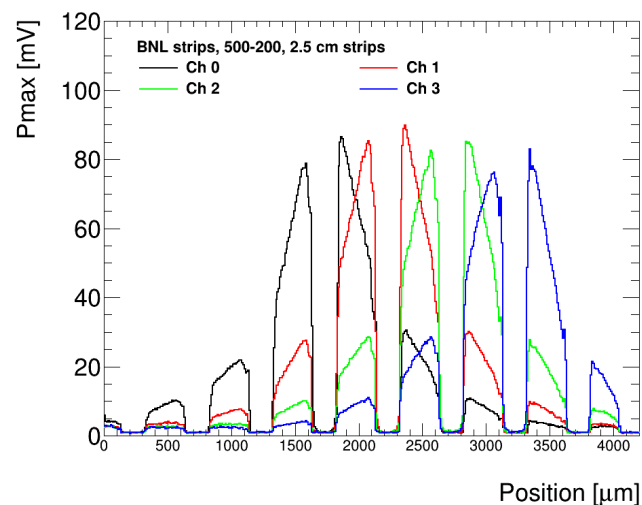
- Radiation levels of $\mathcal{O}(10^{14} \text{ cm}^{-2})$ as predicted for ePIC should not have a significant impact on sensor performance, but **increase in leakage current** needs to be considered
- AC-LGAD pad geometry: **capacitance of AC metal pads represents the input capacitance to the front-end electronics** – important for signal coupling and noise!
 - **Dominated by pad size and geometry**, C increases with size
 - Impact of dielectric negligible for 50 μm sensors, n+ might have an effect
 - Tested at several frequencies
- **Inter pad capacitances**: a factor in the observed higher signal sharing for longer strips
 - Effect clearly seen in data and simulation



Strips laser studies



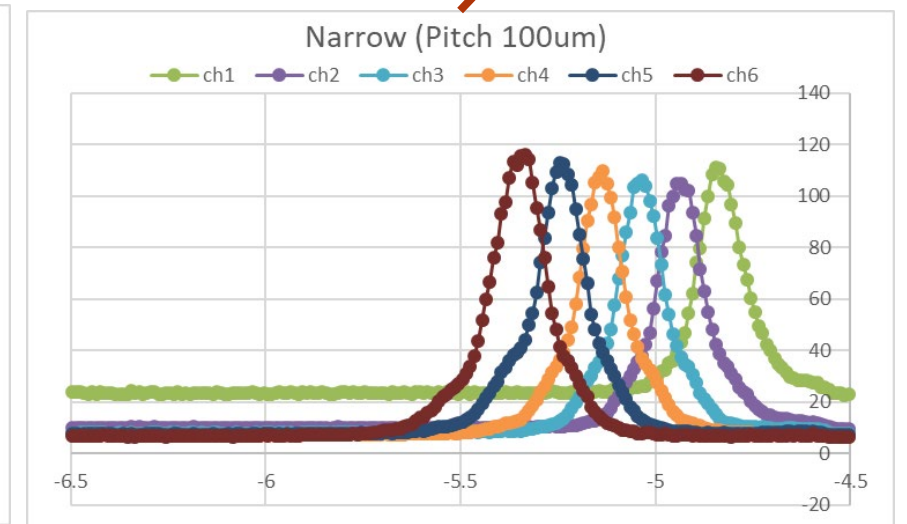
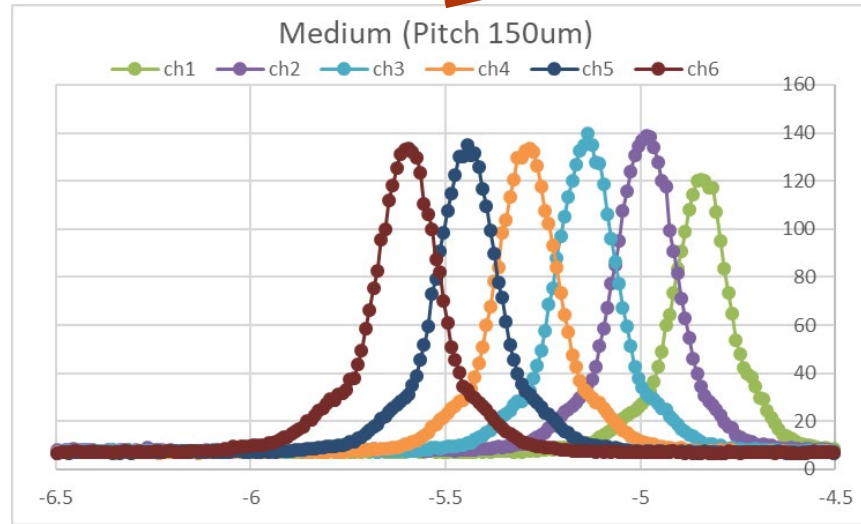
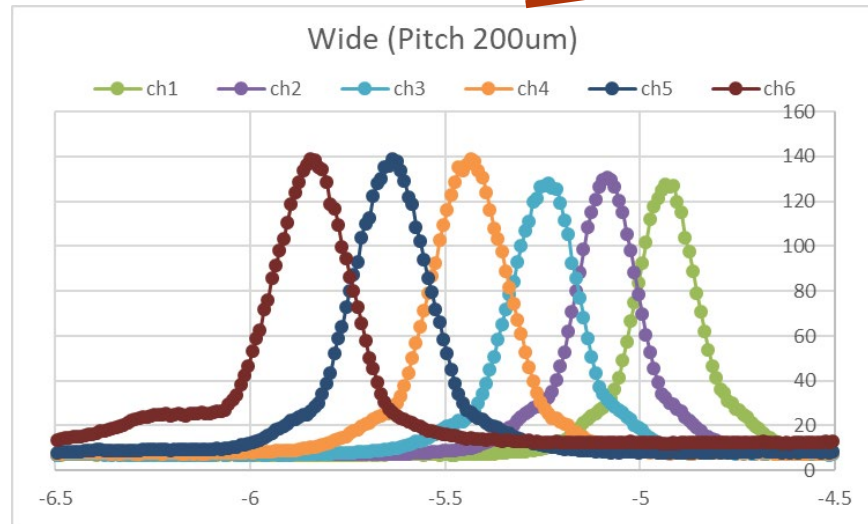
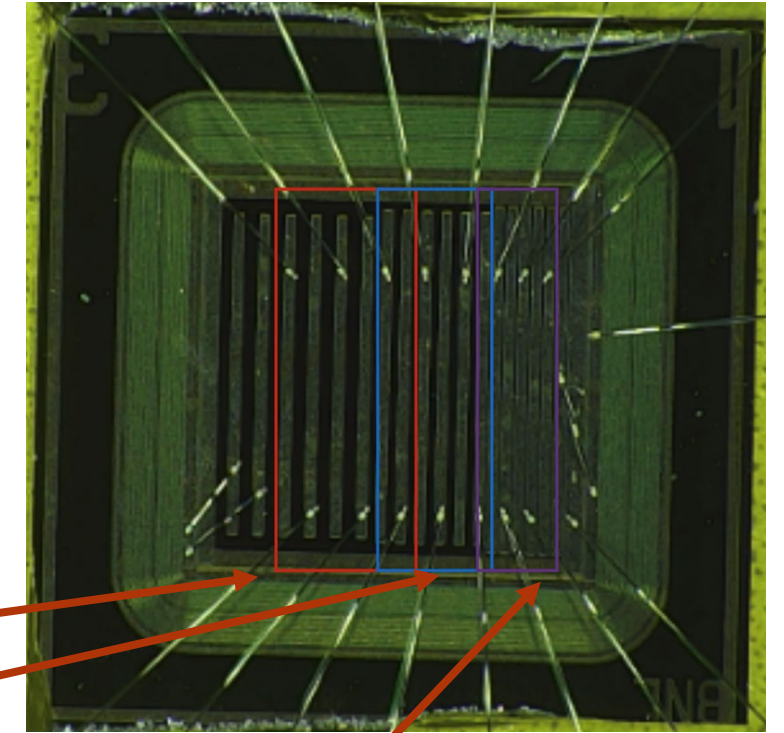
- Effect on charge sharing of pitch and width
- Effect on the charge sharing of the strip length



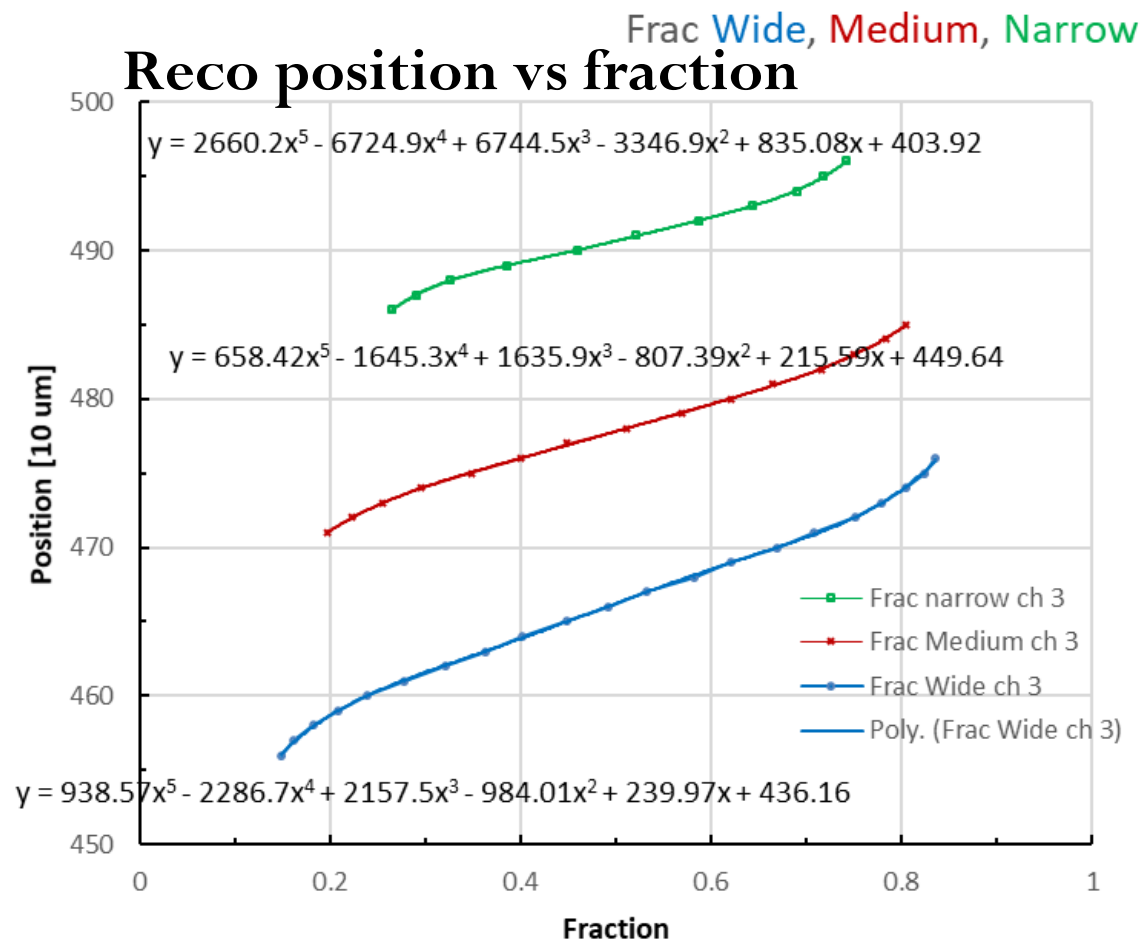
- Charge sharing for long strips (2.5 cm)

FNAL test beam data analysis

- Analyzing data from FNAL test beam 2021 and 2022 (H. Sadrozinski, J. Ott + Students)
- Analysis of BNL strip sensor data
 - Effect on charge sharing of strip pitch
 - Study of large area charge sharing (caused by high energy deposit in the landau tail)
 - Effect on charge sharing of position of wire bond connection on the strip
 - Comparison with laser data and TCAD simulation
- Sensor has strips with pitch 100, 150, or 200 μm , strip metal width always 80 μm
 - Pmax profile as we move across sensor

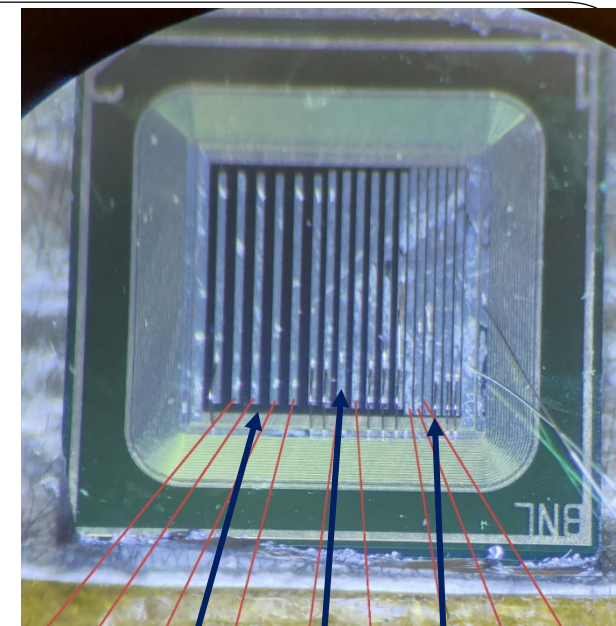
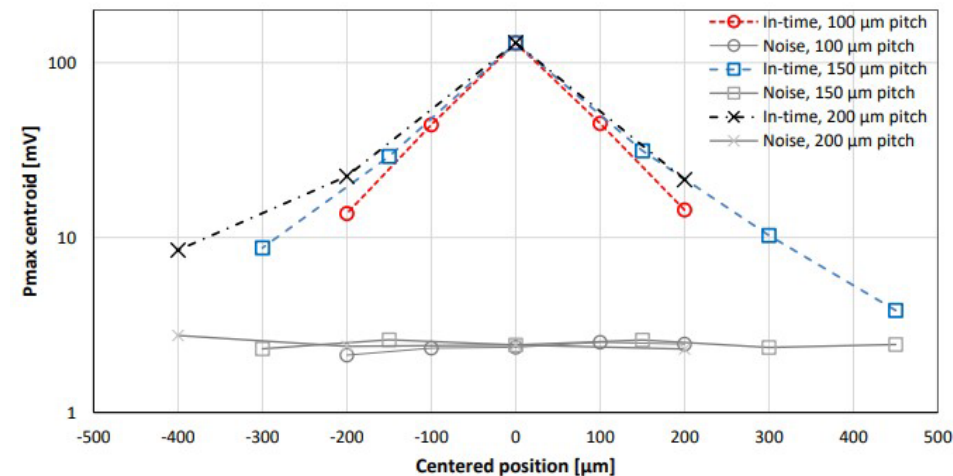


Signal Sharing between neighbors versus location, 5th order polynomial fits, and resulting position resolution

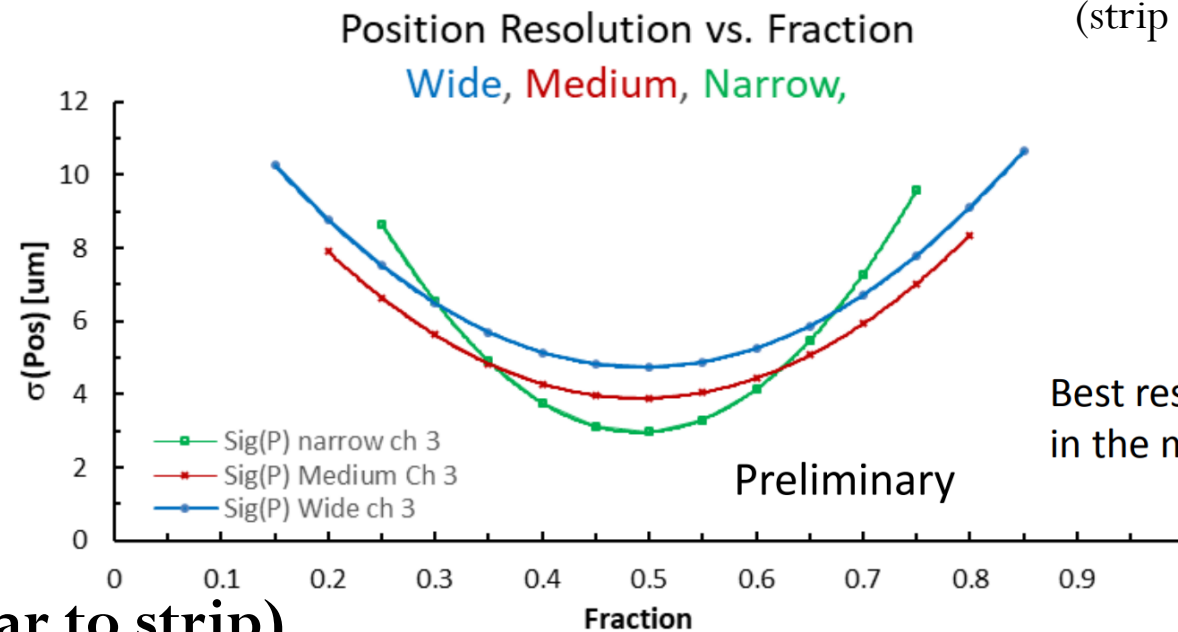


Position resolution between 3-5 μm
in between strips (direction perpendicular to strip)

Logarithmic charge sharing



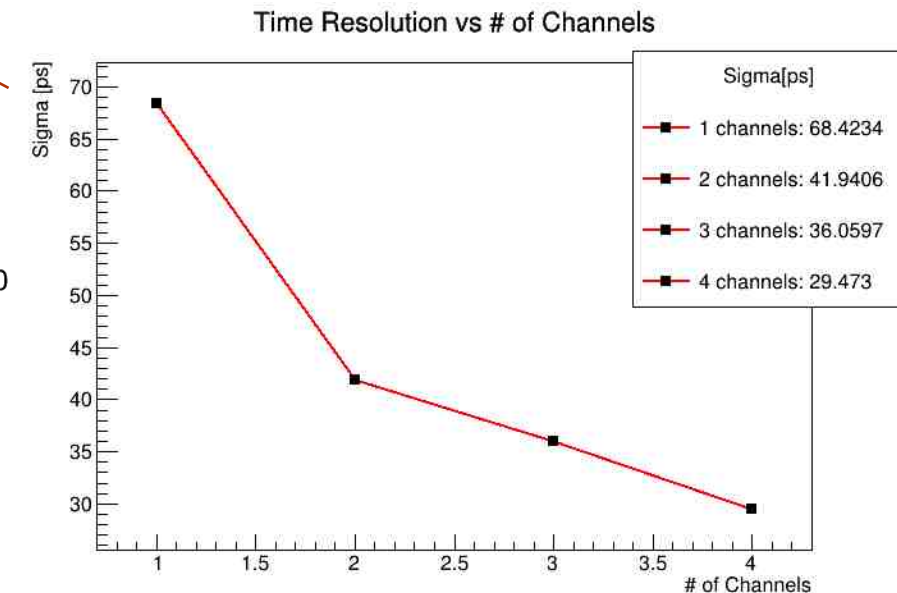
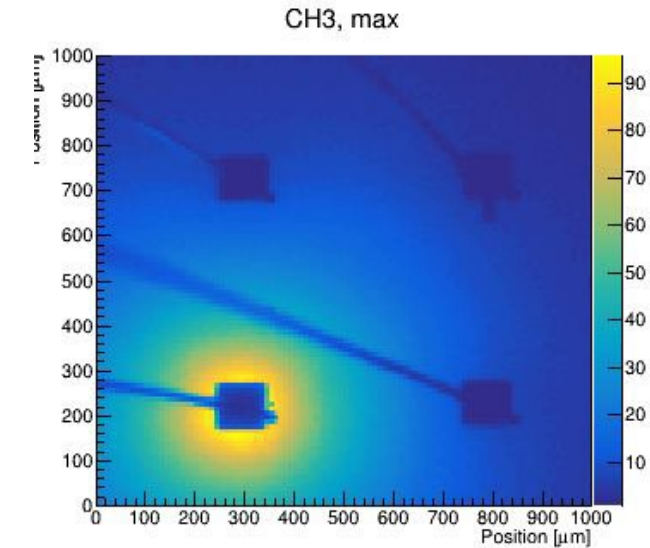
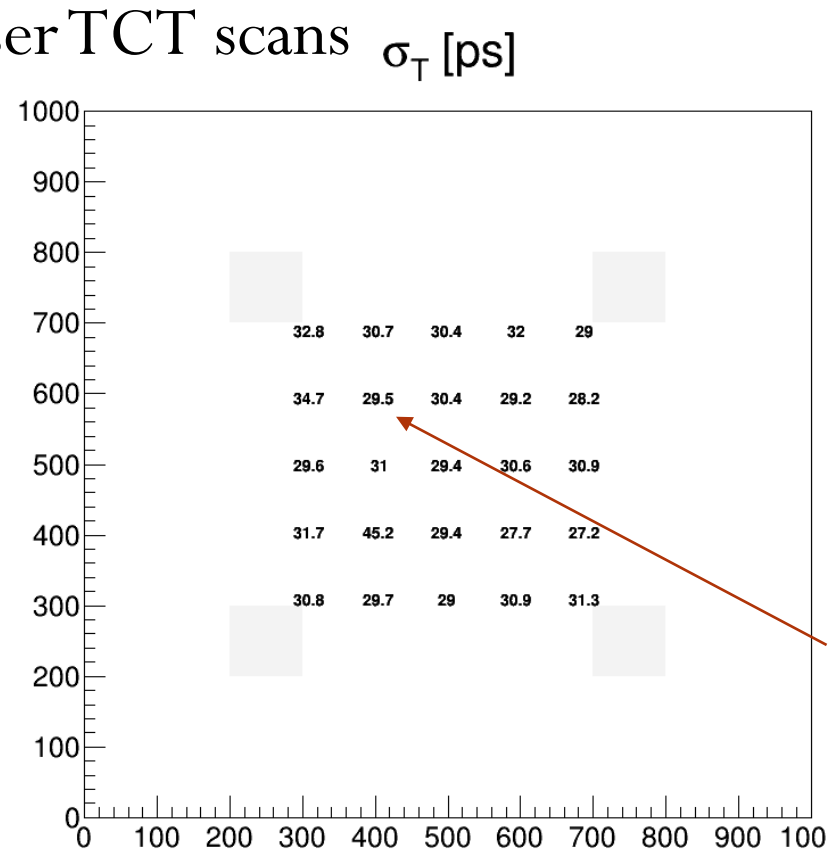
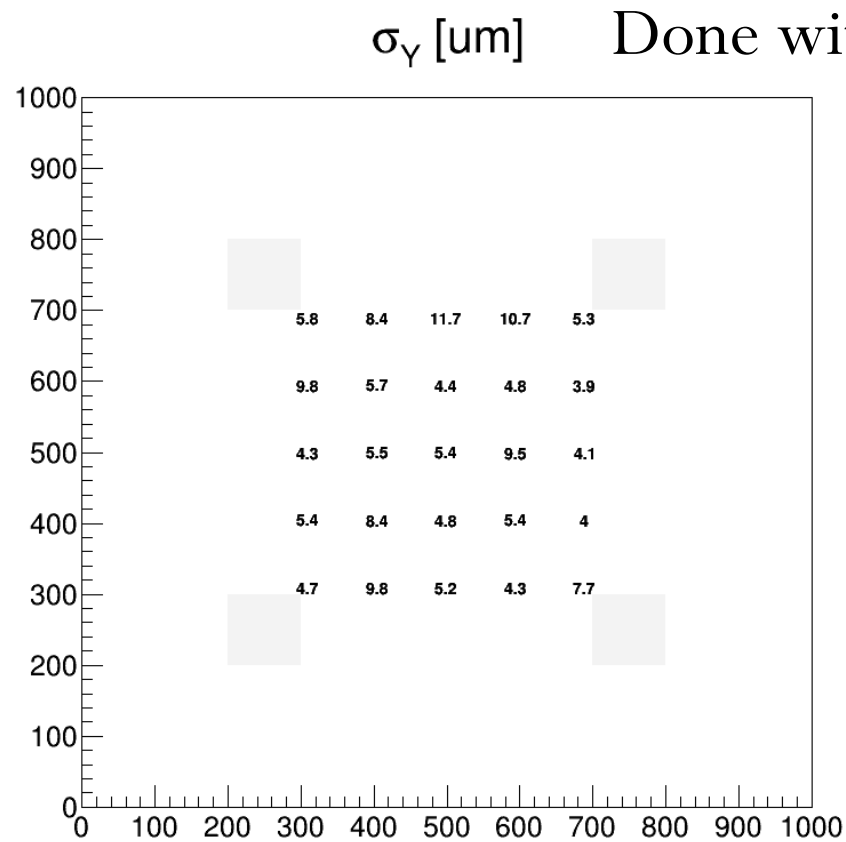
200 μm, 150 μm, 100 μm
(strip width 80 μm)



Best resolution for Frac = 0.5
in the middle between strips!

Estimated reconstructed position resolution and Jitter

FBK AC-LGAD 500 μm pitch, 100 μm pads



Reconstruction algorithm: χ^2 with reference data

See: <https://indico.cern.ch/event/1157463/contributions/4922739/>

Key points

- AC-LGAD can provide very good position (down to pitch/10-100) and time resolution
 - Position reconstruction using charge sharing
 - Combination of time of arrival to improve time resolution
- However many parameters have to be optimized to achieve the perfect performance
 - A range of strip geometries show good results, however very narrow strips (50 microns or less) or long strips (2 cm) have shown too much charge sharing and poor performance (large charge sharing means less charge per electrode, less S/N)
 - Small pads with large pitch show good reconstruction properties and low input capacitance. Pad geometry can be optimized.

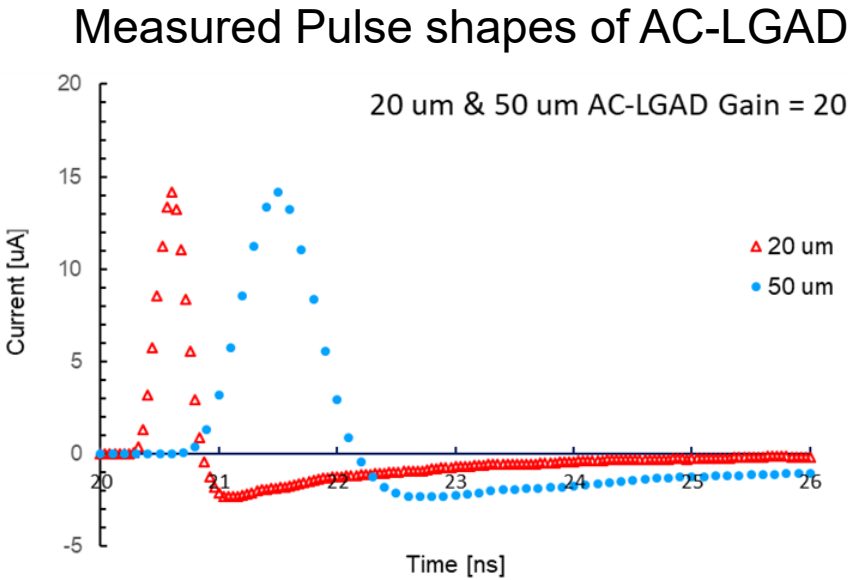
ASIC development and testing



Fast LGAD Read-out ASICs at SCIPP

The development work of LGAD sensors was/is based on high-speed readout boards with discrete components introduced by SCIPP.

The crucial characteristics of LGAD signals were mapped out.



LGAD Characteristics	50 um	20 um
Rise Time (10-90%) [ps]	455	182
Input Charge (G = 20) [fC]	11	4.6
I_{MPV} Input Current [uA]	15	15

Design Goals

ASIC Parameter	50 um Sensor	20 um Sensor	Comment
Rise time (10 – 90%) [ps]	455	182	Rise time (electronics) = Rise time (sensor signal)
Jitter [ps]	10	5	< 30 % of the predicted “Landau” Noise
S/N	> 50	> 40	S/N = Rise Time / Jitter
Voltage signal [mV]	70	70	$V_{MPV}=R_{FB} * I_{MPV}$, [$R_{FB} = 5\text{ k}\Omega$]
Noise RMS [mV]	1.4	1.8	
Internal Sensor Gain	> 20	> 20	

It allowed to come up with specifications for different applications in terms of temporal and spatial resolution and the double pulse capability and translate them into required performance parameters for ASICs (“Design Goals”).

<https://doi.org/10.1016/j.nima.2020.164615>

Per-channel power draw to be minimized!



ASICs under Development/Test at SCIPP

Based on the Specifications, three ASICs are being produced which will emphasize different performance goals.

Here we leverage our partner’s familiarity with the technology and our experience with sensors and readout systems.

HPSoC and ASROC being developed in collaboration with SCIPP

SCIPP role: guiding the chip development, development of electronic board for chip characterization, testing the chip performance with calibration input and with an LGAD sensor with laser and Sr90 source

Lead Institution		Technology	Output	# of Chan	Funding	Specific Goals	Status
INFN Torino	FAST	110 nm CMOS	Discrim. & TDC!	20	INFN	Large Capacitance TDC	Testing, new update in a few months
NALU Scientific	HPSoC*	65 nm CMOS	Waveform	5 (Prototype) > 81 (Final)	DoE SBIR	Maximize timing precision Digital back-end	Testing
Anadyne Inc	ASROC**	Si-Ge BiCMOS	Discrim.	16	DoE SBIR	Maximize timing precision Low Power	Simulations final Layout Board design

* HPSoC : High Pitch digitizer System on a Chip,
(L. Macchiarulo et al.: “Design of HPSoC - a 10GSa/s Waveform Digitizer for Readout of Dense Sensor Arrays”, submitted to IEEE NSS-MIC 2022)

** ASROC: A custom amplifier/discriminator IC designed for AC-LGAD readout,
(G. Saffier-Ewing et al., “ASROC: A custom amplifier/discriminator IC designed for AC-LGAD readout“ , TWEPP 2021)

Further Details of ASIC Initiatives

FAST ASIC (INFN)

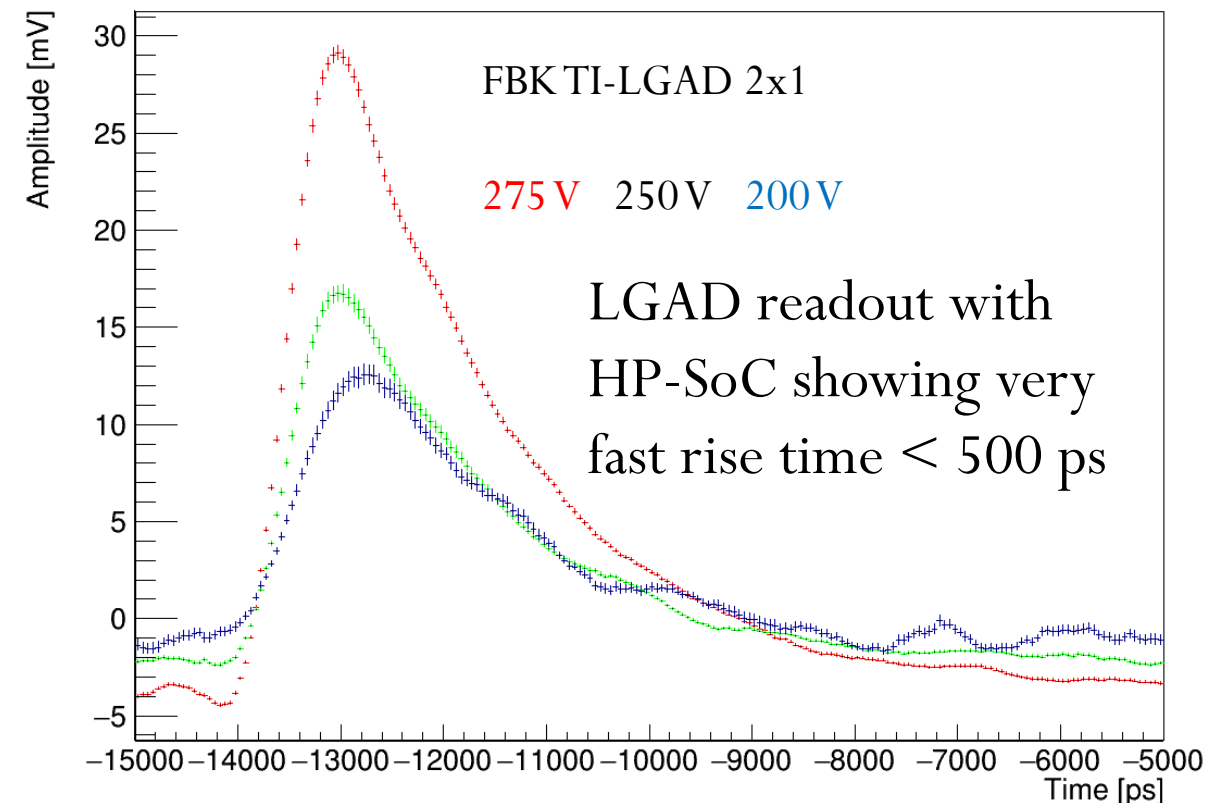
- Longer shaping time (> 800 ps) not optimized for thin sensors (200–500ps signal rise)
- Power draw: 1 mW/channel for analog, 1 mW/channel for discriminator/TDC
- New design (FAST3) ready soon

ASROC ASIC (Anadyne Inc)

- Uses fast SiGe process for front end
- Promising design but prototype not yet in hand
- Front-end power draw good (< 1 mW) but not clear it can be mated to low-power CMOS for back-end
- Future funding sources unclear

HPSoC ASIC (Nalu Scientific)

- Full, highly flexible “system on chip” (SoC)
- Both front and back end carefully optimized for timing precision
- Integrated 65 nm process promises low power for full readout chain
- Ongoing project with DOE recognition and support
- Prospective performance characteristic on following page
- Power draw: 1.6 mW/ch for analog, 1 mW/ch for digitizer and 1 mW/ch for digital. Current goal, still under development



HP-SoC future development

- Next HP-SoC prototype will address issues (low gain) while maintaining the good proprieties (fast rise time)
 - Final goal: 10 ps of Jitter
- Unfortunately HP-SoC Phase II SBIR was not granted despite positive reviews
 - Currently there's no money to go forward
 - Need funding, no active grant at the moment
- Other funding sources are being pursued
 - SBIR phase I submittal for NP soon
 - DoE supplemental funding (small) to address issue with digital part
 - Jlab “GENERIC EIC-RELATED DETECTOR R&D PROGRAM”, applied few months ago
- The scope of each funding is different (aimed at different details of the development)

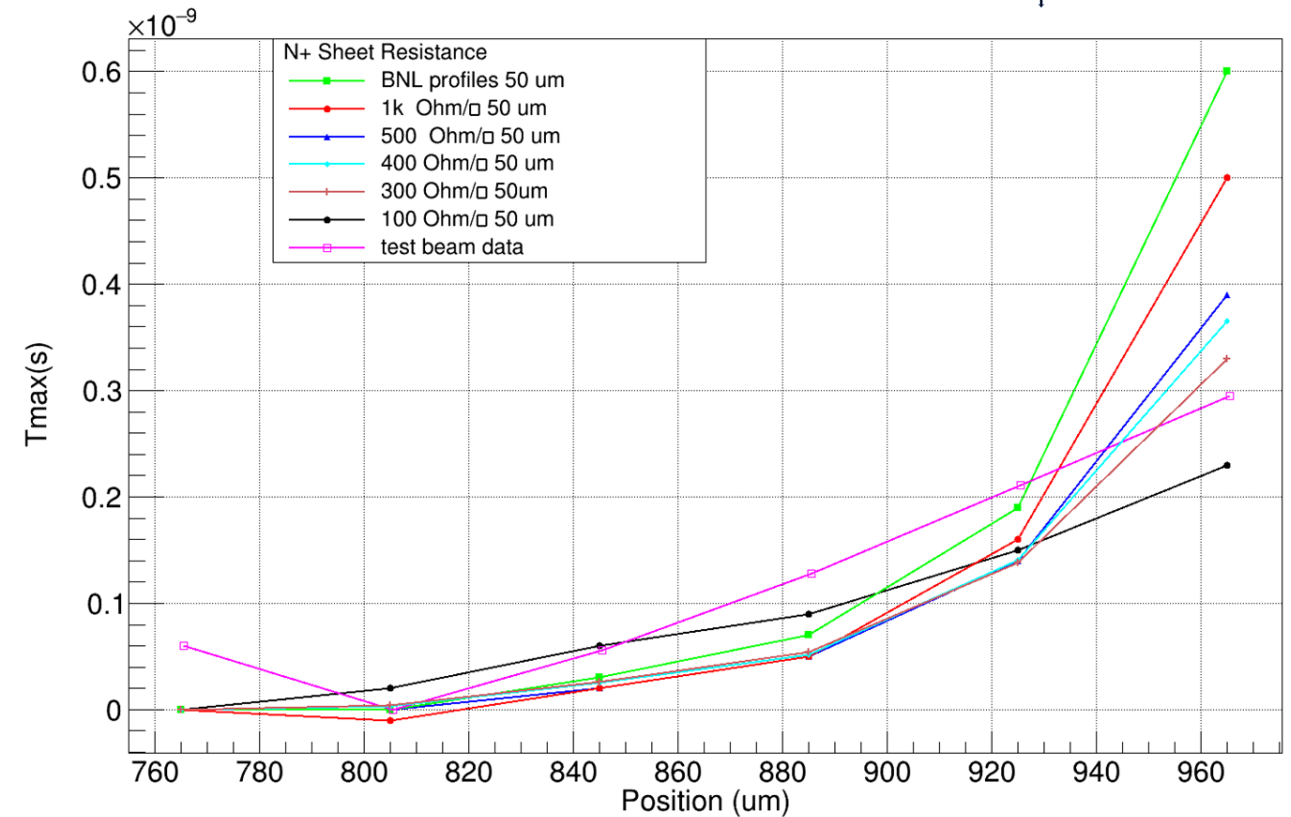
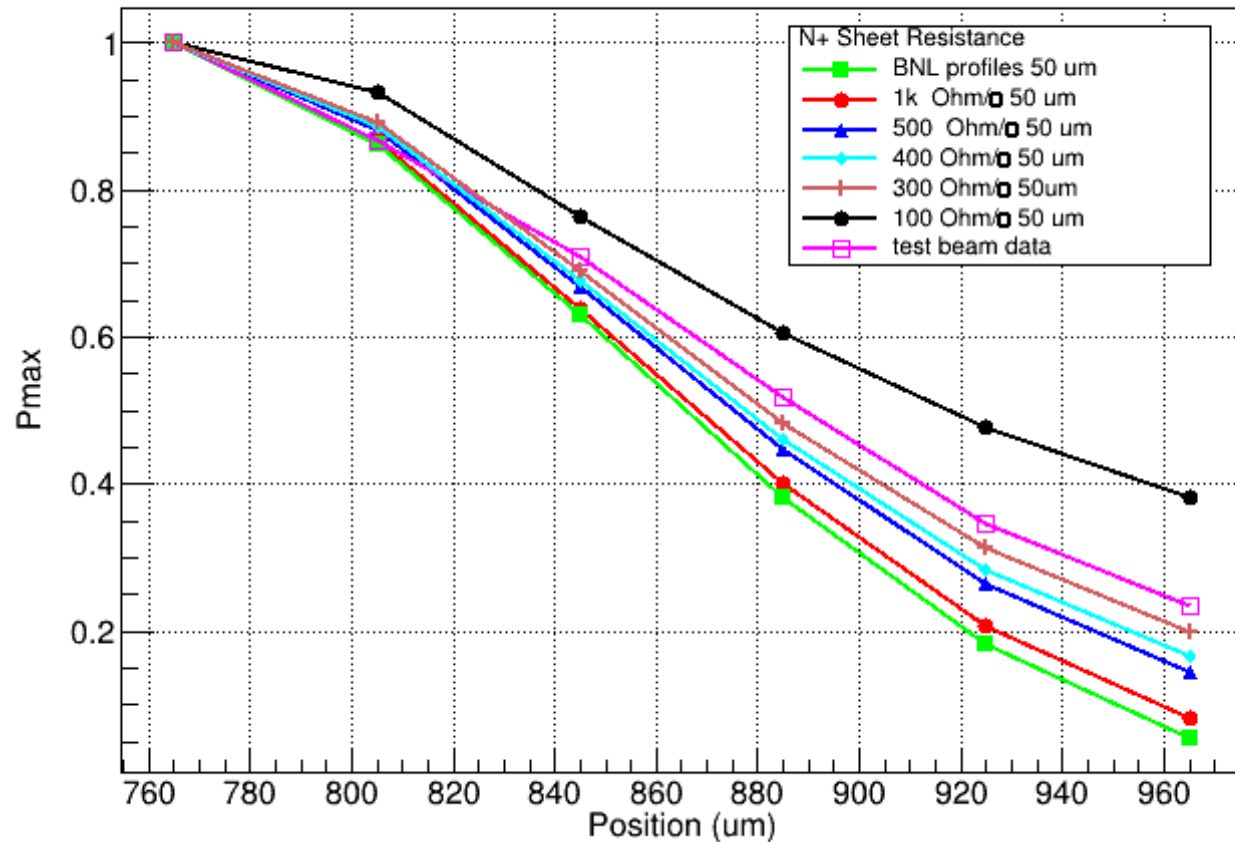
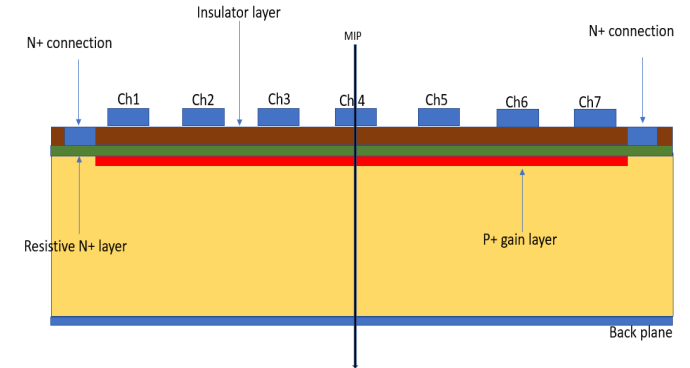
TCAD simulation

TCAD simulation studies

- TCAD simulation of AC-LGADs with two different software (TCAD silvaco and TCAD sentaurus)
- Tuned the simulation to correctly describe the behavior of sensor prototypes from laser and TB measurements using doping information from BNL
- Most relevant studies are
 - 2D studies in Silvaco on effect of N⁺ sheet resistance (Mohammad Nizam)
 - 2D/3D studies in Sentaurus on strip-length effects (Kyung-Wook “Taylor” Shin)
 - 3D studies of gain (including gain suppression) (Yuzhan Zhao (GS))
- **These are important for understanding signal-shape and charge-sharing characteristics** that will impact both the temporal and spatial resolution
- These studies are **expected to provide guidance for further sensor prototyping**
 - Optimize N⁺ resistivity and doping values
 - Identify the best geometry for EIC (size, pitch, length)
 - Effects of the sensor thickness and other parameters

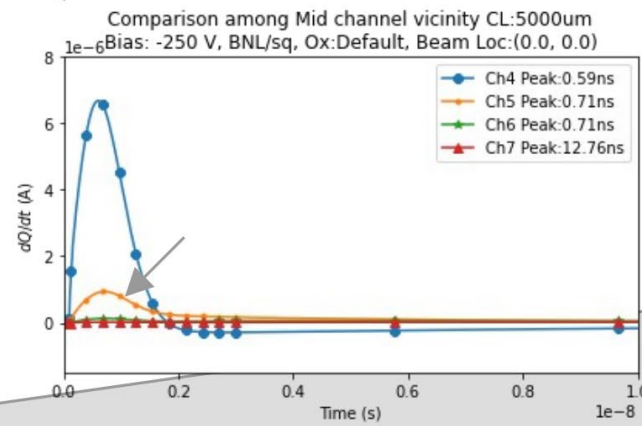
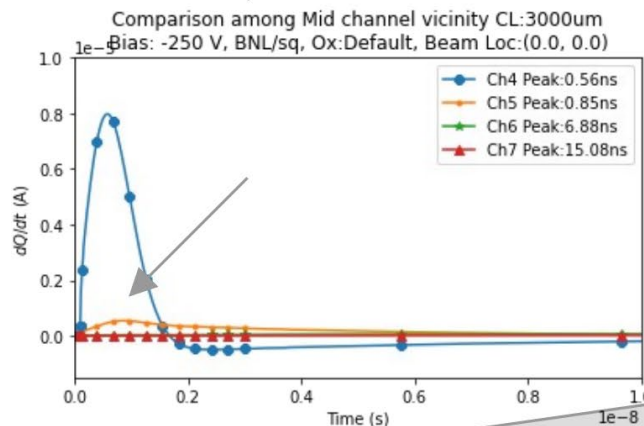
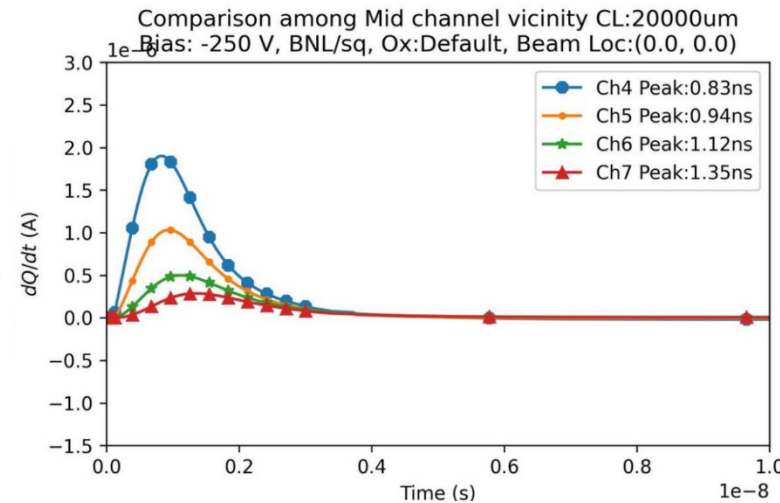
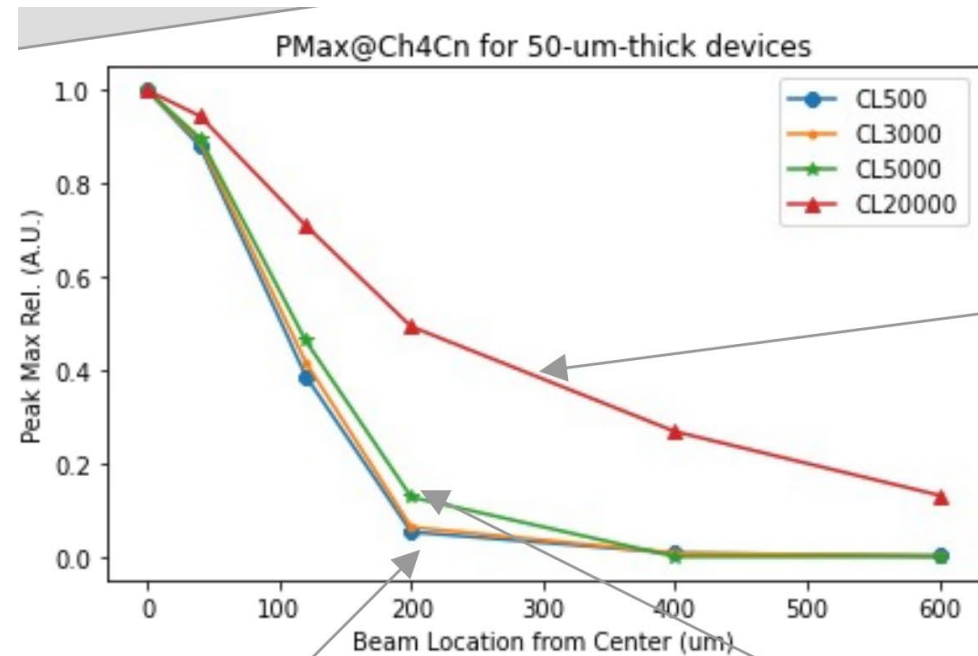
TCAD silvaco simulation, with different N+ variation. Comparison of Pmax and Tmax with TB data with 3 mm strips

Bulk=50 μm , Pitch=200 μm Metal=80 μm



Test Beam data from Marcus Wong (PhD student)
(shown before in slide 9)

3D TCAD Sentaurus strip length studies



Simulation of 200 um pitch strip device with 7 channels

- Strip lengths of 500um to 2cm simulated
- As we increase the strip length, the neighboring crosstalk increases
- The pulse itself is degrading with long strip devices such as 2 cm
 - Longer tail and almost no undershoot

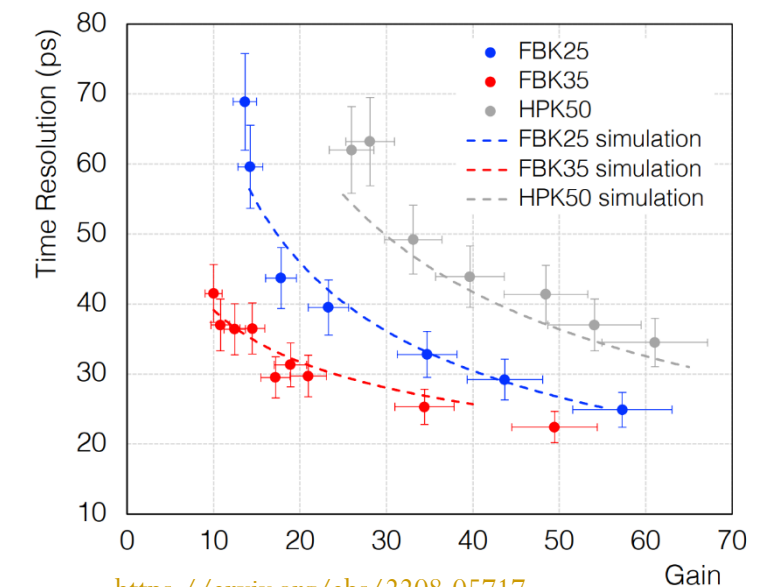
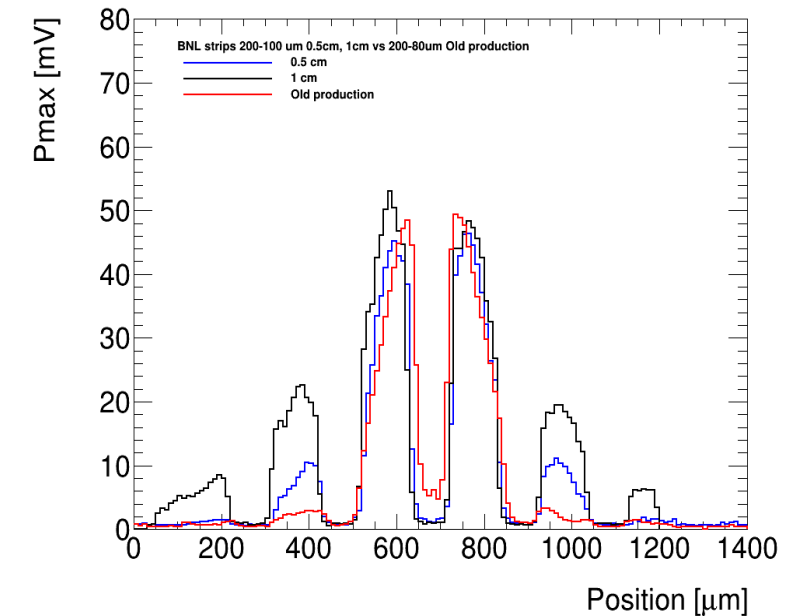
- Behavior observed in actual data!
- Therefore, we can say that increasing the length of the strip device has some negative effects on the results

Note: these effects are only seen when running a full 3D simulation, not seen for 2D simulation

Conclusions

Future sensor productions inputs

- **A range of strip geometries show good results**, however very narrow strips (50 μm or less) or long strips (2 cm) have shown too much charge sharing and poor performance. Study done with BNL sensors.
 - **Strip geometry (width, pitch, length) greatly affects charge sharing**
- **TCAD simulations provide guidance detector parameters:** pitch, metal width, strip length, sensor thickness
- **Studied 500x500 pitch pads with different size and geometries** (other shapes, e.g. circles, can simplify reconstructions)
 - <10 μm position resolution and 30 ps time resolution
 - Increase pitch? For example would 700 μm pitch be ok, saving on channel count, especially for pixels?
- **Thickness is also an open question:** 20 μm and 35 μm thick devices show better time resolution than standard 50 μm . However input capacitance is higher.
 - Better sensor resolution doesn't help if ASIC jitter is $\sim 30\text{ps}$
 - First BNL 20 μm production is ready and will answer many questions
- **Possibility to work with FBK to have a EIC specific production?**
 - They produced high quality AC-LGADs and thin devices (25 μm , 35 μm)
 - Are very open to R&D sensor productions and known to successfully pursue new projects



<https://arxiv.org/abs/2208.05717>

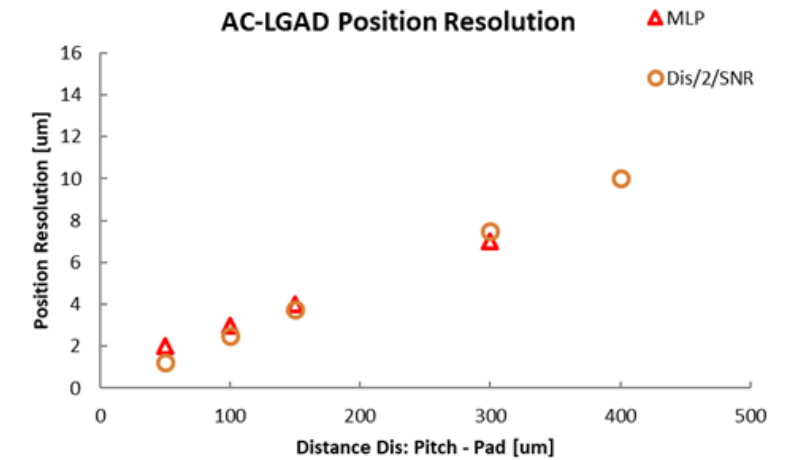
SCIPP contributions and manpower

- **Key points:**

- AC-LGAD can provide very good position (down to pitch/ 10-100) and time resolution
- However many parameters have to be optimized to achieve the perfect performance
- TCAD simulation can be extremely helpful in guiding sensor production

- **SCIPP plans for the next year**

- Continue the **laboratory testing of LGAD prototypes from BNL and other vendors**
- Exploration of **20 um thin detectors**
- **TCAD simulations** to answer the following questions: Optimal strip length, Sheet resistance studies, Charge sharing effects
- **Continue ASIC development with companies** (through SBIRs or other funding)
- Analyze test beam data from FNAL 2022 and next one in 2023
- Manpower at SCIPP on EPIC
 - 3 Faculty (20% FTE) + 1 junior faculty (30% FTE), 1 staff scientist (30% FTE), 3 technical staff (20% FTE), 2 postdocs (40% FTE), 3 PhD students, ~8 undergrad students



SCIPP contributors

- Hartmut Sadrozinski (Faculty)
- Bruce Schumm (Faculty)
- Abe Seiden (Faculty)
- Matthew Gignac (Junior faculty)
- Simone Mazza (Staff Scientist)
- Jennifer Ott (Post-doc)
- Mohammad Nizam (Post-doc)
- Taylor Shin (Technical staff)
- Max Wilder (Technical staff)
- Forest Martinez-McKinney (Technical staff)
- Serguei Kachigun (Technical staff)
- Nicolo Cartiglia (Visiting, INFN Torino)
- Alejandro Rojas (Visiting, INFN Torino)
- Yuzhan Zhao (PhD student)
- Adam Molnar (PhD student)
- Miguel Escobar (PhD student)
- C. Bishop, A. Das, A. Summerel, J. Ding, N. Yoho, T. Stern, N. Mobtaker, S. Letts (Undergraduate students)
 - Students supported by DoE grant

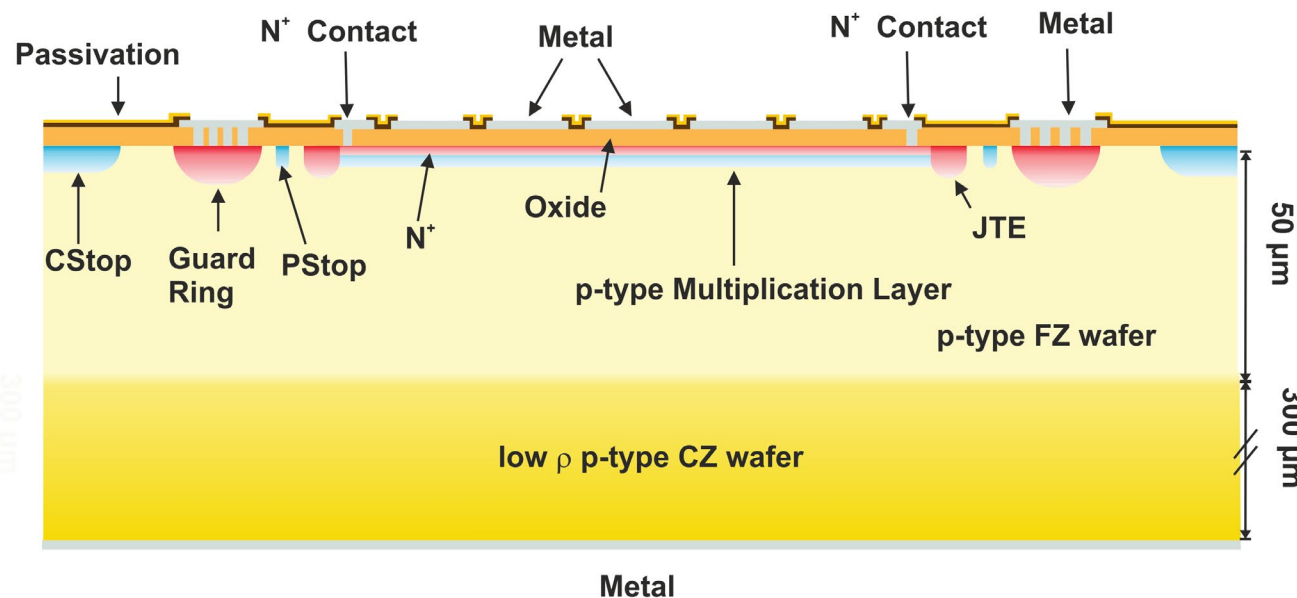
Reference slides

- Laboratory sensor testing contributions during US-Japan (UCSC, KEK, BNL, FNAL) meetings
 - https://indico.cern.ch/event/1121021/contributions/4706804/attachments/2384599/4075195/221221_AC_strips.pdf
 - https://indico.cern.ch/event/1131856/contributions/4749535/attachments/2397533/4099660/230222_AC_strips.pdf
 - https://indico.cern.ch/event/1146890/contributions/4814022/attachments/2423028/4150178/300322_BNL_AC_strips_old_new.pdf
 - https://indico.cern.ch/event/1180221/contributions/4956851/attachments/2477093/4251546/300622_BNL_strips_double_channel_readout_2.pdf
- Study of the effect of the metal electrode shape in pad AC-LGAD (<https://indico.cern.ch/event/1157463/contributions/4922739/>)
- Test beam analysis contributions during US-Japan (UCSC, KEK, BNL, FNAL) meetings
 - https://indico.cern.ch/event/1044975/contributions/4663819/attachments/2394229/4093863/JOtt_VCI2022_ACLGADs.pdf
 - https://indico.cern.ch/event/1149759/contributions/4824988/attachments/2424585/4156241/pulse_sharing.pdf
 - https://indico.cern.ch/event/1166218/contributions/4897977/attachments/2456016/4209530/sean_letts_6_3_22.pdf
 - [https://indico.cern.ch/event/1180221/contributions/4956850/attachments/2477075/4251509/7_1_22%20\(2\).pdf](https://indico.cern.ch/event/1180221/contributions/4956850/attachments/2477075/4251509/7_1_22%20(2).pdf)

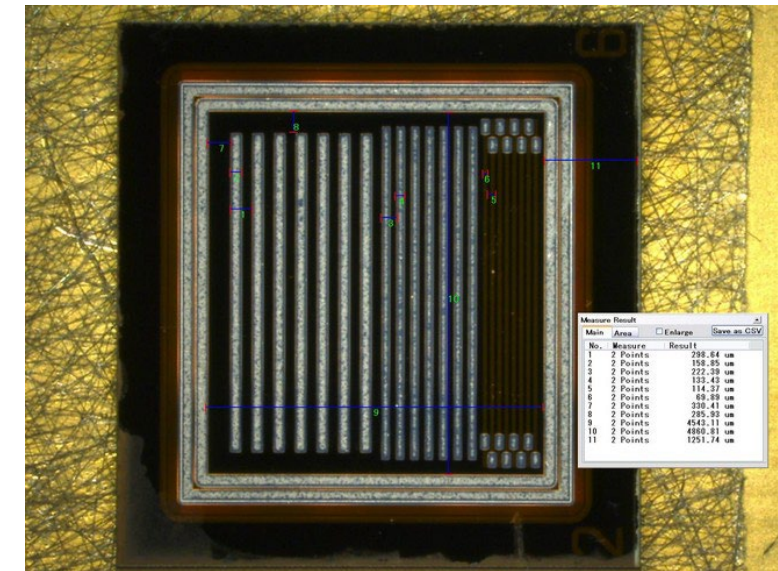
Backup

Recap - AC-LGADs

- Most advanced prototype of high granularity LGADs are **AC-LGADs**
 - (UCSC - US patent N. 9,613,993 B2, granted Apr. 4, 2017)
- Continuous sheets of multiplication layer and **N⁺ resistive layer**
 - N⁺ layer is grounded through side connections
- **Readout pads are AC-coupled** (Insulator layer between N⁺ and pads)
 - Allows for 100% fill factor and fine segmentation
- **Intrinsic charge sharing** between metal electrodes
 - Allows for precision hit precision better than $\sqrt{12}$
 - 5 μm precision achievable for 500 μm pitch



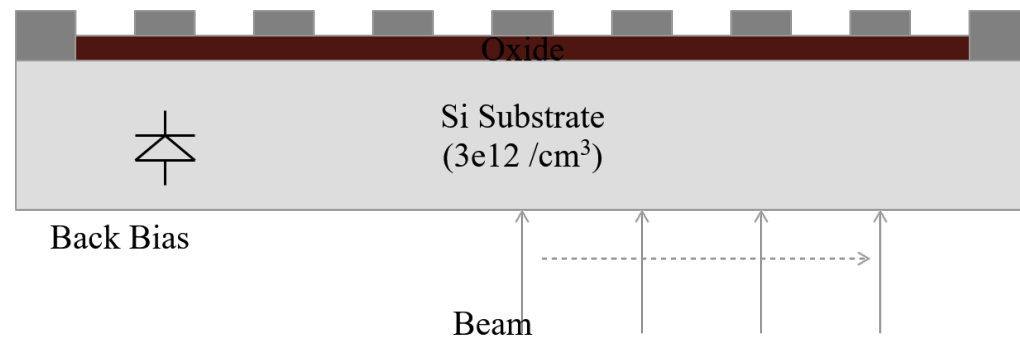
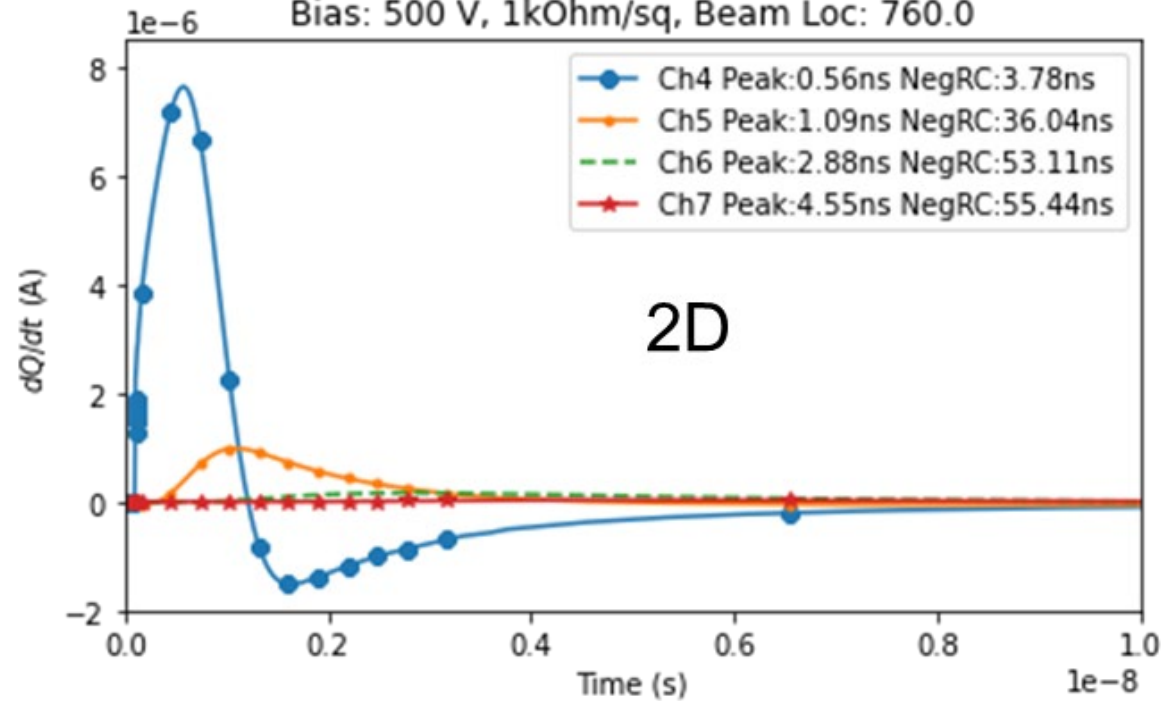
- **The response of the sensors can be tuned by modifying several parameters**
 - Pad distance
 - Resistivity of N⁺ layer
 - Oxide thickness
 - Pad geometry and dimension



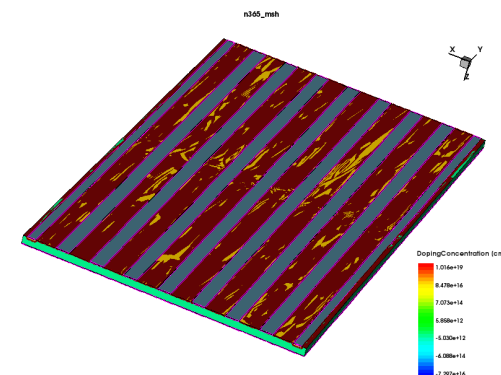
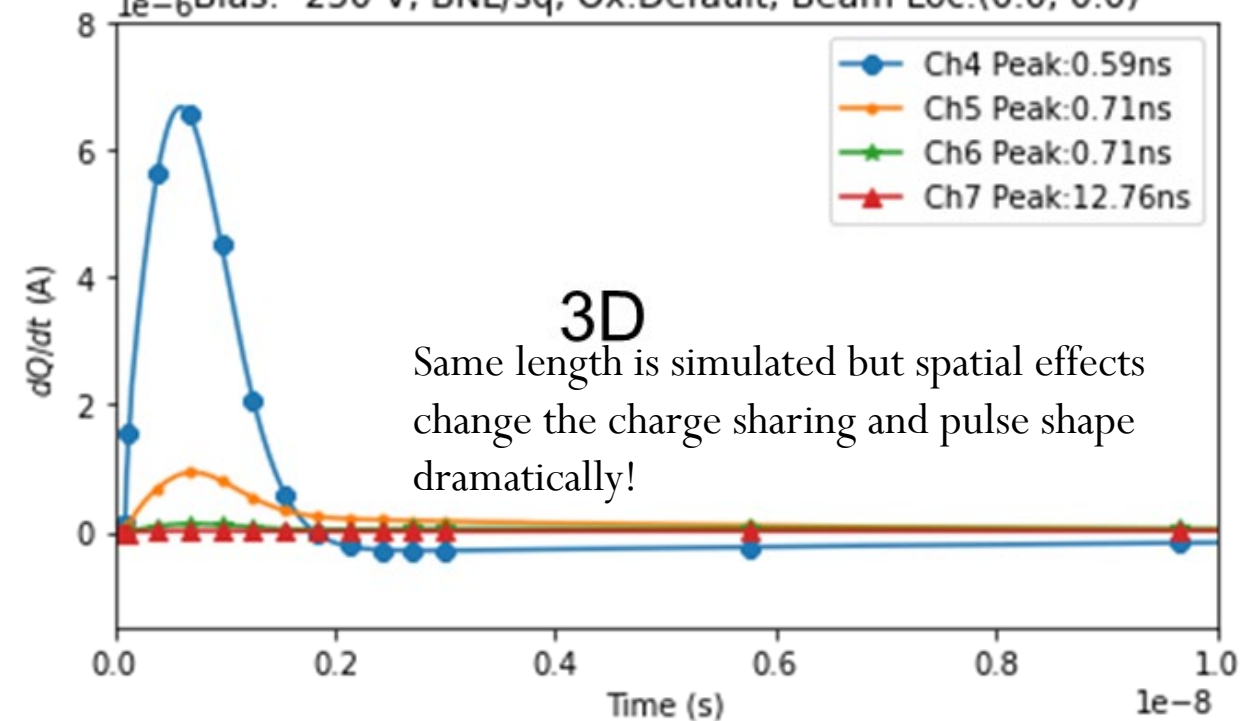
Prototype AC-LGAD from BNL, different geometry strips

2D vs 3D TCAD sentaurus simulation

Comparison between Ch4 vs. Ch5
Bias: 500 V, 1kOhm/sq, Beam Loc: 760.0

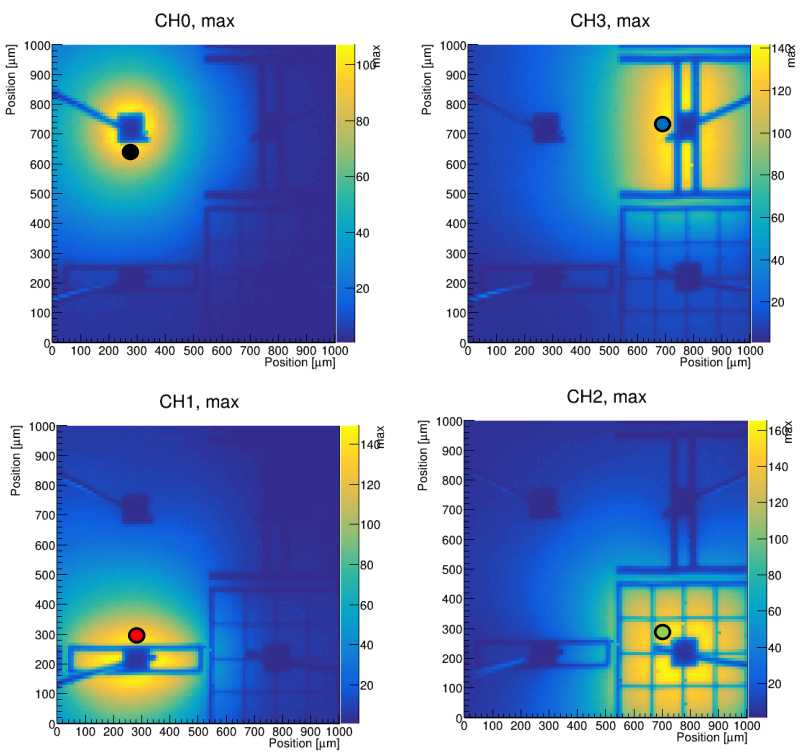


Comparison among Mid channel vicinity CL:5000um
Bias: -250 V, BNL/sq, Ox:Default, Beam Loc:(0.0, 0.0)



The much more time-consuming 3D program is needed when instead of readout pads long strips are considered, where the length of the strips (running into the paper) is important. Both the maximum pulse height (Pmax) and the time of arrival of the pulse (Tmax) of the 3D program describe faithfully the observed pulse shapes.

Different pixel geometries, FBK RSD2 production

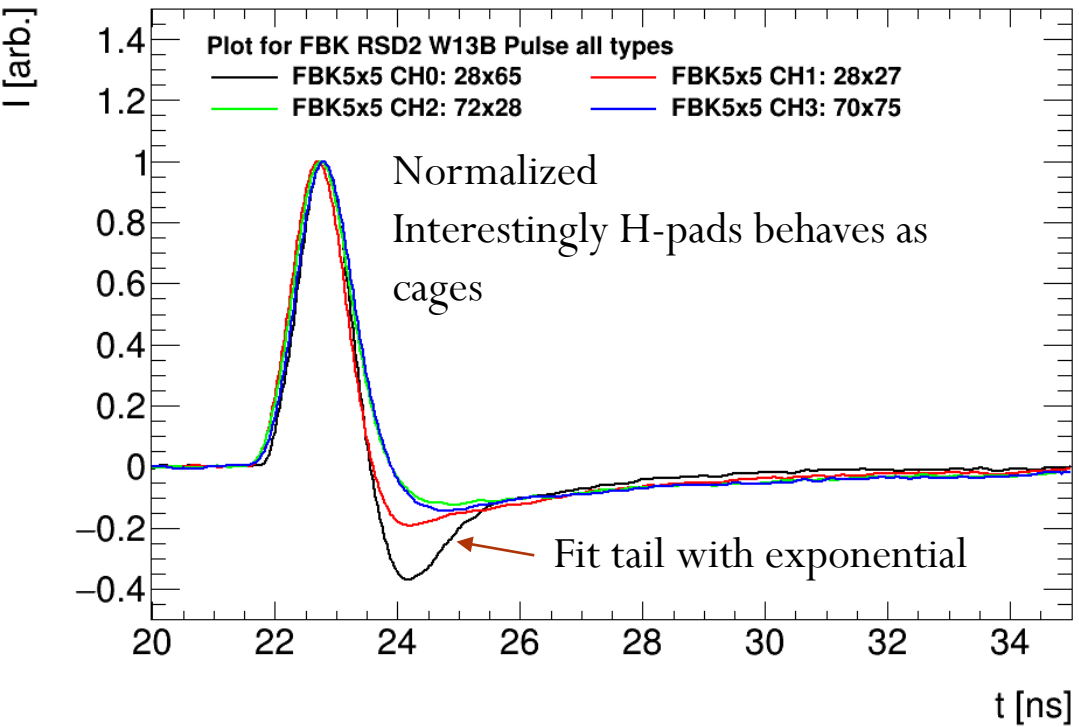
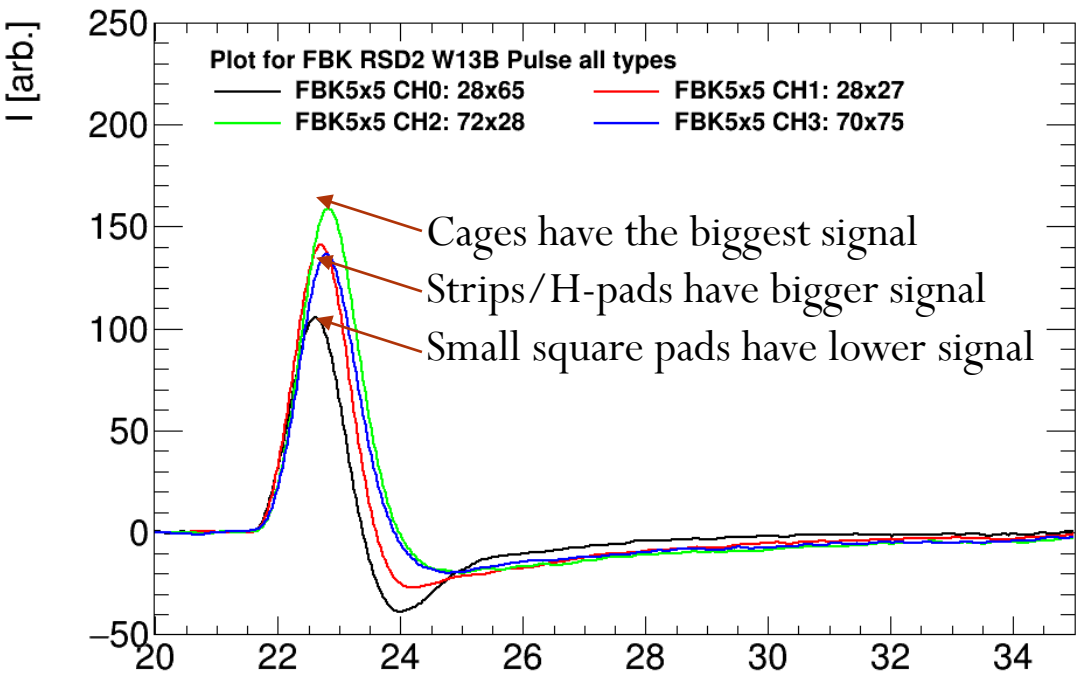


Positive pole of the signal is the same for all pad types

However they have different RC constant and return to baseline

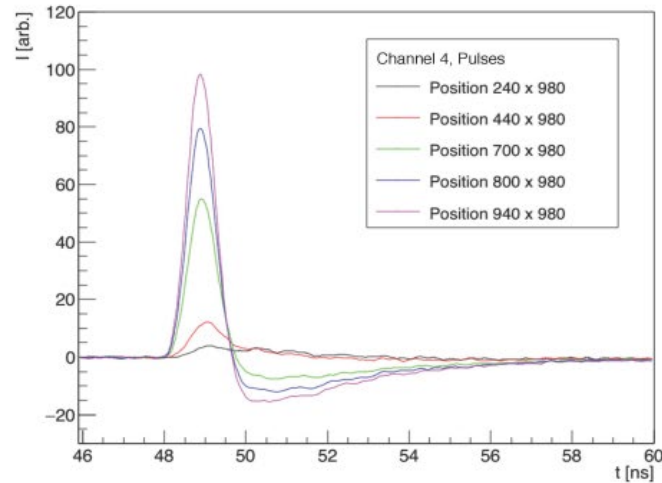
Unclear why it doesn't scale directly with the capacitance of the pad

Pad type	Exponential RC constant	Capacitance
Square pads	0.61	94 fF
Micro-strips	0.28	299 fF
H-pads	0.19	639 fF
Cage	0.19	801 fF

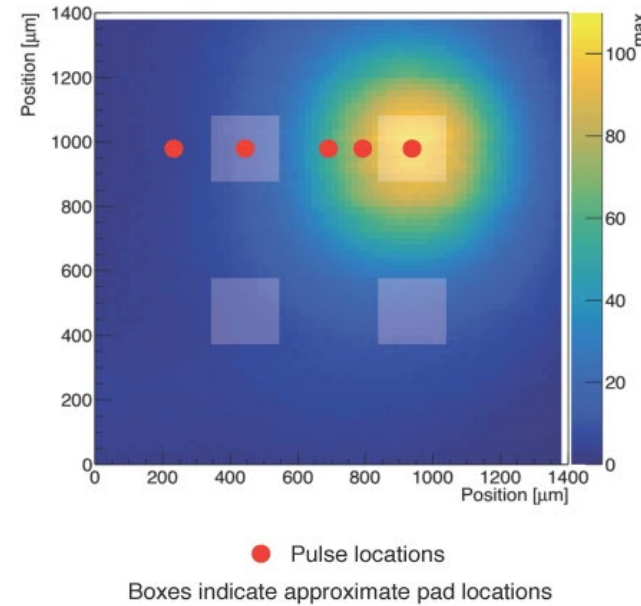


Pixel laser studies – FBK RSD1 production (pads 500um pitch)

Channel 4, Pulses



Channel 4, Pmax



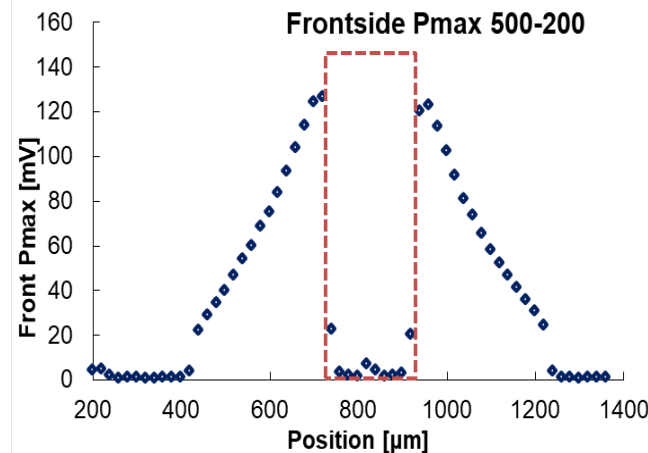
Pixel Pitch = 500μm, Pad Size = 200μm

Pmax under next neighbor pad: ~ 10% of hit pad.

Pmax beyond next neighbor pad: less than 2%.

No direct capacitive pick-up between pads.

Pulses have very consistent rise and fall times. 10-90% rise-time about 530 psec. Different amplitudes basis of position interpolation.



Pulse maximum decreases nearly linearly. The coordinate along the direction we are scanning, referenced to the center between the pads, is therefore approximately: $x = (P1 - P2)/(P1+P2)$. The expected error on x in linear approximation is:

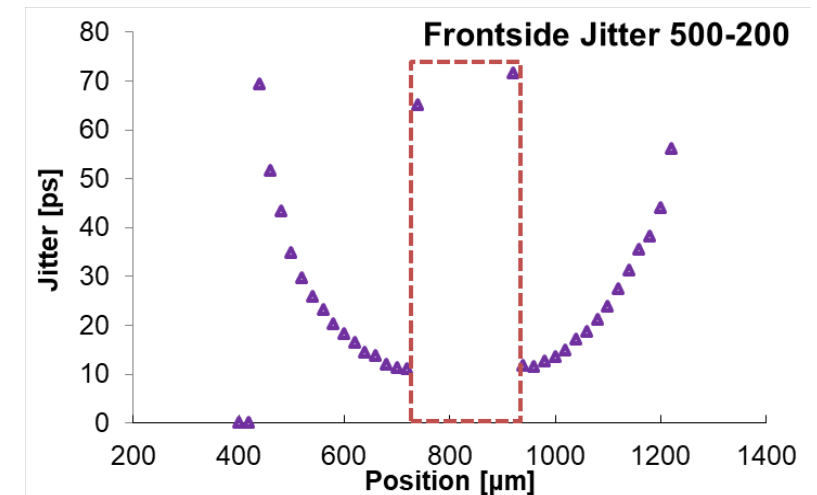
$$\sigma_x = [\text{Interpad Spacing} / \text{signal-to-noise ratio}] f$$

f is a factor near 1: $[0.5 / (\text{maximum value of } (P1-P2)/(P1+P2))] \sqrt{(P1^2 + P2^2)/(P1+P2)}$.

We have a collection of times measured on several pads to combine. (Assume any systematics have been corrected). The jitter for each is then estimated to be $T_{\text{MAX}} / (P_i / \sigma_{\text{NOISE}})$. Assuming that T_{MAX} and σ_{NOISE} are in common we can then calculate that the best estimate for the time and its error are;

$$t = \sum t_i P_i^2 / \sum P_i^2 \quad \text{with} \quad \sigma_t = T_{\text{MAX}} / [\sqrt{\sum P_i^2} / \sigma_{\text{NOISE}}]$$

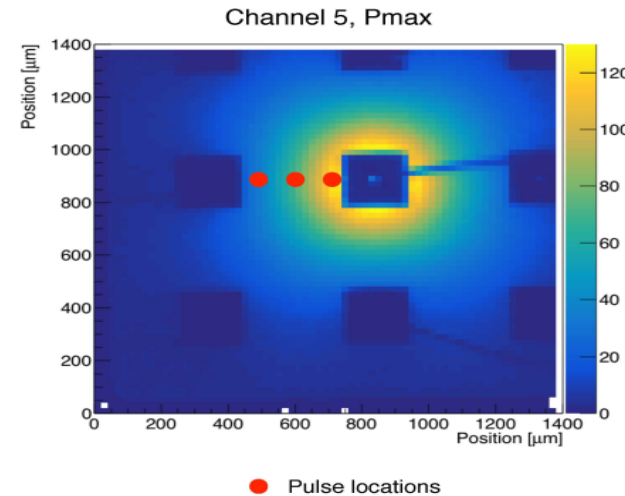
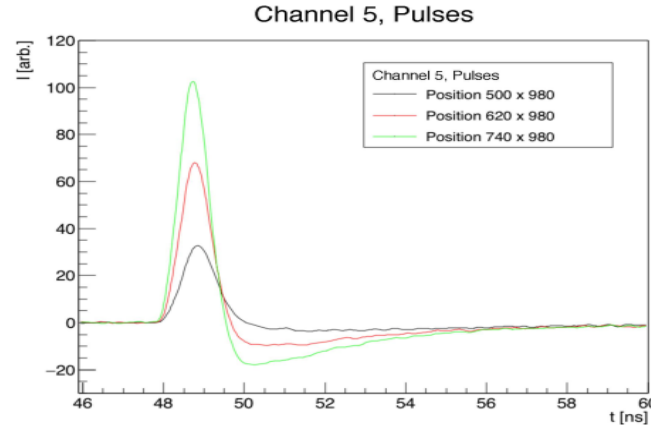
(Time resolution is inversely proportional to the pulse height.)



Pulse Shapes for Front or Back Laser Irradiated Sensor

Frontside Scan: Pulse Comparison

In Between Pad 4 and 5:



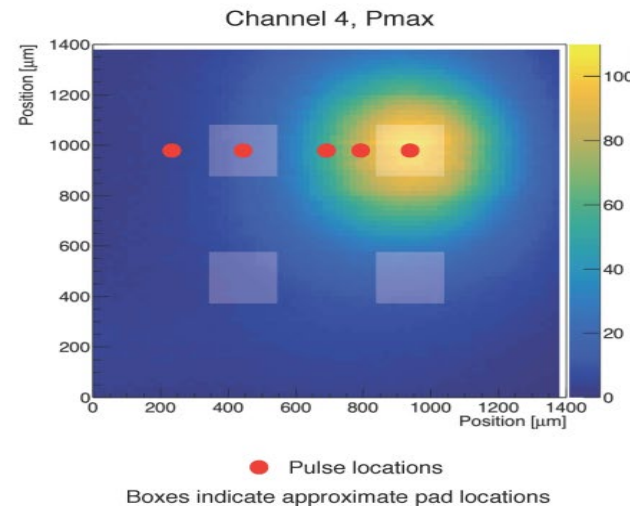
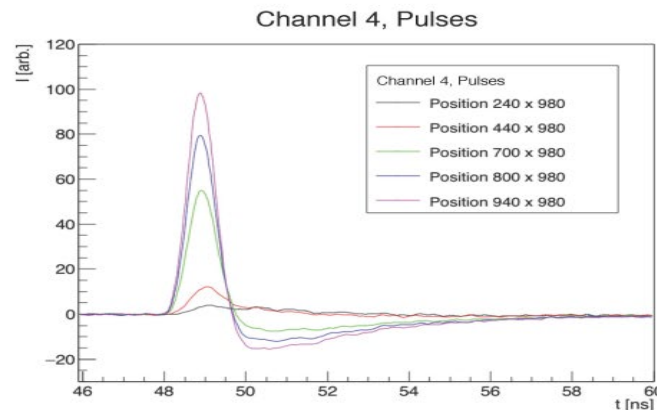
Pixel Pitch = 500 μm , Pad Size = 200 μm

Laser irradiation, locations shown by red dots in figures. Front-side, can't irradiate location of metal pad, backside can explore full detector response.

Pulses have very consistent rise and fall times. 10-90% rise-time about 530 psec. Different amplitudes basis of position interpolation.

Backside Scan: Pulse Comparison

In Between Pad 4 and 5:

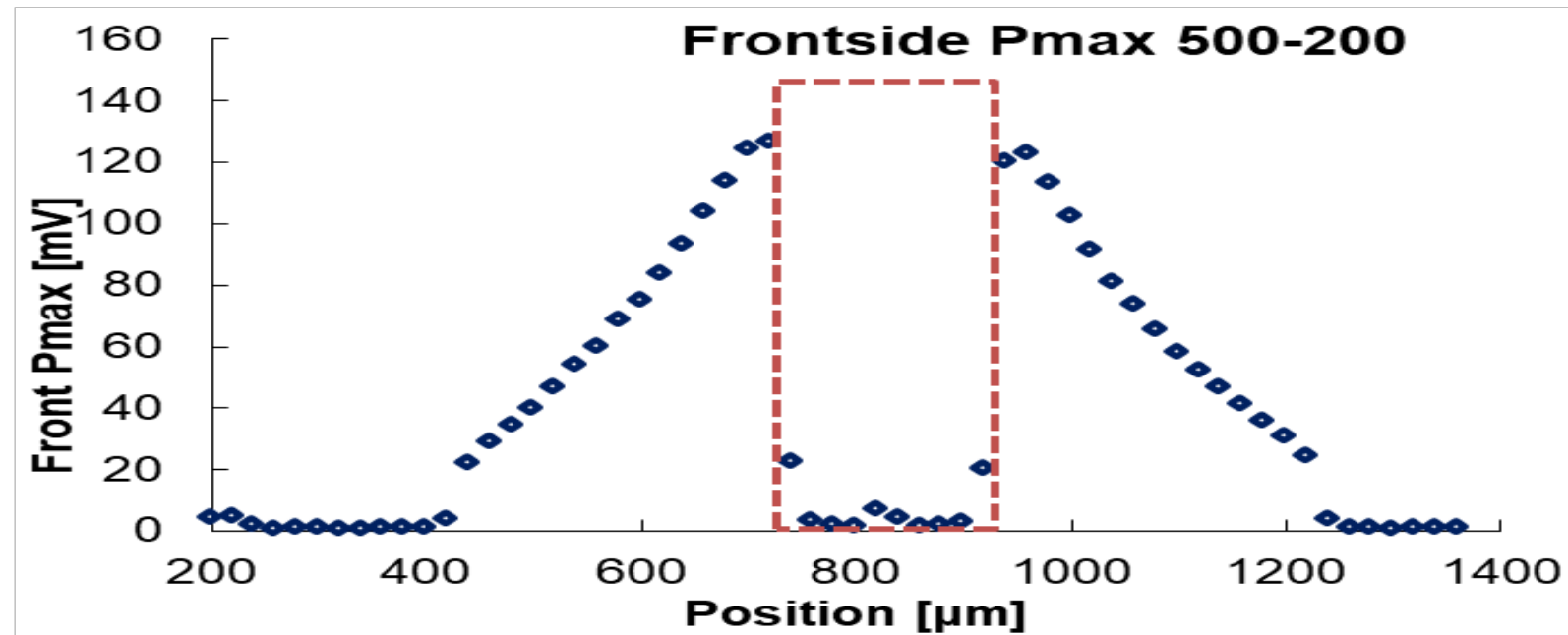


Pmax under next neighbor pad: ~ 10% of hit pad.

Pmax beyond next neighbor pad: less than 2%.

No direct capacitive pick-up between pads.

Position Measurement for 500-200



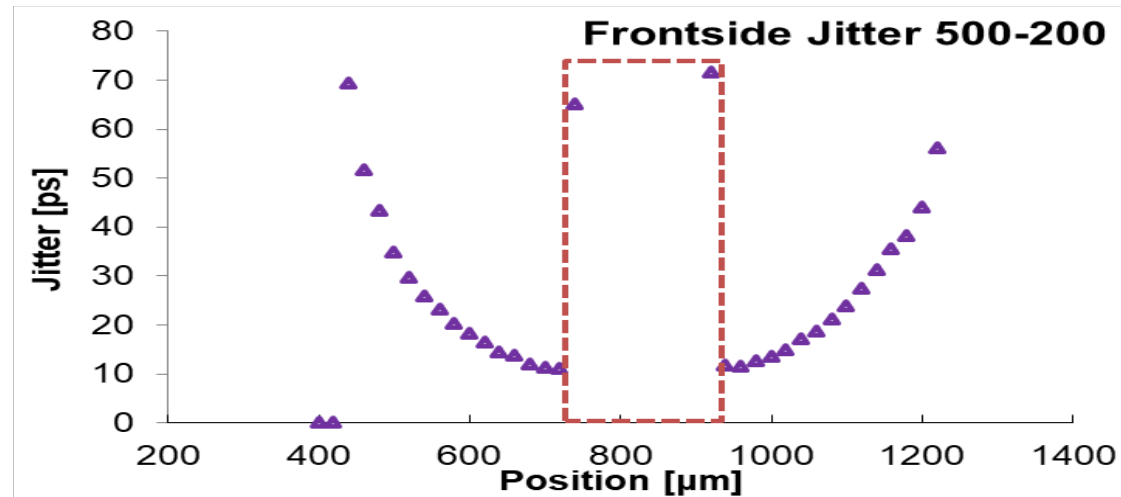
Pulse maximum decreases nearly linearly as we move away from the pad in a direction given in the previous figure. A measurement of the coordinate along the direction we are scanning, referenced to the center between the pads, is therefore approximately: $x = (P1 - P2)/(P1+P2)$ where P1 is shown above and P2 is pulse height for neighbor (not shown). $(P1 + P2)$ is nearly constant independent of location in x. From this one can calculate the expected error on x in terms of the uncorrelated variation on the pulse heights from electronics noise. The linear approximation gives for the error on x:

$$\sigma_x = [\text{Interpad Spacing} / \text{signal-to-noise ratio}] f$$

The signal-to-noise ratio is the electronics noise (assumed to be the same for each pad) divided by $(P1+P2)$ and f is a factor near 1 given by: $[0.5 / (\text{maximum value of } (P1-P2)/(P1+P2))] \sqrt{(P1^2 + P2^2)/(P1+P2)}$. The position resolution varies only a little with x.

Time Measurement for 500-200

500-200: Jitter = 11 ps near pad (note no Landau contribution for Laser). Further away use several time measurements.



We have a collection of times measured on several pads and need to combine for a best value and error estimate. Assume any systematics have been corrected and we have times t_i for the various pads (usually 3 or 4). The jitter for each (where jitter is the contribution from the electronics system, assume Landau fluctuations are in common) is then estimated to be $T_{MAX} / (P_i / \sigma_{NOISE})$. Here T_{MAX} is the 10-90% rise-time of the signal, σ_{NOISE} is the electronics noise, and P_i is the maximum pulse height. Assuming that T_{MAX} and σ_{NOISE} are in common we can then calculate that the best estimate for the time and its error are;

$$t = \sum t_i P_i^2 / \sum P_i^2 \quad \text{with} \quad \sigma_t = T_{MAX} / [\text{sqrt}(\sum P_i^2) / \sigma_{NOISE}]$$

Data above for one pad follow expectation that resolution is inversely proportional to the pulse height.

Simulation Framework:

- ❑ 2D Silvaco© Victorydevice
- ❑ Impact Ionization = Grant (has a low-field, an intermediate-field, and a high-field region, there is no temperature dependence)
- ❑ Mobility Models:
 - Conmob (the concentration dependent mobility model)
 - Fldmob (the lateral electric field-dependent mobility model)
- ❑ Recombination model = Shockley – Read –Hall Recombination model (SRH)
Method = Newton (Nonlinear solutions are obtained using the Newton method)
- ❑ Charge deposition (MIP) using singleeventupset method (80 e/h pairs per micron)
- ❑ X-mesh size = 5 μm
- ❑ Y-mesh size = 1 μm

Areas of Past/Current Work Relevant to the EIC

- Over the past couple years, **SCIPP** has directed some of its LGAD effort in directions designed to **generally or directly support EIC detector development**
 - Sensor testing/simulation and ASIC production/testing
- SCIPP is currently involved in:
 - US-Japan grant for the development of AC-LGADs (funds for production of AC-LGADs at BNL and HPK, supports testing at FNAL test beam facility) mostly aimed at the EIC
 - eRD112 for ASIC and sensor development
- Interested in eRD109 for ASIC development in the future