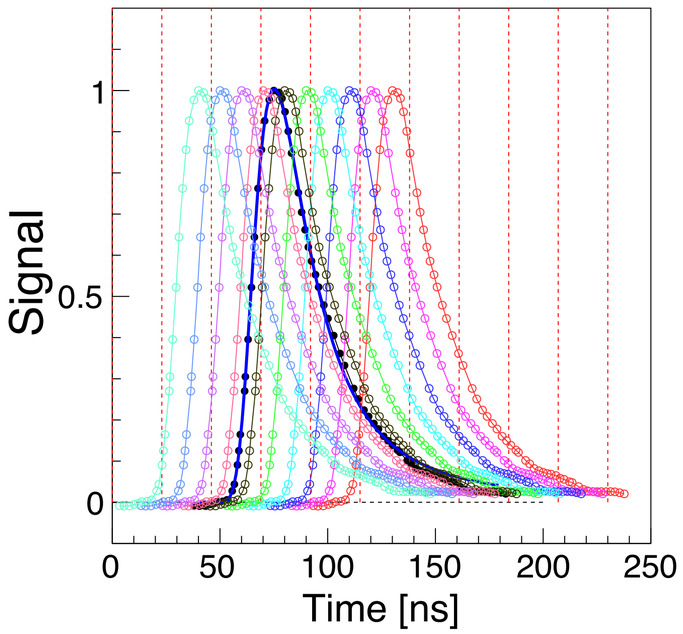
R&D on the HGCROC

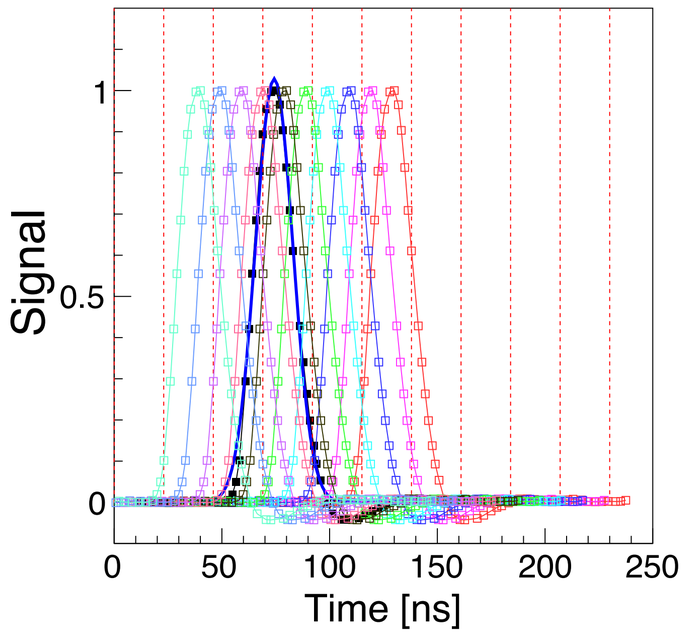
Norbert Novitzky

Signal shape

Default



Physics



Two signal shapes are identified from the HGCROC:

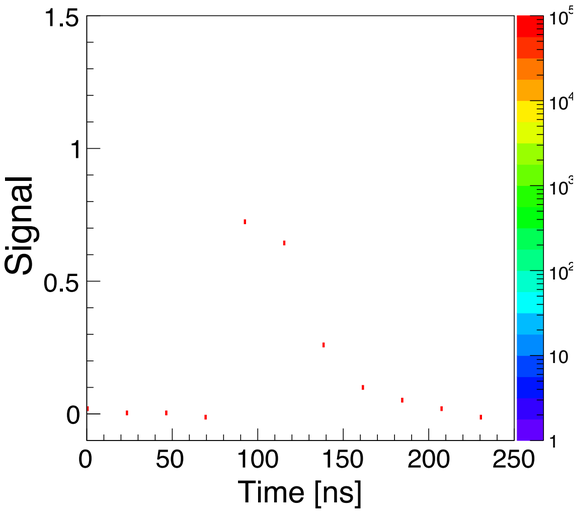
- The default one has a longer tail, while the physics one is constrained to the 25ns window:
  - My guess would be to reduce the pile-ups for the CMS detector
  - We could just stick to the default shape and save multiple BX (25ns samples) from the pulse

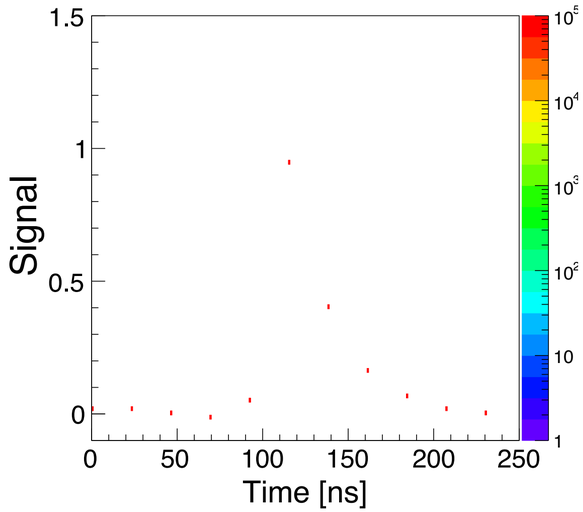
Each color represent a 10ns shift of the same signal - 100 MHz clock cycle:
Each red dashed line represent one 25ns clock cycle of the clock

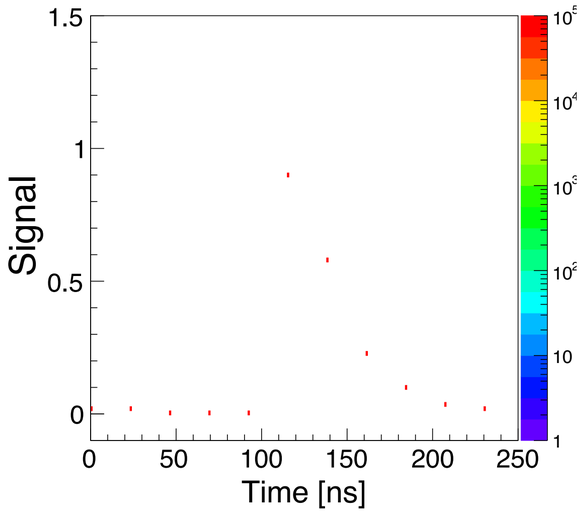
Strategy is to collect 3-4 samples of the default shape

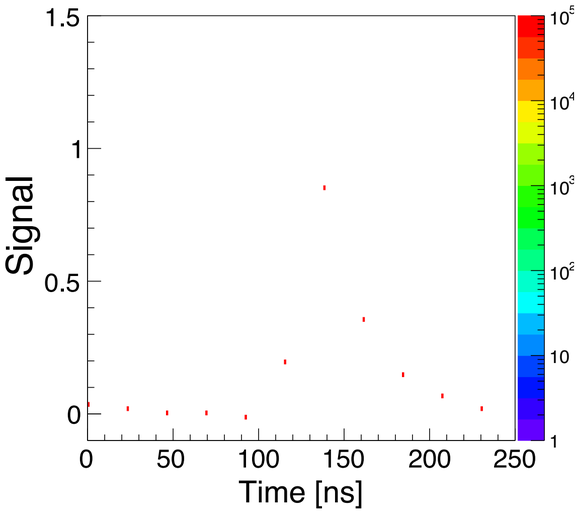
How it would look like - Default

No noise

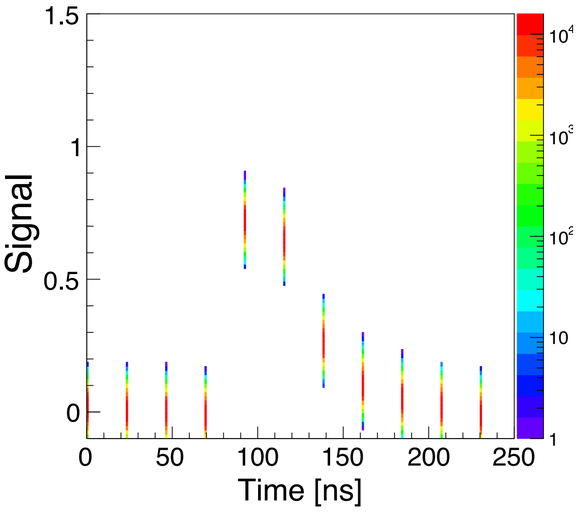


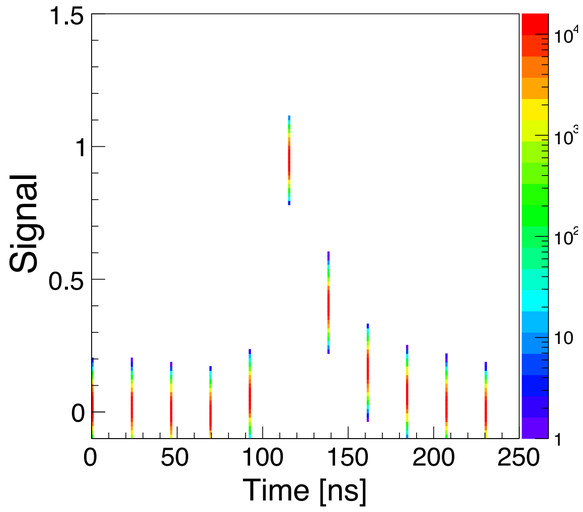


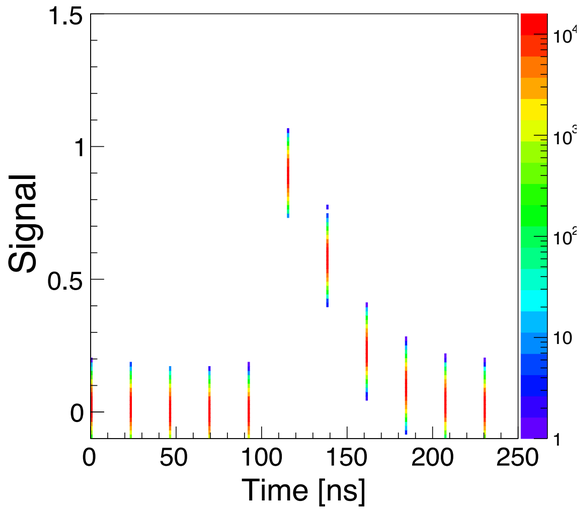


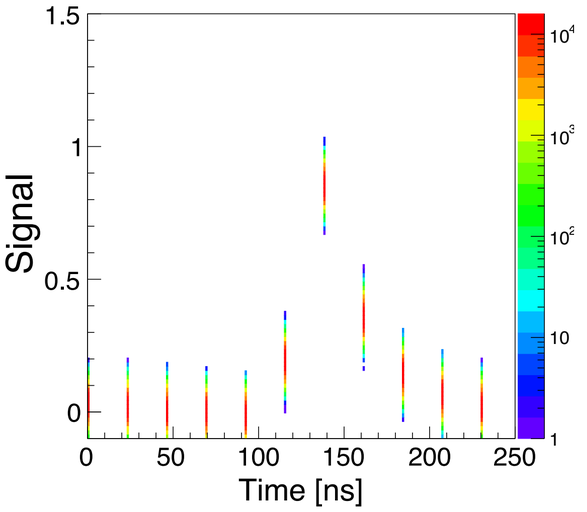


Added random noise (driven from MIP measurements)



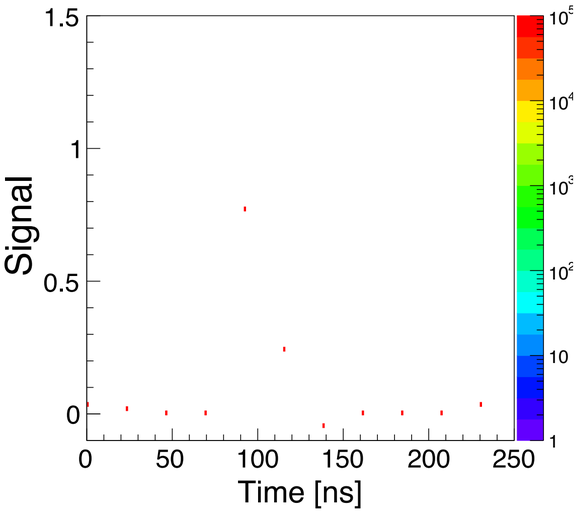


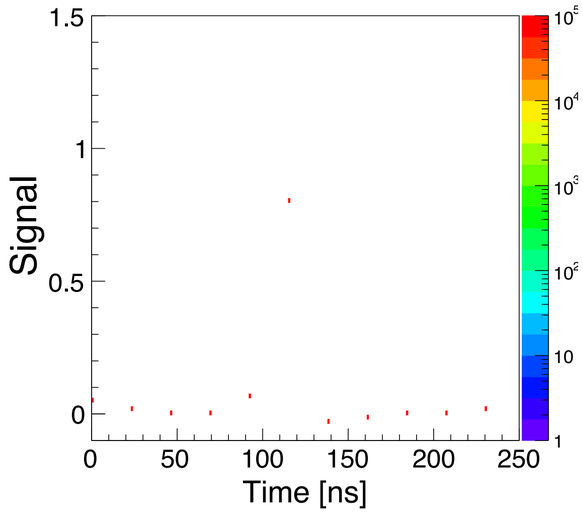


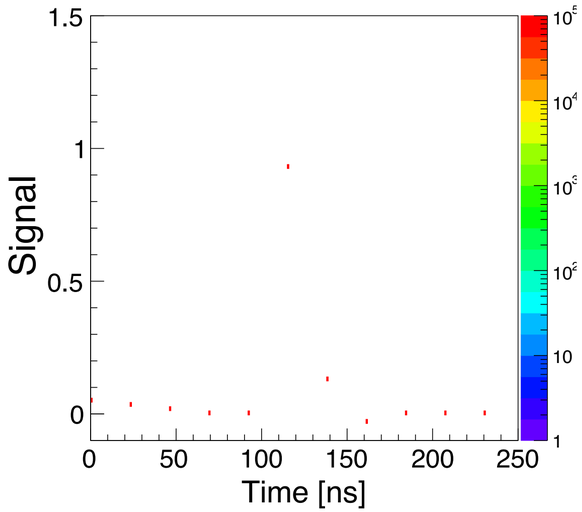


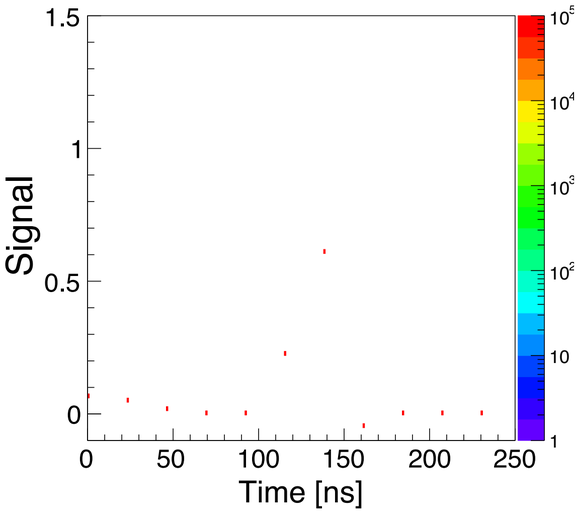
How it would look like - Physics

No noise

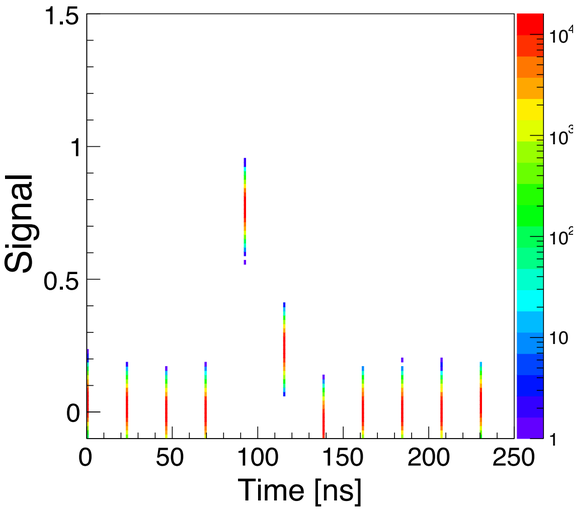


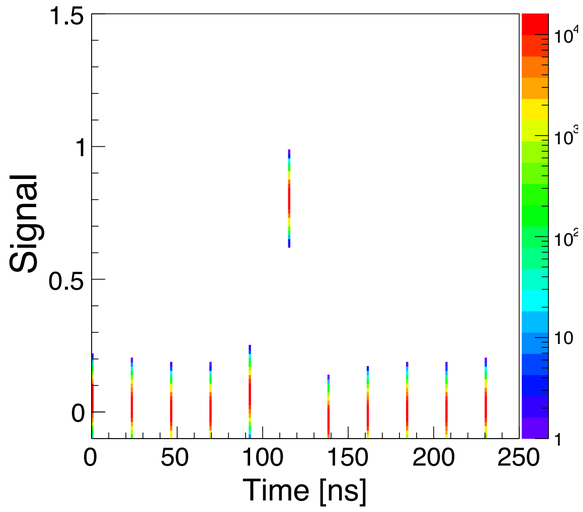


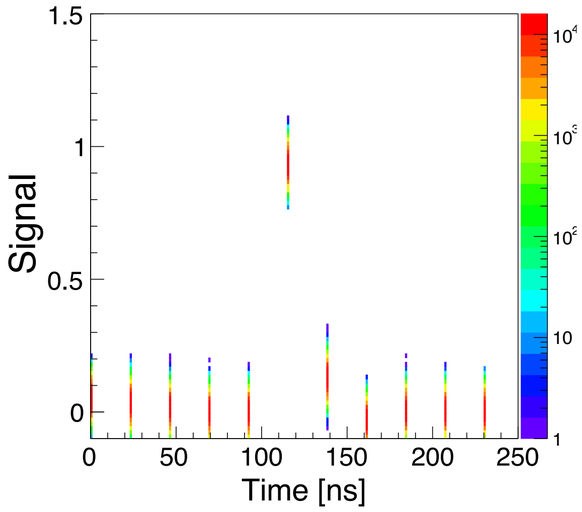


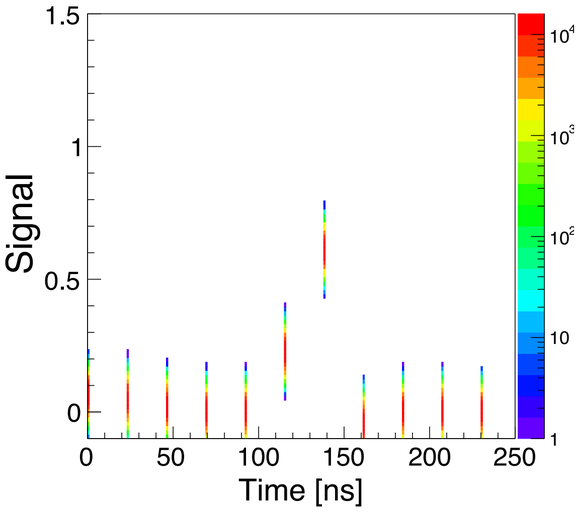


Added random noise (driven from MIP measurements)

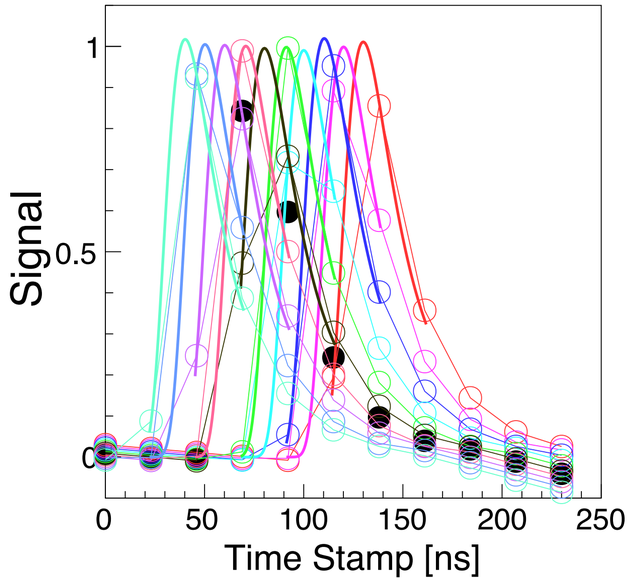


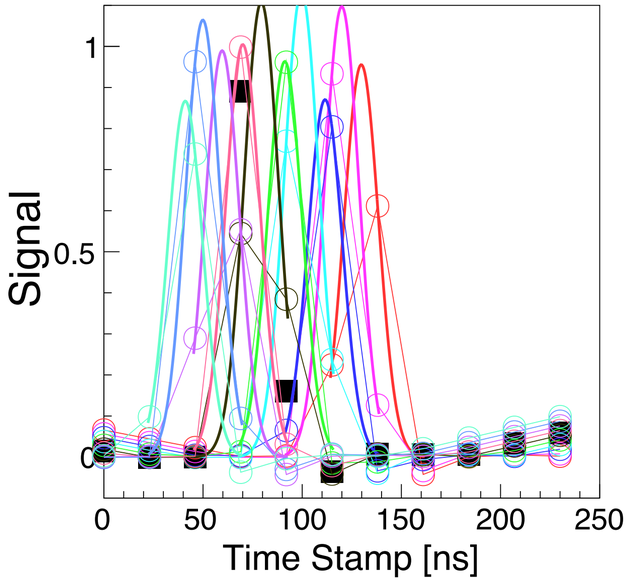






Fitting the signal shape



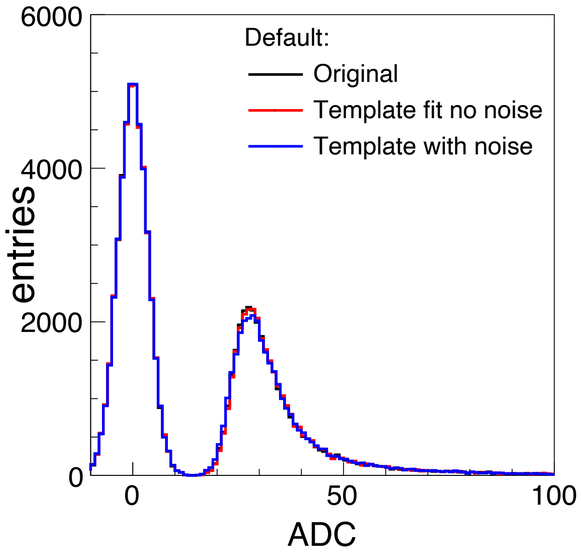


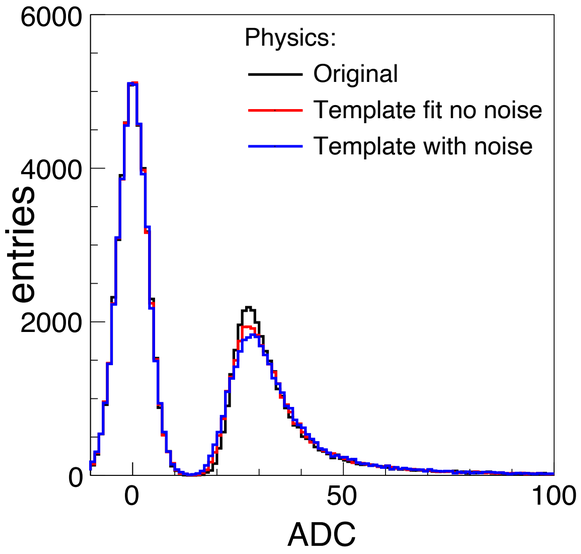
Extracting the signal:

- Identify the maximum of the signal
- Use -25 ns and +25 ns samples
- Fit the signal shape:
  - Landau for the default
  - Gaus for the physics

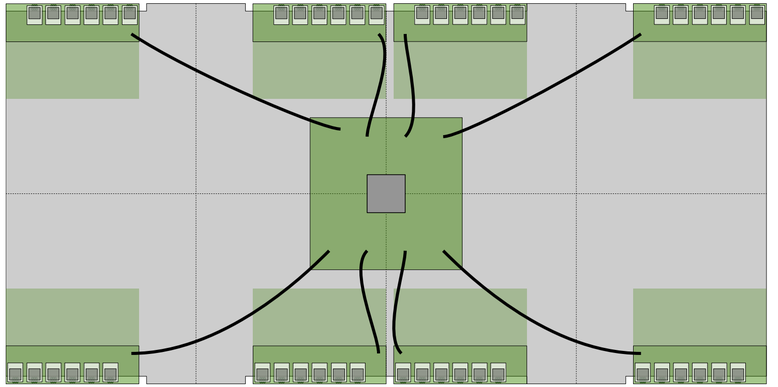
Realistic shape of the MIP signal in Silicon pad (not SiPM):

- Data was taken in PS 2022
- The MIP signal is mpv 27 ADC
- Realistic noise (pedestal added)
- The template fit uses 3 data samples with and without added noise on each point

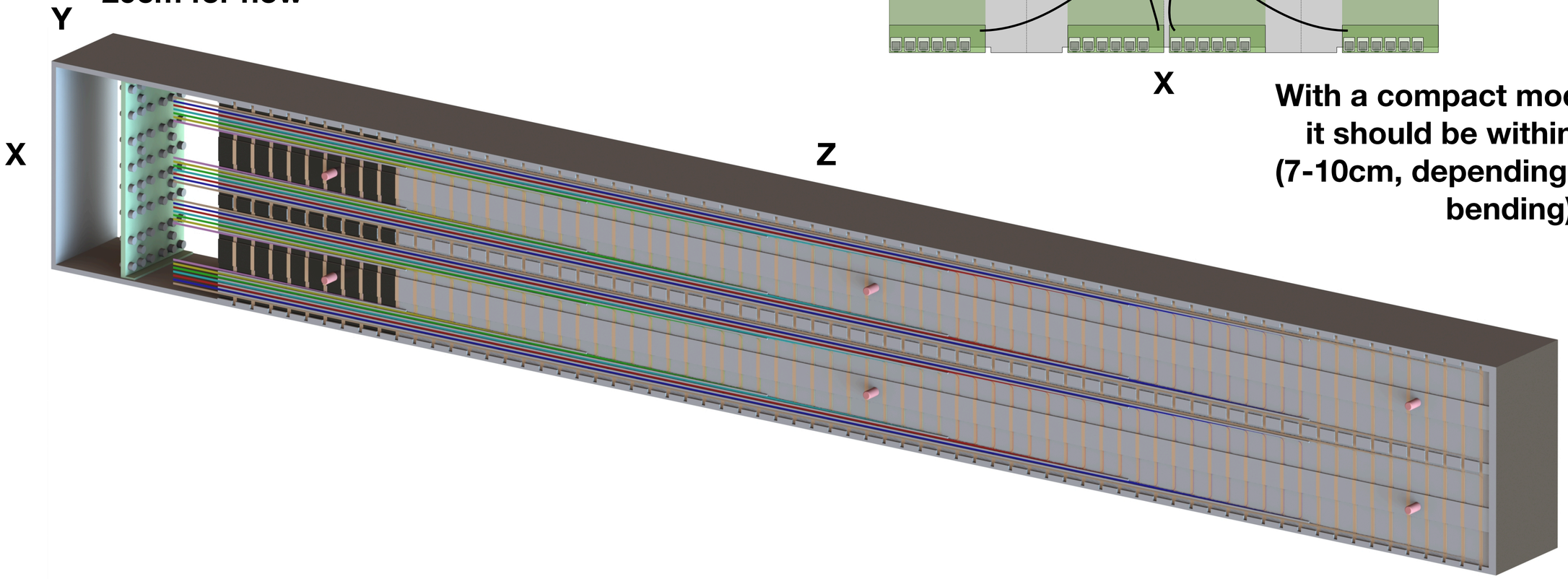




Inside the calorimeter

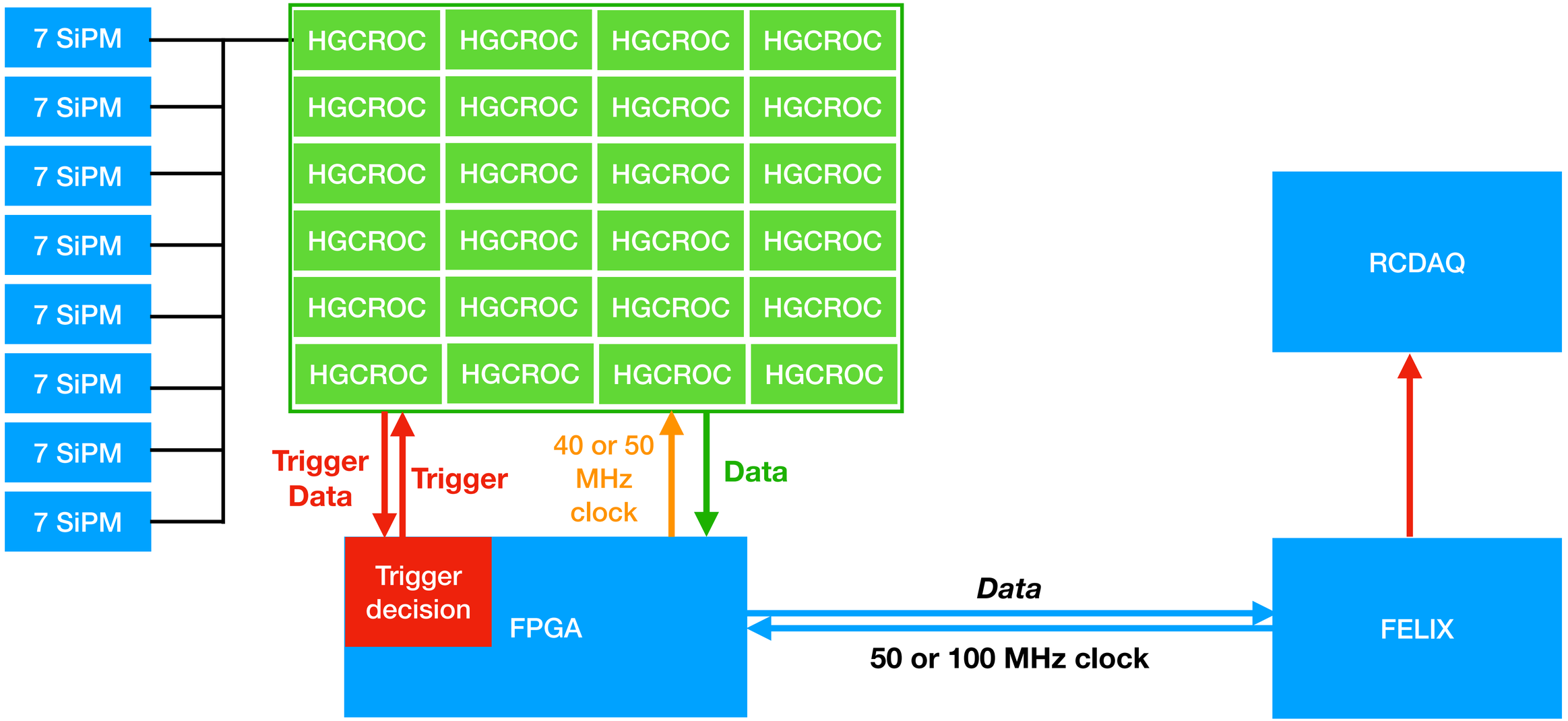


20cm for now

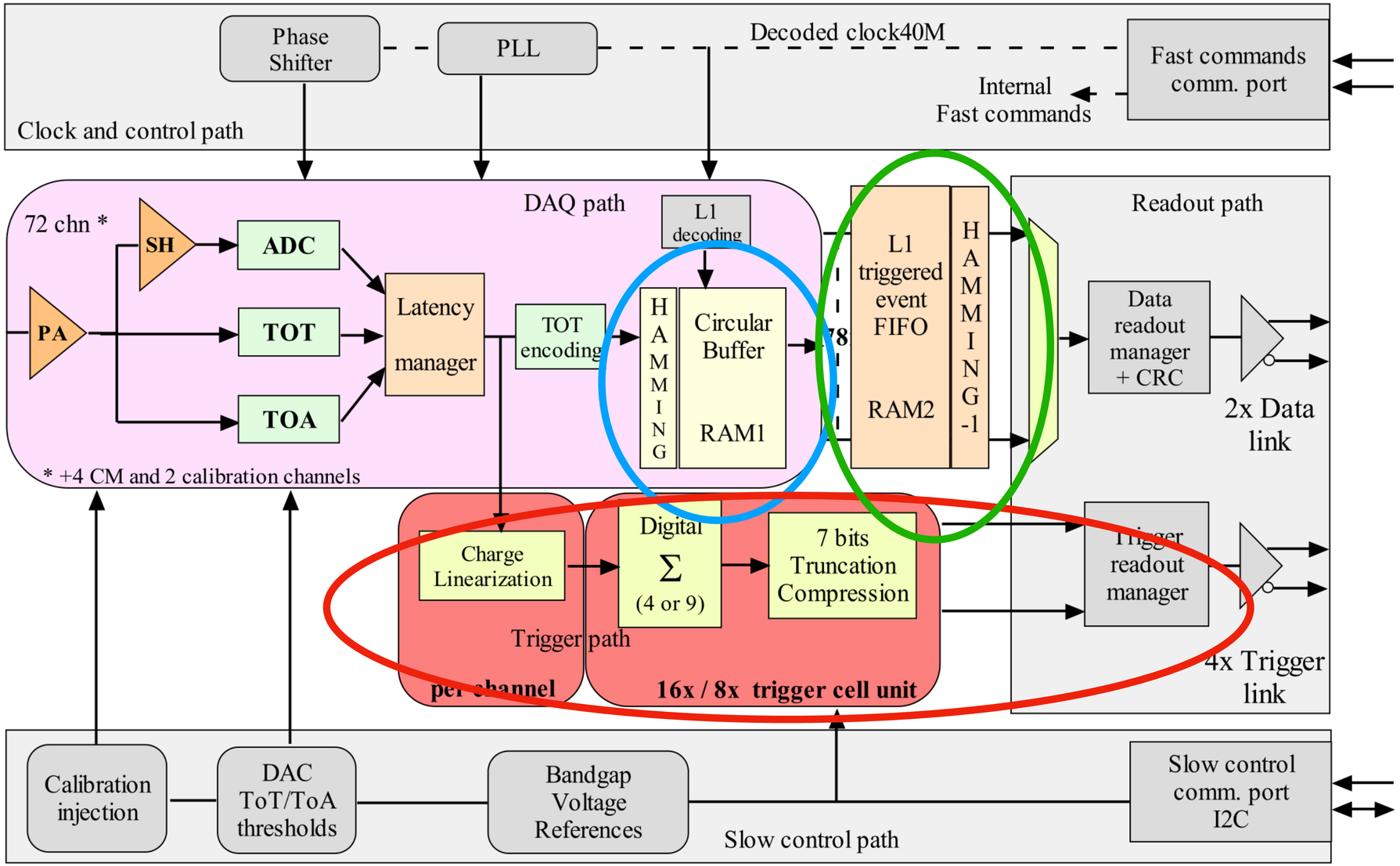


With a compact modular design it should be within few cm's (7-10cm, depending on the fiber bending)

Proposed hierarchy



HGCROC overview



Trigger data:
- 4 or 9 channels are summed up
- Sent as a 64-bit word out on 4 trigger links

RAM1:
- Circular buffer of 512 samples
- 512 x 25 ns = 12.5 µs total
- L1 needed to shift to the RAM2
  - We can shift 3-4 samples

RAM2:
- Circular buffer of 32 samples
- Space for 8-10 events
- Max readout speed 960 kHz

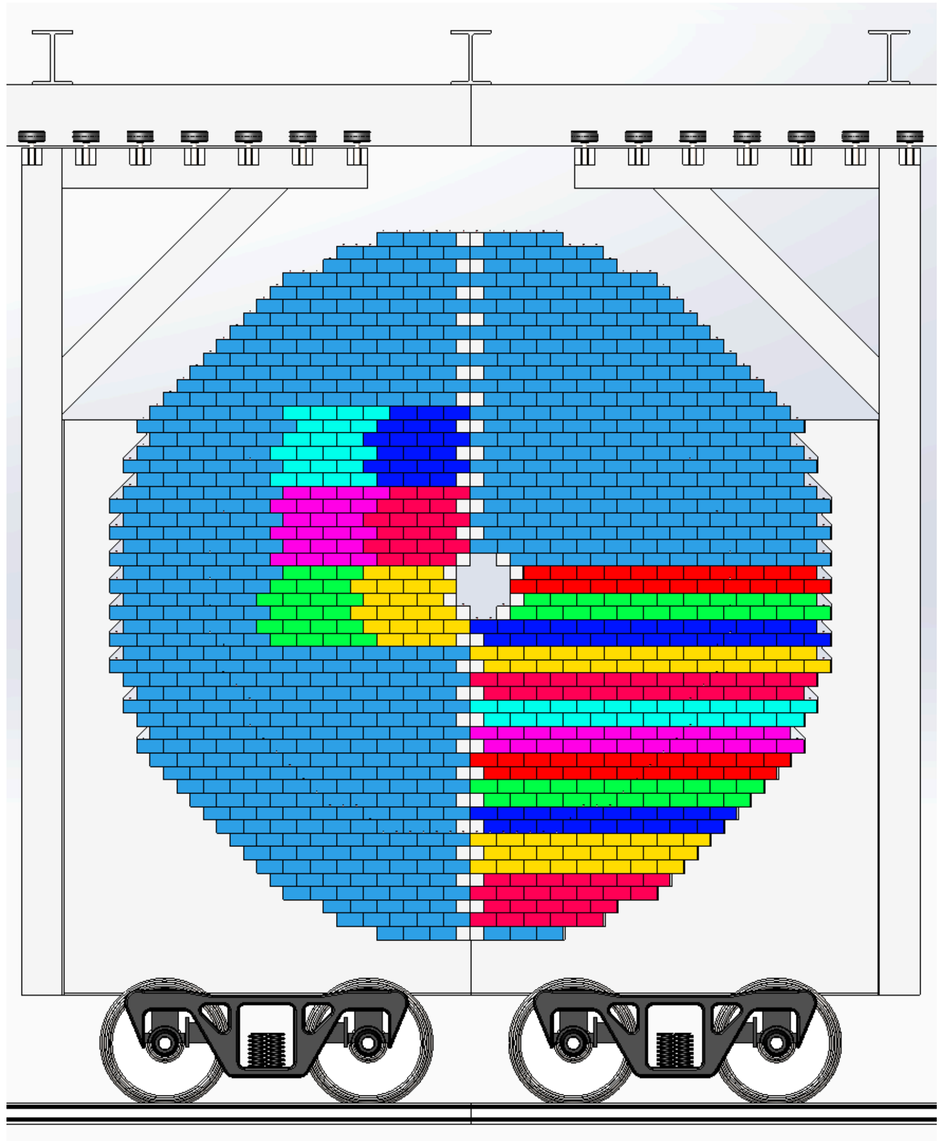
Expected hit rate is 50kHz in forward region, with 4 samples it would be 200 kHz readout speed (1/4 of the capability)

Possible placements of the FPGA board

Option A:

1 meter away from the beam pipe

Spider web design towards the FPGA



Option B:

On the side of the calorimeters

Snake design of the cables