ROC DF18 Empty Port Termination

RIKEN/RBRC

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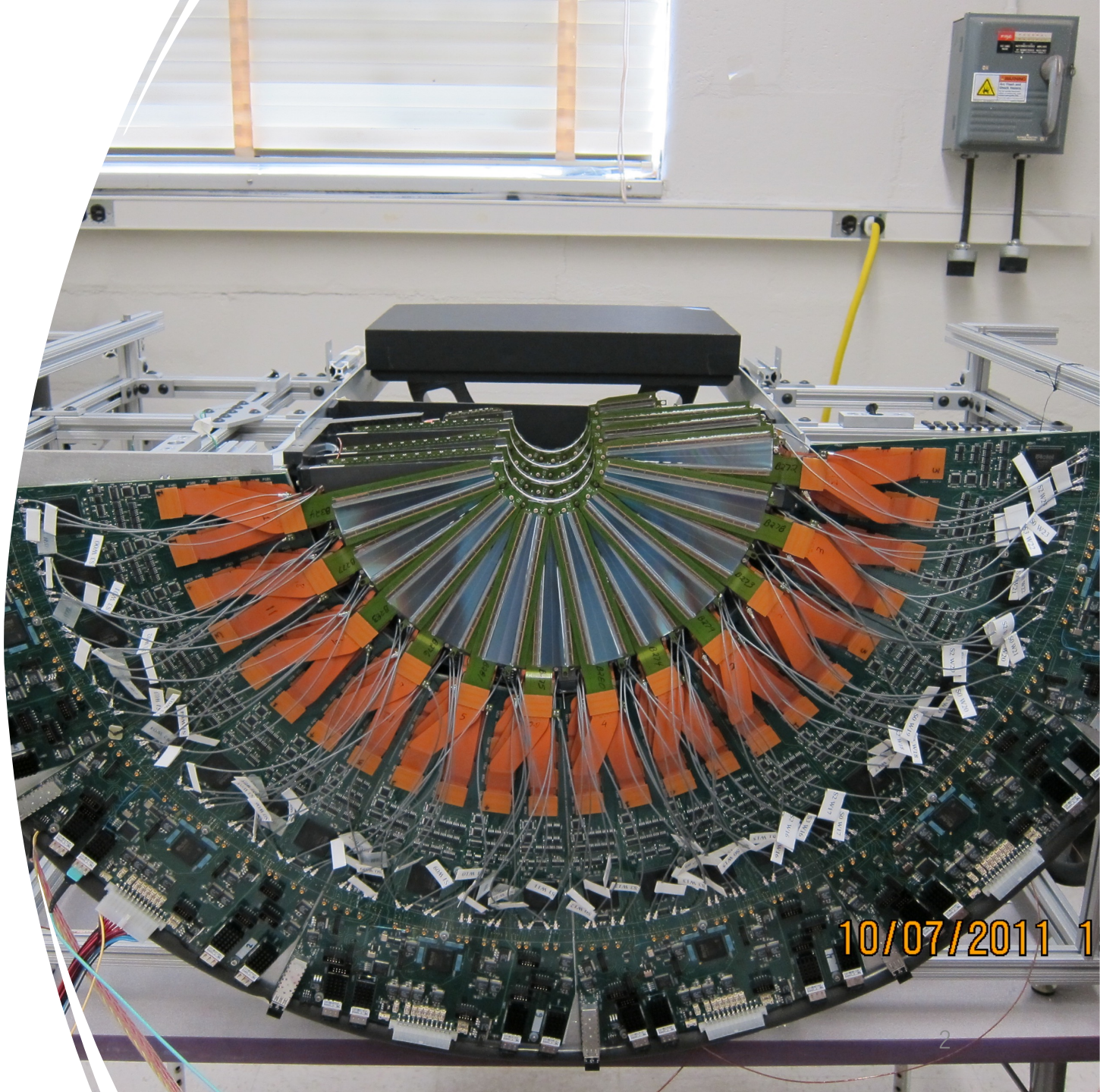
FVTX ROC Ports Configuration

- All ROC DF18 ports were occupied in FVTX operation.
- Thus there was no even a single ports remain open during their operation.



What's Wrong?

Fake hits?

- Many of you experienced fake hits appear on the terminal in the test bench DAQ.
- These fake hits belong to non-existing module, i.e. decoded as hit from empty ports.

How come hits are generated from empty ports?

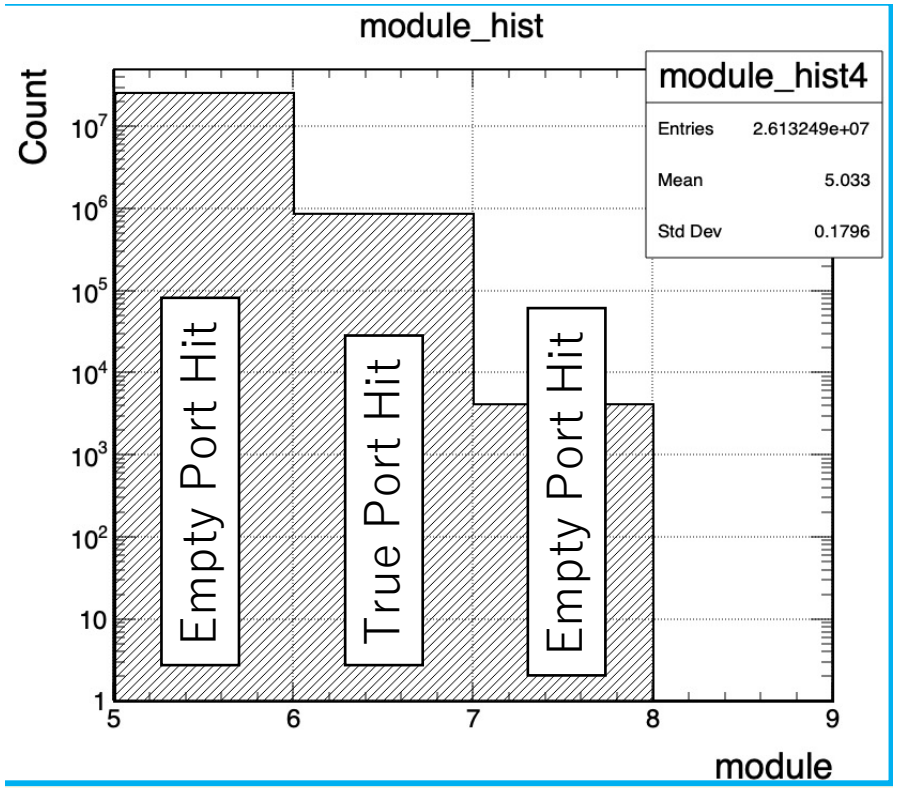
- The current hypothesis is these fake hits are generated at the empty port due to the reflection of digital signal.

Is this fatal for our data quality?

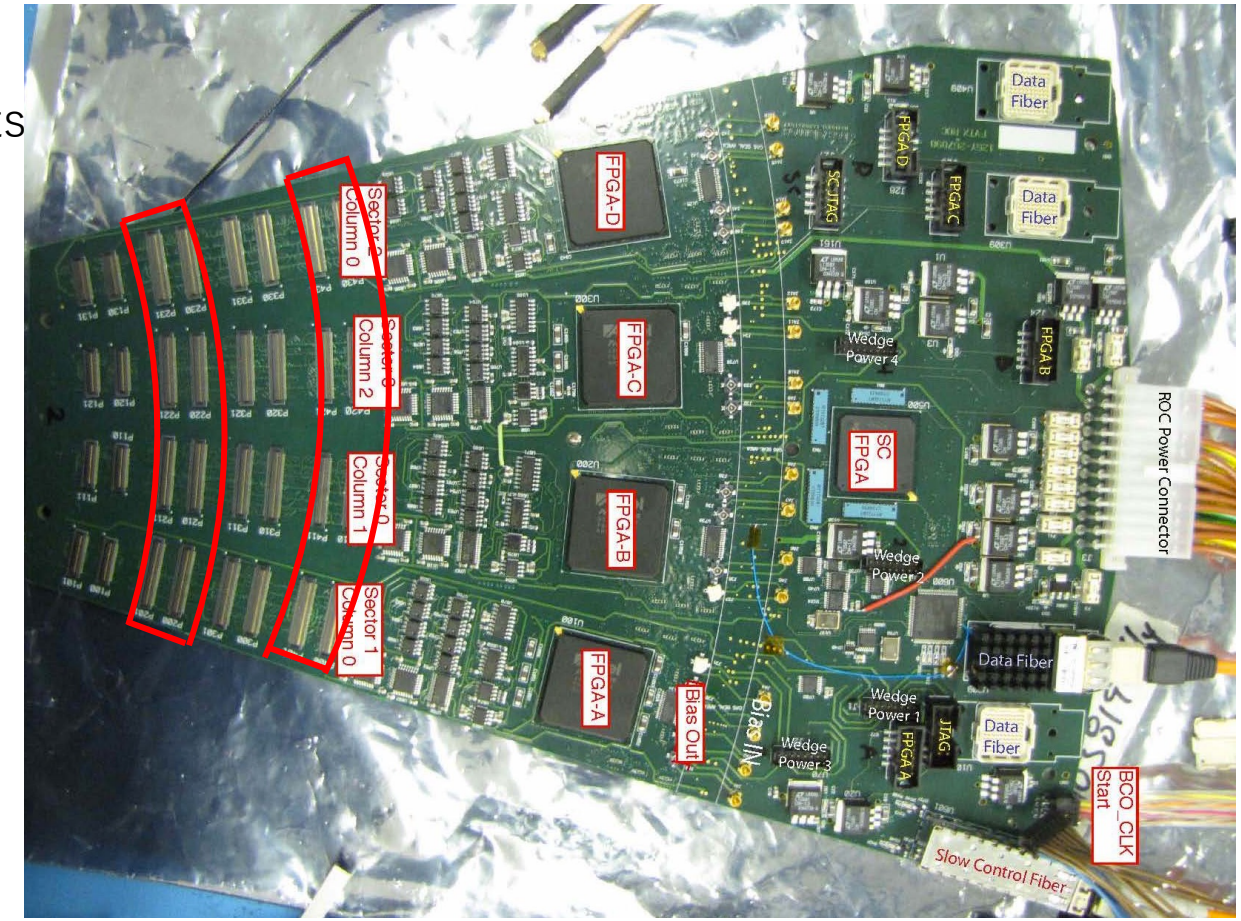
- Probably not. These data will never be processed in the analysis.
- Data size will be the concern.

Fake Hits from Empty Ports

- Only station 1 and 3 will be used.
- Half of DF18 ports are to be remain open.
- Fake hits are observed from the empty ports



From Hikaru's Study on Feb. 24, 2022

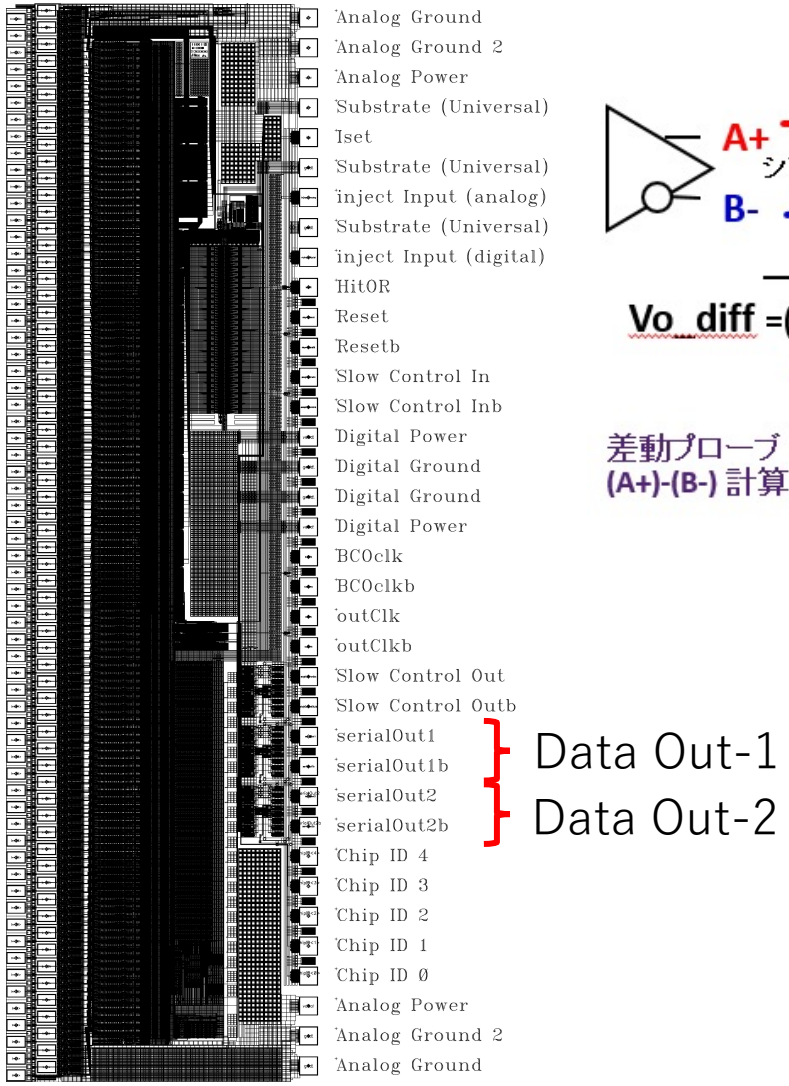


Software or Hardware Solution?

- Mask particular fiber @ FELIX
- Mask particular leg of FPGA @ ROC

It is possible to mask empty ports at ROC or FELIX stage, though we haven't tested yet and we don't know when we can do it. 2nd software solution may require data FPGA upgrade at ROC. The plan is to pursue both solutions in parallel.

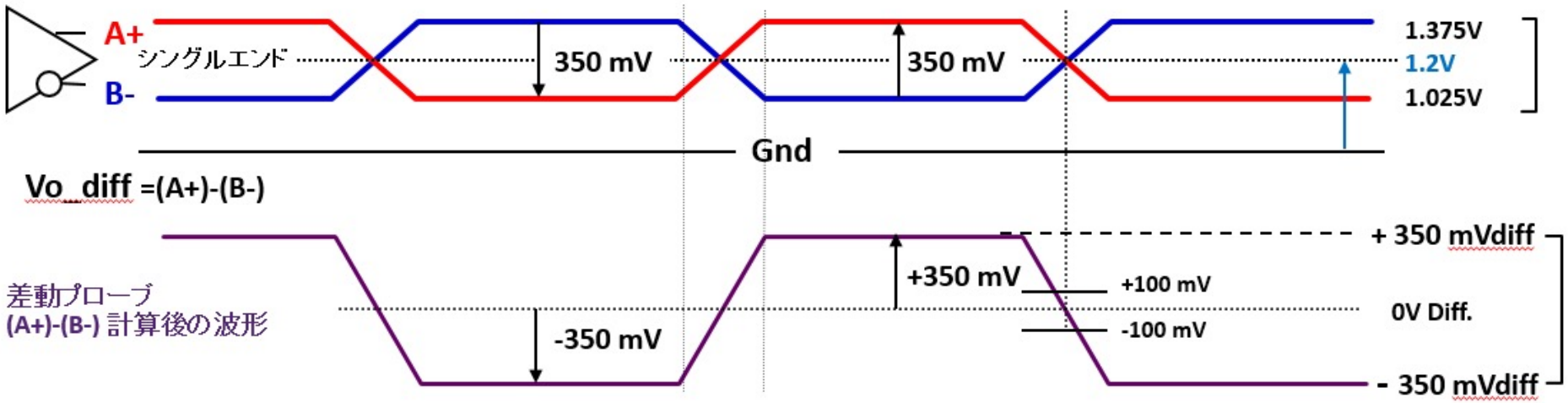
Low Voltage Differential Signaling (LVDS)



Data Out-1

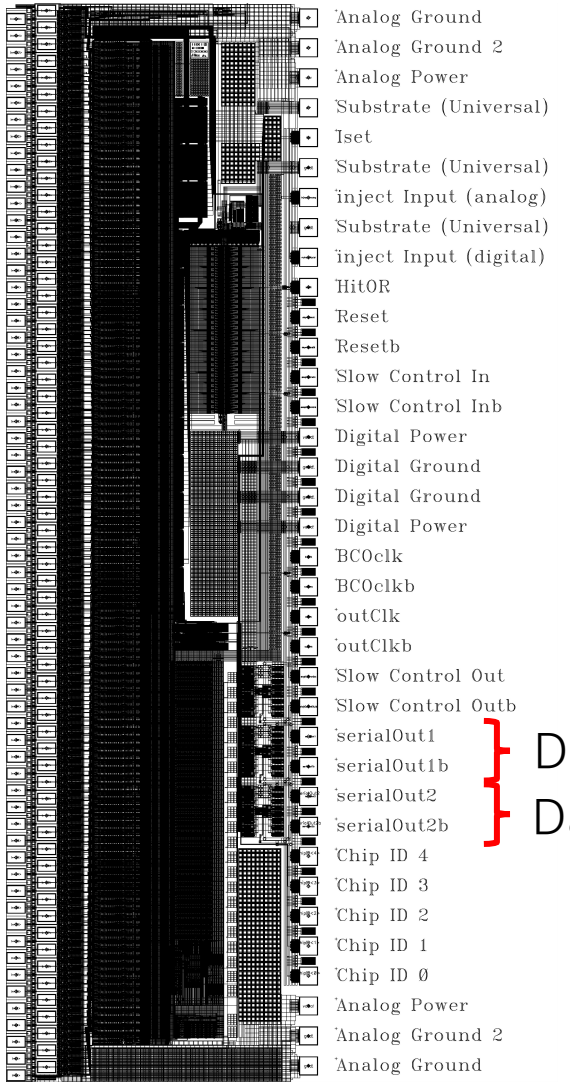
Data Out-2

FPHX



- Signals are transmitted in pair of signal lines with opposite phase.
- They are taken differential at the receiver

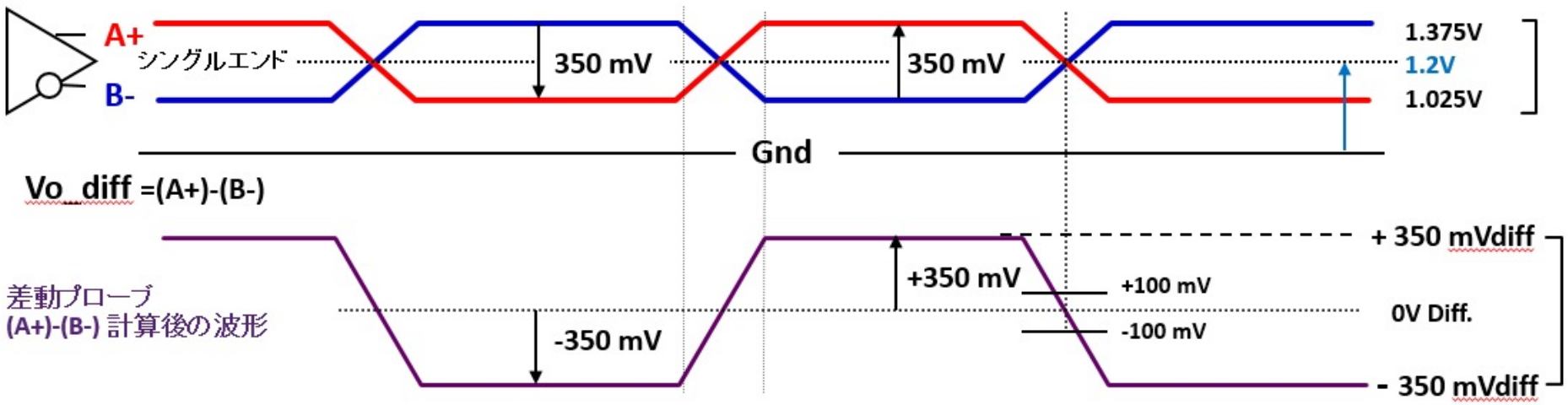
Low Voltage Differential Signaling (LVDS)

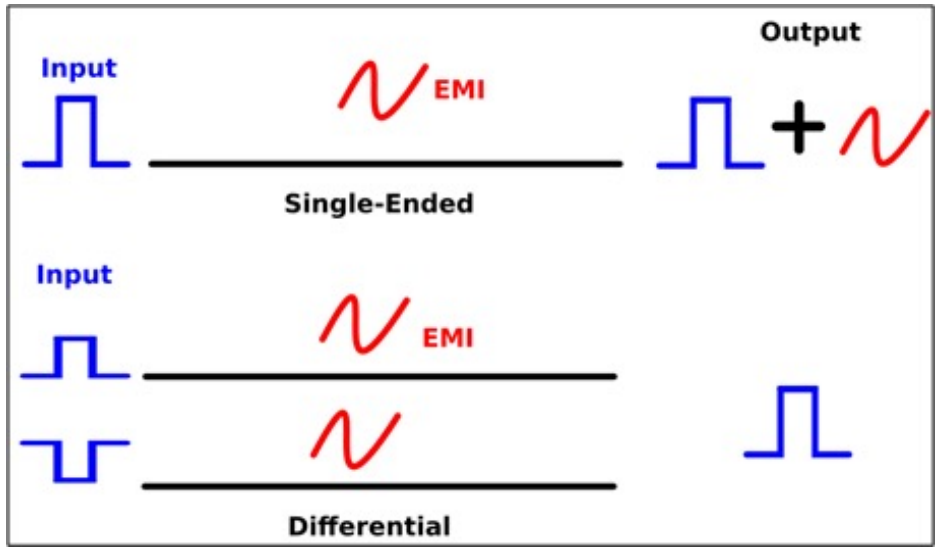


FPHX

Data Out-1

Data Out-2

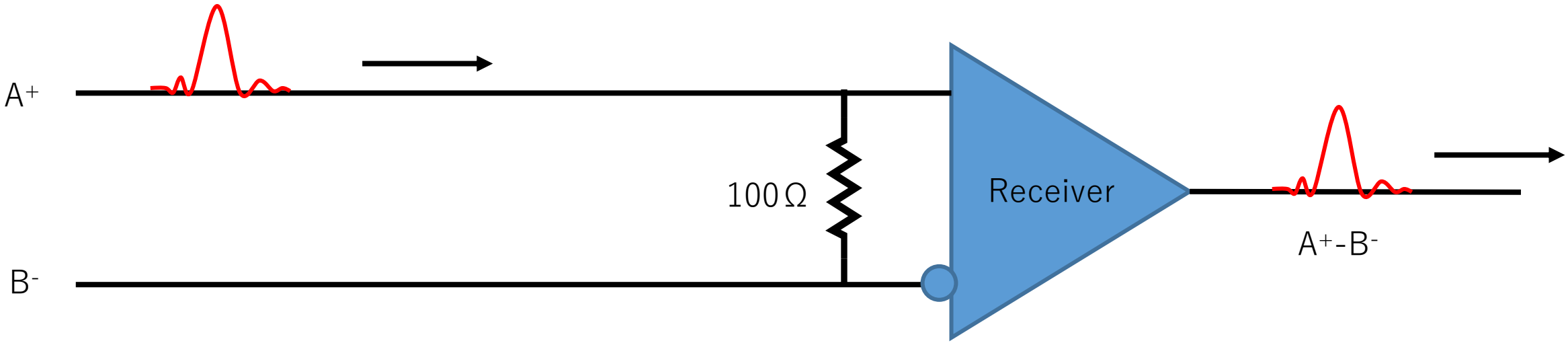




Signal is suffered from noise

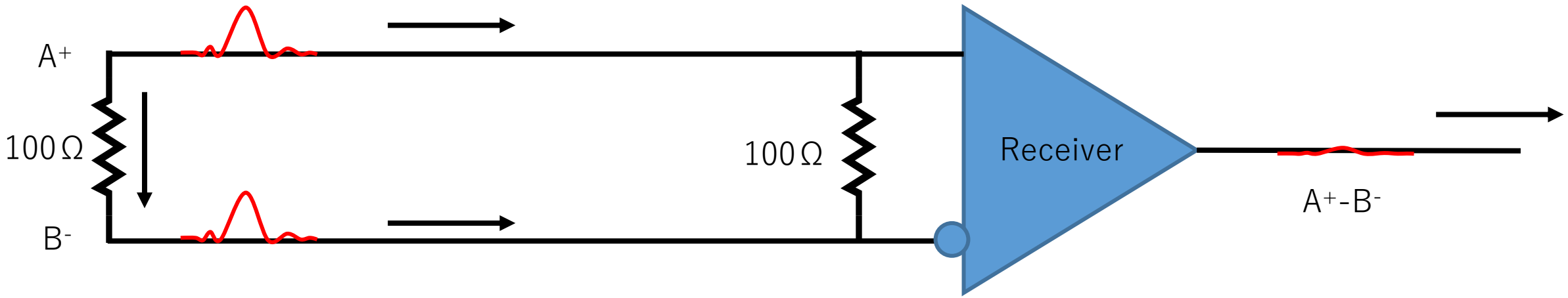
Common mode noise can be canceled at the receiver

Empty Port = Open End Circuit



Somehow one of the LVDS pair lines picks up unique noise. The receiver process this noise as it is to the down stream.

Solution : Termination



The simplest solution is to terminate the open end by 100Ω resistance and let the noise to be common mode between LVDS pairs. This way, the noise will be canceled at the receiver.

DF18 Channel Map

Table made by Rkkyo Undergrads

Station-0

ROC Side

RECEPTACLE (TOP)

J1 (out side)				J2 (in side)			
#	name (net)	#	name (net)	#	name (net)	#	name (net)
1	1_CHIP1_OUT 1P	60	1_CHIP1_OUT 0P	1	OUT_CLK1n		BCO_CLK1p
2	1_CHIP1_OUT 1N	59	1_CHIP1_OUT 0N	2	OUT_CLK1p		BCO_CLK1n
3	1_CHIP2_OUT 1P	58	1_CHIP2_OUT 0P	3	DGND		RESET1p
4	1_CHIP2_OUT 1N	57	1_CHIP2_OUT 0N	4	DGND		RESET1n
5	1_CHIP3_OUT 1P	56	1_CHIP3_OUT 0P	5	SC_IN1n		SC_OUT1p
6	1_CHIP3_OUT 1N	55	1_CHIP3_OUT 0N	6	SC_IN1p		SC_OUT1n
7	1_CHIP4_OUT 1P	54	1_CHIP4_OUT 0P	7	DGND		DGND
8	1_CHIP4_OUT 1N	53	1_CHIP4_OUT 0N	8	DGND		DGND
9	CAL_INJECT1	52	DGND	9	AGND		DGND
10	AGND	51	1_CHIP5_OUT 0N	10	AGND		DGND
11	1_CHIP5_OUT 1P	50	1_CHIP5_OUT 0P	11	AGND		+2.5VD
12	1_CHIP5_OUT 1N	49	DGND	12	AGND		+2.5VD
13	AGND	48	DGND	13	+2.5VA		+2.5VD
14	+2.5VA	47	+2.5VD	14	+2.5VA		+2.5VD
15	+2.5VA	46	+2.5VD	15	+2.5VA		+2.5VD
16	+2.5VA	45	+2.5VD	16	+2.5VA		+2.5VD
17	+2.5VA	44	+2.5VD	17	+2.5VA		+2.5VD
18	AGND	43	DGND	18	+2.5VA		+2.5VD
19	0_CHIP5_OUT 0P	42	DGND	19	AGND		+2.5VD
20	0_CHIP5_OUT 0N	41	0_CHIP5_OUT 1N	20	AGND		+2.5VD
21	AGND	40	0_CHIP5_OUT 1P	21	AGND		DGND
22	0_CAL_INJECT0	39	DGND	22	AGND		DGND
23	0_CHIP4_OUT 0N	38	0_CHIP4_OUT 1N	23	DGND		DGND
24	0_CHIP4_OUT 0P	37	0_CHIP4_OUT 1P	24	DGND		DGND
25	0_CHIP3_OUT 0N	36	0_CHIP3_OUT 1N	25	SC_IN0n		SC_OUT0p
26	0_CHIP3_OUT 0P	35	0_CHIP3_OUT 1P	26	SC_IN0p		SC_OUT0n
27	0_CHIP2_OUT 0N	34	0_CHIP2_OUT 1N	27	DGND		RESET0p
28	0_CHIP2_OUT 0P	33	0_CHIP2_OUT 1P	28	DGND		RESET0n
29	0_CHIP1_OUT 0N	32	0_CHIP1_OUT 1P	29	OUT_CLK0n	32	BCO_CLK0p
30	0_CHIP1_OUT 0P	31	0_CHIP1_OUT 1N	30	OUT_CLK0p	31	BCO_CLK0n

Only LDVD Data Pairs are to be terminated.

Station-1,2,3

ROC Side

RECEPTACLE (TOP)

J1 (out side)				J2 (in side)			
#	name (net)	#	name (net)	#	name (net)	#	name (net)
1	AGND	100	DGND	1	AGND	100	DGND
2	1_CHIP1_OUT 1P	99	1_CHIP1_OUT 0P	2	SC_IN1p	99	RESET1p
3	1_CHIP1_OUT 1N	98	1_CHIP1_OUT 0N	3	SC_IN1n	98	RESET1n
4	1_CHIP2_OUT 1P	97	1_CHIP2_OUT 0P	4	DGND	97	BCO_CLK1p
5	1_CHIP2_OUT 1N	96	1_CHIP2_OUT 0N	5	DGND	96	BCO_CLK1n
6	1_CHIP3_OUT 1P	95	1_CHIP3_OUT 0P	6	OUT_CLK1p	95	SC_OUT1p
7	1_CHIP3_OUT 1N	94	1_CHIP3_OUT 0N	7	OUT_CLK1n	94	SC_OUT1n
8	1_CHIP4_OUT 1P	93	1_CHIP4_OUT 0P	8	DGND	93	DGND
9	1_CHIP4_OUT 1N	92	1_CHIP4_OUT 0N	9	DGND	92	DGND
10	CAL_INJECT1	91	DGND	10	1_CHIP6_OUT 1P	91	1_CHIP6_OUT 0P
11	AGND	90	DGND	11	1_CHIP6_OUT 1N	90	1_CHIP6_OUT 0N
12	1_CHIP5_OUT 1P	89	1_CHIP5_OUT 0P	12	1_CHIP8_OUT 1P	89	1_CHIP8_OUT 0P
13	1_CHIP5_OUT 1N	88	1_CHIP5_OUT 0N	13	1_CHIP8_OUT 1N	88	1_CHIP8_OUT 0N
14	1_CHIP7_OUT 1P	87	1_CHIP7_OUT 0P	14	1_CHIP10_OUT 1P	87	1_CHIP10_OUT 0P
15	1_CHIP7_OUT 1N	86	1_CHIP7_OUT 0N	15	1_CHIP10_OUT 1N	86	1_CHIP10_OUT 0N
16	1_CHIP9_OUT 1P	85	1_CHIP9_OUT 0P	16	1_CHIP12_OUT 1P	85	1_CHIP12_OUT 0P
17	1_CHIP9_OUT 1N	84	1_CHIP9_OUT 0N	17	1_CHIP12_OUT 1N	84	1_CHIP12_OUT 0N
18	1_CHIP11_OUT 1P	83	1_CHIP11_OUT 0P	18	AGND	83	DGND
19	1_CHIP11_OUT 1N	82	1_CHIP11_OUT 0N	19	AGND	82	DGND
20	1_CHIP13_OUT 1P	81	1_CHIP13_OUT 0P	20	AGND	81	DGND
21	1_CHIP13_OUT 1N	80	1_CHIP13_OUT 0N	21	AGND	80	+2.5VD
22	AGND	79	DGND	22	AGND	79	+2.5VD
23	AGND	78	DGND	23	+2.5VA	78	+2.5VD
24	+2.5VA	77	+2.5VD	24	+2.5VA	77	+2.5VD
25	+2.5VA	76	+2.5VD	25	+2.5VA	76	+2.5VD
26	+2.5VA	75	+2.5VD	26	+2.5VA	75	+2.5VD
27	+2.5VA	74	+2.5VD	27	+2.5VA	74	+2.5VD
28	AGND	73	DGND	28	+2.5VA	73	+2.5VD
29	AGND	72	DGND	29	AGND	72	+2.5VD
30	0_CHIP13_OUT 0N	71	0_CHIP13_OUT 1N	30	AGND	71	+2.5VD
31	0_CHIP13_OUT 0P	70	0_CHIP13_OUT 0P	31	AGND	70	DGND
32	0_CHIP11_OUT 0N	69	0_CHIP11_OUT 1N	32	AGND	69	DGND
33	0_CHIP11_OUT 0P	68	0_CHIP11_OUT 1P	33	AGND	68	DGND
34	0_CHIP9_OUT 0N	67	0_CHIP9_OUT 1N	34	0_CHIP12_OUT 0N	67	0_CHIP12_OUT 1N
35	0_CHIP9_OUT 0P	66	0_CHIP9_OUT 1P	35	0_CHIP12_OUT 0P	66	0_CHIP12_OUT 1P
36	0_CHIP7_OUT 0N	65	0_CHIP7_OUT 1N	36	0_CHIP10_OUT 0N	65	0_CHIP10_OUT 1N
37	0_CHIP7_OUT 0P	64	0_CHIP7_OUT 1P	37	0_CHIP10_OUT 0P	64	0_CHIP10_OUT 1P
38	0_CHIP5_OUT 0N	63	0_CHIP5_OUT 1N	38	0_CHIP8_OUT 0N	63	0_CHIP8_OUT 1N
39	0_CHIP5_OUT 0P	62	0_CHIP5_OUT 1P	39	0_CHIP8_OUT 0P	62	0_CHIP8_OUT 1P
40	AGND	61	DGND	40	0_CHIP6_OUT 0N	61	0_CHIP6_OUT 1N
41	CAL_INJECT0	60	DGND	41	0_CHIP6_OUT 0P	60	0_CHIP6_OUT 1P
42	0_CHIP4_OUT 0N	59	0_CHIP4_OUT 1N	42	DGND	59	DGND
43	0_CHIP4_OUT 0P	58	0_CHIP4_OUT 1P	43	DGND	58	DGND
44	0_CHIP3_OUT 0N	57	0_CHIP3_OUT 1N	44	OUT_CLK0n	57	SC_OUT0p
45	0_CHIP3_OUT 0P	56	0_CHIP3_OUT 1P	45	OUT_CLK0p	56	SC_OUT0n
46	0_CHIP2_OUT 0N	55	0_CHIP2_OUT 1N	46	DGND	55	RESET0p
47	0_CHIP2_OUT 0P	54	0_CHIP2_OUT 1P	47	DGND	54	RESET0n
48	0_CHIP1_OUT 0N	53	0_CHIP1_OUT 1N	48	SC_IN0p	53	BCO_CLK0p
49	0_CHIP1_OUT 0P	52	0_CHIP1_OUT 1P	49	SC_IN0n	52	BCO_CLK0n
50	AGND	51	DGND	50	AGND	51	DGND

Terminator Design and Schedule

- Need to make AC, BD type (AC, BD type are incompatible) for Station-0 (60 pins) and Station-1,2,3 (100 pins) types.
- Searching for 60 pin type DF18 connectors (discontinued long time ago)
- Terminate only 100Ω LVDS pairs. Rests remain open.
- Employ double sided circuit boards (2 x DF18 in the bottom side and 100Ω resisters on the top side.)
- The board suppose to be as small as possible not to interfere with adjacent connectors. The board should have a symbol to indicate the orientation. (Rotation asymmetric).

Schedule

- Layout Design : 2 weeks
- 60 pin type DF18 procurement : Unknown
- Print board fabrication : 2 weeks
- Component implementation : 2 weeks
- Expected delivery of 3 x 4 types in middle of October~

More sophisticated termination?

受信側 ― 差動ペア終端（LVDS）

LVDS差動ペアでは、**図6**のように差動伝送路の特性インピーダンスに合わせ受信端部分に100Ω程度で終端しています。デバイスに終端抵抗が内蔵されている場合は、100Ω（標準）が多く、使用する基板、コネクター、ケーブルの伝送路はこの内蔵終端に合わせて差動特性インピーダンス100Ωで設計することになります。

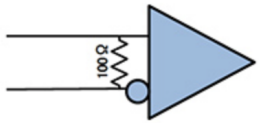
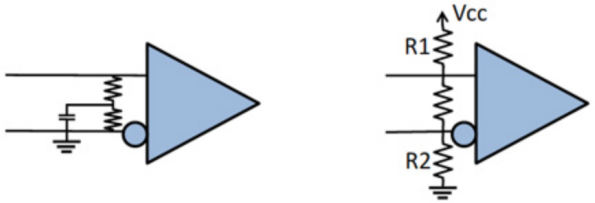


図6：LVDS差動ペアの受信端終端

この100ΩのLVDS受信部終端はコモンモードが浮いているため、外部終端では**図7**のように2つの50Ω抵抗の間のコモンモードに低インピーダンスパスを付け、不要輻射ノイズを低減する方法も可能です。また**図8**は入力がハイインピーダンス時に出力が不安定になる場合の対応方法としてプラスとマイナスラインに10K～20KΩ程度の抵抗を介してVccとGNDへ接続し小さいバイアス電流を流して電位差を与える外部フェイルセーフバイアス付きの終端になります。



左＝図7：コモンモードノイズ低減終端 ／ 右＝図8：フェイルセーフバイアス付き終端

送信端の直列抵抗による終端とRC終端

大振幅のシングルエンド信号を用いた基板上のデバイス同士やバス接続の伝送路では、受信部の終端は通常使用されていません。特性インピーダンスに合わせた終端抵抗がない伝送路では、受信端で信号が反射し、そのエネルギーが送信端へ戻ってきます。ただ、ドライバーの出力インピーダンスが20～30Ω程度の場合、50Ω伝送路では **図9**のように30～20Ω程度の直列抵抗を送信の出力端子の近傍に付けると、受信端のハイインピーダ

送信端の直列抵抗による終端とRC終端

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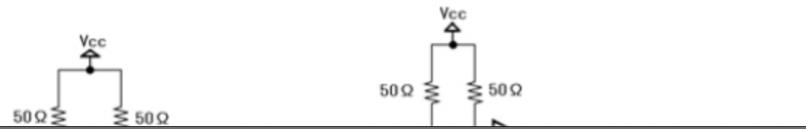
左＝図9：送信側／直列抵抗での終端 ／ 右＝図10：受信側／RC終端

送信端の直列抵抗による終端方法は、ある程度高速なシングルエンド信号の反射によるリンギングの対策として使用されており、リファレンス回路などのクロックラインやバス信号の部分でよく採用されている構成です。受信側では部品点数が多くなりますが、**図10**のように終端抵抗部の電力消費を抑えた、抵抗＋コンデンサーのRC終端も可能です。

送受信 ― 両終端／CMLとLVDSの終端方式の違い

CMLドライバー／レシーバーでは **図11**のように送信側、受信側ともにVccへ終端しています。高速性に優れていますがLVDSの構成と比較するとドライバーの消費電力は大きくなります。



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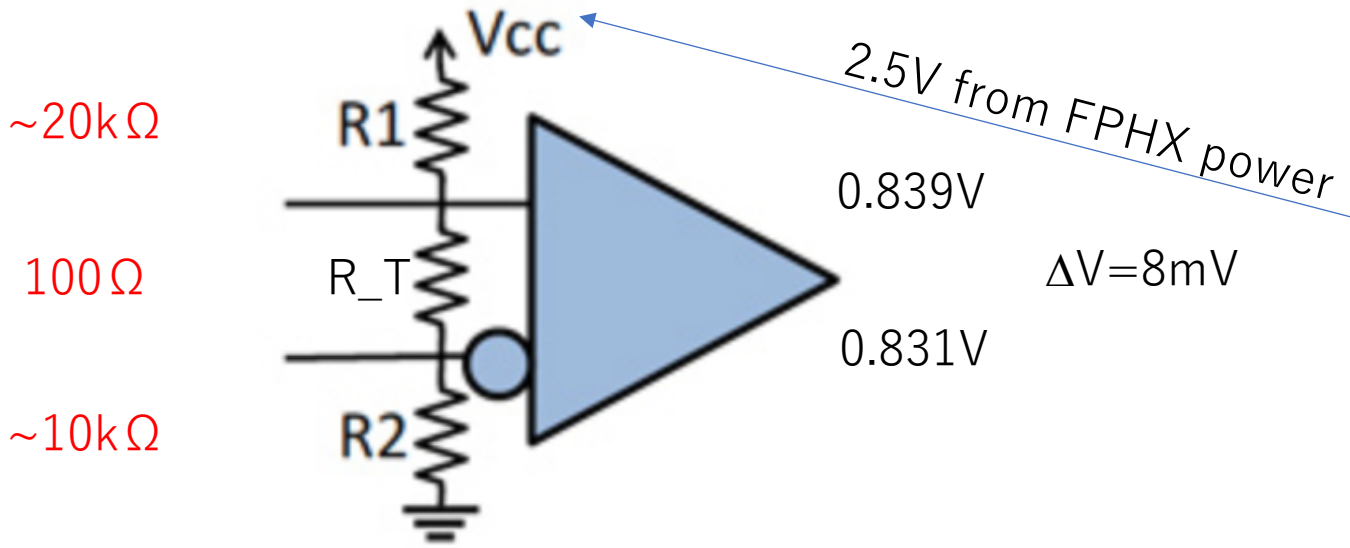

右＝図8：フェイルセーフバイアス付き終端

ROC Side							
RECEPTACLE (TOP)							
J1 (out side)				J2 (in side)			
#	name (net)	#	name (net)	#	name (net)	#	name (net)
1	AGND	100	DGND	1	AGND	100	DGND
2	DS1_CP01_OUT1P	99	DS1_CP01_OUT0P	2	SC_IN1P	99	RESET1P
3	DS1_CP01_OUT1N	98	DS1_CP01_OUT0N	3	SC_IN1N	98	RESET1N
4	DS1_CP02_OUT1P	97	DS1_CP02_OUT0P	4	DGND	97	BCO_CLK1P
5	DS1_CP02_OUT1N	96	DS1_CP02_OUT0N	5	DGND	96	BCO_CLK1N
6	DS1_CP03_OUT1P	95	DS1_CP03_OUT0P	6	OUT_CLK1P	95	SC_OUT1P
7	DS1_CP03_OUT1N	94	DS1_CP03_OUT0N	7	OUT_CLK1N	94	SC_OUT1N
8	DS1_CP04_OUT1P	93	DS1_CP04_OUT0P	8	DGND	93	DGND
9	DS1_CP04_OUT1N	92	DS1_CP04_OUT0N	9	DGND	92	DGND
10	CAL_INJECT1	91	DGND	10	DS1_CP06_OU	91	DS1_CP06_OUT0P
11	AGND	90	DGND	11	DS1_CP06_OU	90	DS1_CP06_OUT0N
12	DS1_CP05_OUT1P	89	DS1_CP05_OUT0P	12	DS1_CP08_OU	89	DS1_CP08_OUT0P
13	DS1_CP05_OUT1N	88	DS1_CP05_OUT0N	13	DS1_CP08_OU	88	DS1_CP08_OUT0N
14	DS1_CP07_OUT1P	87	DS1_CP07_OUT0P	14	DS1_CP10_OU	87	DS1_CP10_OUT0N
15	DS1_CP07_OUT1N	86	DS1_CP07_OUT0N	15	DS1_CP10_OU	86	DS1_CP10_OUT0P
16	DS1_CP09_OUT1P	85	DS1_CP09_OUT0P	16	DS1_CP12_OU	85	DS1_CP12_OUT0P
17	DS1_CP09_OUT1N	84	DS1_CP09_OUT0N	17	DS1_CP12_OU	84	DS1_CP12_OUT0N
18	DS1_CP11_OUT1P	83	DS1_CP11_OUT0P	18	AGND	83	DGND
19	DS1_CP11_OUT1N	82	DS1_CP11_OUT0N	19	AGND	82	DGND
20	DS1_CP13_OUT1P	81	DS1_CP13_OUT0P	20	AGND	81	DGND
21	DS1_CP13_OUT1N	80	DS1_CP13_OUT0N	21	AGND	80	VDD(+2.5V)
22	AGND	79	DGND	22	AGND	79	VDD(+2.5V)
23	AGND	78	DGND	23	VA(+2.5V)	78	VDD(+2.5V)
24	VA(+2.5V)	77	VDD(+2.5V)	24	VA(+2.5V)	77	VDD(+2.5V)
25	VA(+2.5V)	76	VDD(+2.5V)	25	VA(+2.5V)	76	VDD(+2.5V)
26	VA(+2.5V)	75	VDD(+2.5V)	26	VA(+2.5V)	75	VDD(+2.5V)
27	VA(+2.5V)	74	VDD(+2.5V)	27	VA(+2.5V)	74	VDD(+2.5V)
28	AGND	73	DGND	28	VA(+2.5V)	73	VDD(+2.5V)
29	AGND	72	DGND	29	AGND	72	VDD(+2.5V)
30	DS0_CP13_OUT0N	71	DS0_CP13_OUT1N	30	AGND	71	VDD(+2.5V)
31	DS0_CP13_OUT0P	70	DS0_CP13_OUT1P	31	AGND	70	DGND
32	DS0_CP11_OUT0N	69	DS0_CP11_OUT1N	32	AGND	69	DGND
33	DS0_CP11_OUT0P	68	DS0_CP11_OUT1P	33	AGND	68	DGND
34	DS0_CP09_OUT0N	67	DS0_CP09_OUT1N	34	DS0_CP12_OU	67	DS0_CP12_OUT1N
35	DS0_CP09_OUT0P	66	DS0_CP09_OUT1P	35	DS0_CP12_OU	66	DS0_CP12_OUT1P
36	DS0_CP07_OUT0N	65	DS0_CP07_OUT1N	36	DS0_CP10_OU	65	DS0_CP10_OUT1N
37	DS0_CP07_OUT0P	64	DS0_CP07_OUT1P	37	DS0_CP10_OU	64	DS0_CP10_OUT1P
38	DS0_CP05_OUT0N	63	DS0_CP05_OUT1N	38	DS0_CP08_OU	63	DS0_CP08_OUT1N
39	DS0_CP05_OUT0P	62	DS0_CP05_OUT1P	39	DS0_CP08_OU	62	DS0_CP08_OUT1P
40	AGND	61	DGND	40	DS0_CP06_OU	61	DS0_CP06_OUT1N
41	CAL_INJECT0	60	DGND	41	DS0_CP06_OU	60	DS0_CP06_OUT1P
42	DS0_CP04_OUT0N	59	DS0_CP04_OUT1N	42	DGND	59	DGND
43	DS0_CP04_OUT0P	58	DS0_CP04_OUT1P	43	DGND	58	DGND
44	DS0_CP03_OUT0N	57	DS0_CP03_OUT1N	44	OUT_CLK0N	57	SC_OUT0P
45	DS0_CP03_OUT0P	56	DS0_CP03_OUT1P	45	OUT_CLK0P	56	SC_OUT0N
46	DS0_CP02_OUT0N	55	DS0_CP02_OUT1N	46	DGND	55	RESET0P
47	DS0_CP02_OUT0P	54	DS0_CP02_OUT1P	47	DGND	54	RESET0N
48	DS0_CP01_OUT0N	53	DS0_CP01_OUT1N	48	SC_IN0P	53	BCO_CLK0P
49	DS0_CP01_OUT0P	52	DS0_CP01_OUT1P	49	SC_IN0N	52	BCO_CLK0N
50	AGND	51	DGND	50	AGND	51	DGND