The Development of a Versatile Data Acquisition System for Detector R&D - CaRIBOu

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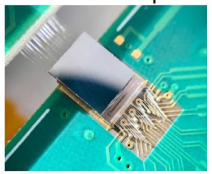
Outline

- Introduction of CaRIBOu (Control and Readout Integrated Board)
- Current CaRIBOu System
- Upgrade of CaRIBOu System

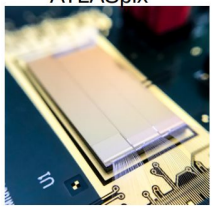
Introduction of CaRIBOu - Motivation

- Many different silicon detector technologies under investigation have
  - **Similar DAQ requirements**: readout, control, powering for most silicon pixel detectors, such as
    - **CLIC :** CLICpix1/2,C3PD, ATLASPix(2-3),CLICTD, Fastpix
    - **RD50 Collaboration:** RD50-MPW1, RD50-MPW2
    - **ATLAS:** ATLASPix series, CCPD
    - **NASA/AMEGO :** ASTROpix v1-2
    - **EIC:** LGAD for Roman Pots project (foreseen)
  - Differences in voltage levels, number of channels (data/voltage) or protocols
- Provide a versatile DAQ system which offers **re-usable hardware, firmware and software components**
- Minimize repetitive DAQ development tasks to focus on ASIC/Sensor characterization

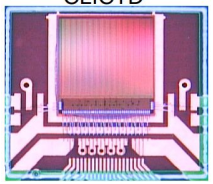
C3PD + CLICpix2



ATLASpix

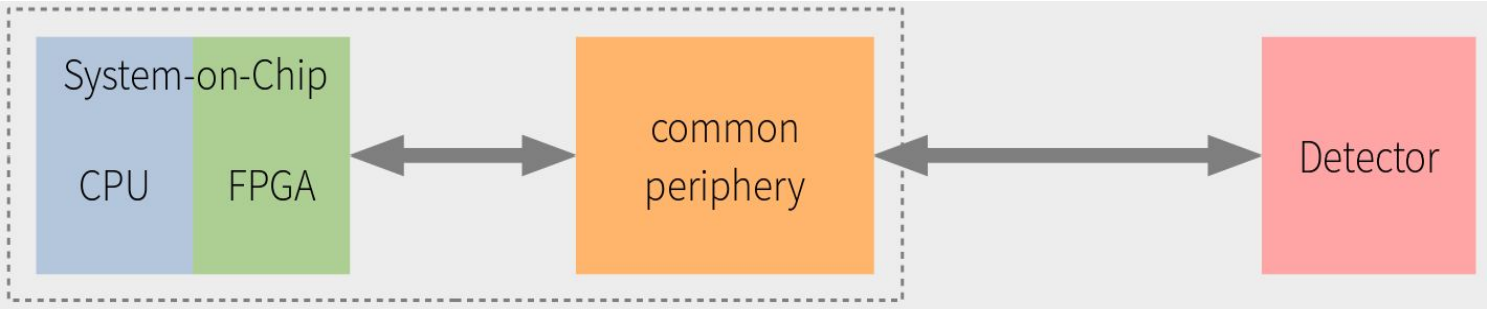


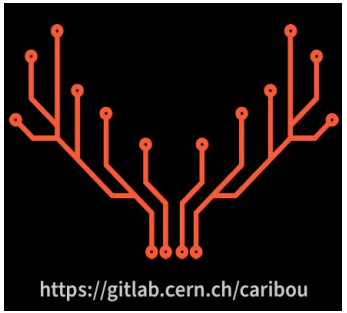
CLICTD



ASTROPIXv1

Introduction of CaRIBOu - Architecture





The CaRIBOu DAQ system is a **generic hardware, firmware and software platform** for different experiments. It consists, common periphery board and:

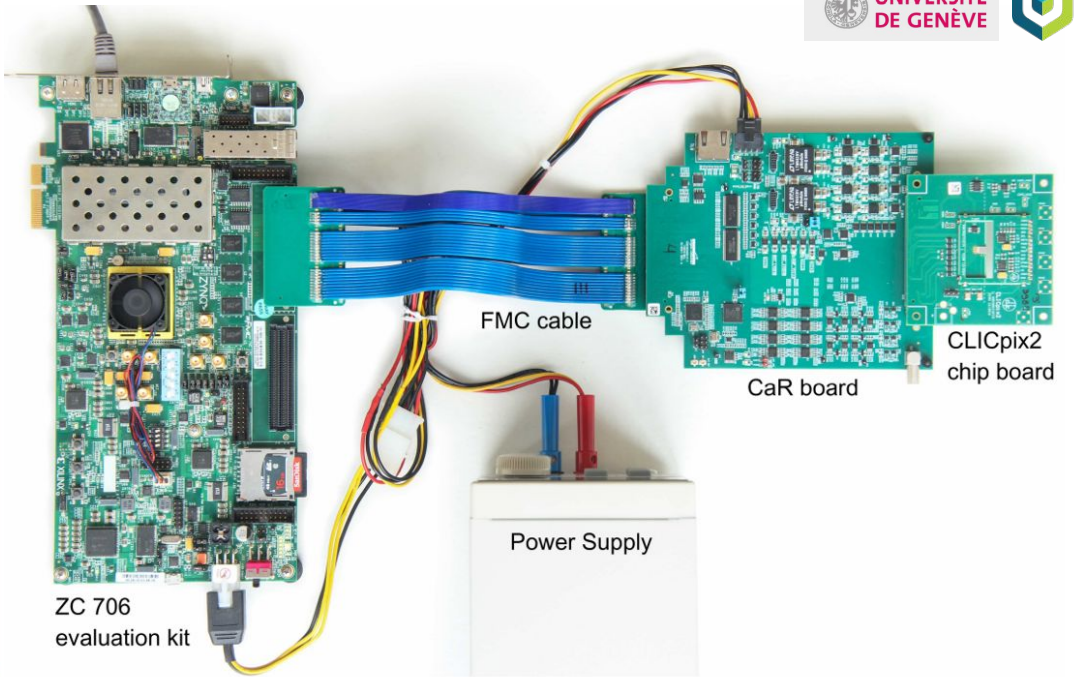
- A simple and low cost **SoC FPGA** platform
- A **common periphery board**
- An **Application-specific detector carrier board** - Detector chip and passive components only
- Common **software tool and source code**

Introduction of CaRIBOu - Advantages

The CaRIBOu DAQ system has several advantages:

- promote **reusability and sharing** of code between users
- **reducing development time** when integrating new ASIC or connecting to larger detector systems
- **quick development** of a readout system for R&D activities

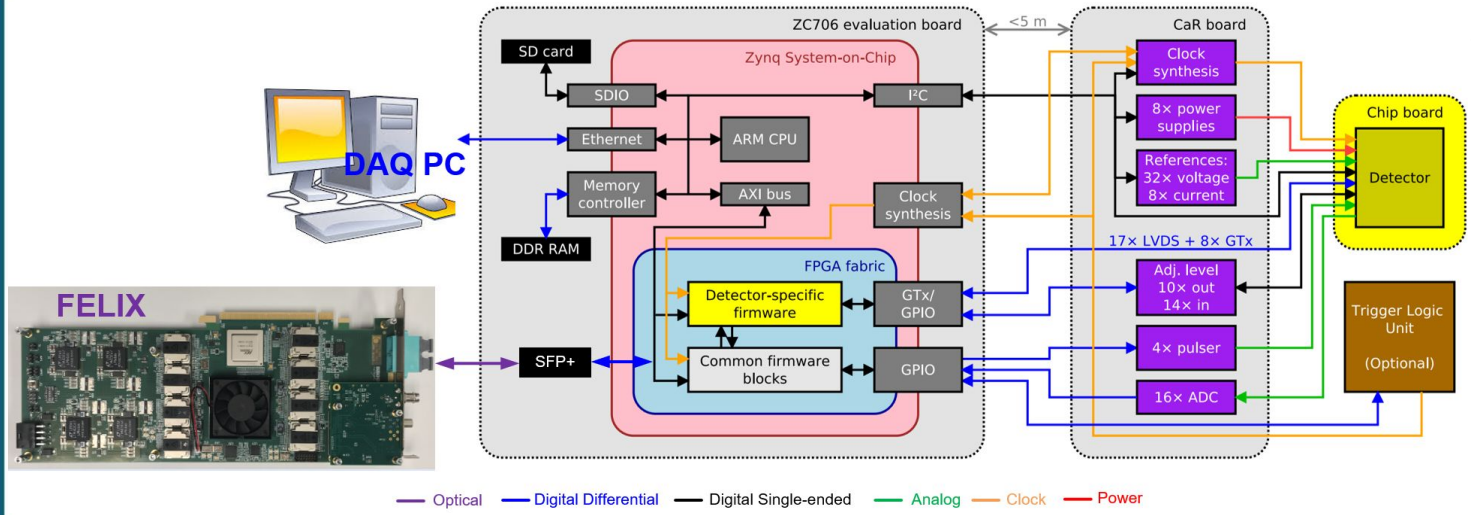
Current CaRIBOu System - Hardware



The current CaRIBOu DAQ system consists of:

- A Xilinx ZYNQ-7000 SoC FPGA based **ZC706** evaluation board
- A Control and Readout (**CaR**) board
- An Application-specific detector carrier board

CaRIBOu System - Block Diagram



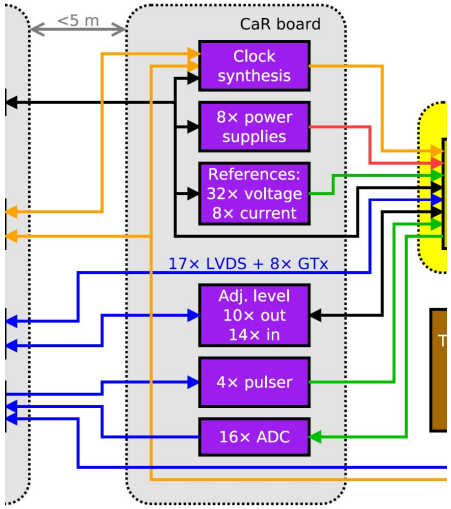
The block diagram of CaRIBOu DAQ system is shown on the left:

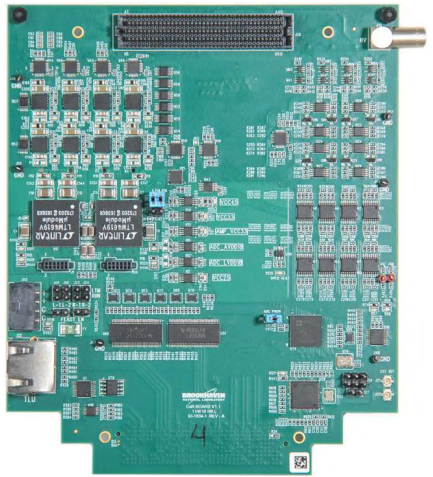
- ZC706 provides the CPU/Ethernet/SD/DDR4/MMCM/GPIO/I2C/GTX
- It also has the SFP+ optical link to **FELIX**
- FMC cable between ZC706 and CaR
- 320 pin SEAF connector for chip board

CaR Board

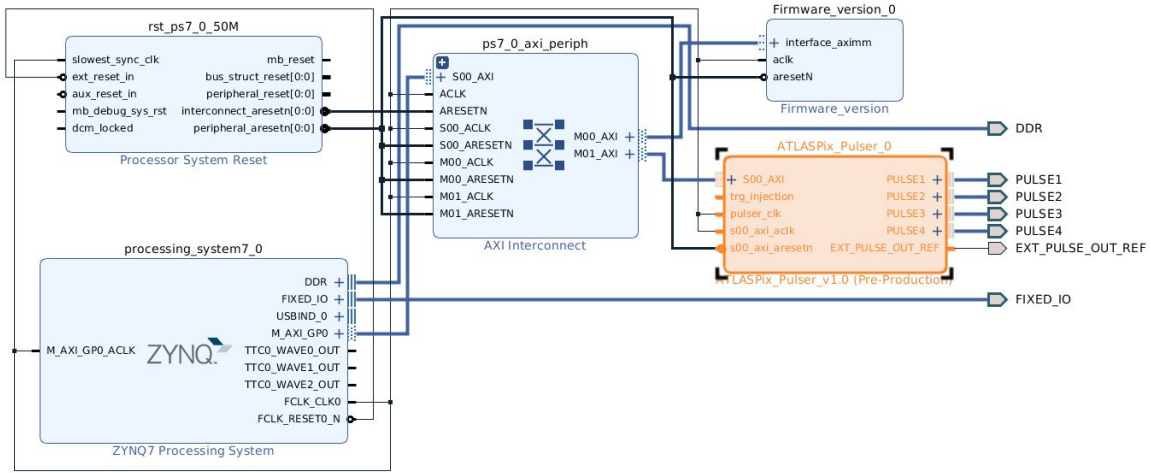
The CaR board has below features to support the different chips/ASICs

- 8 adjustable power supplies with monitoring
- 8-input 12-bit ADC with 50 kSamples/s (I2C interface)
- 16-input 14-bit ADC with 65 MSamples/s (parallel interface)
- 4 injection pulsers with adjustable pulse amplitude
- 32 adjustable voltage references
- 8 adjustable current references
- 10 output and 14 input single-ended links with adjustable voltage level
- 17 bidirectional LVDS links (up to 1.1 Gb/s)
- 8 full-duplex high-speed MGT links (0.8-12 Gb/s)
- programmable clock generator with external reference input
- interface for trigger and time reference (3 LVDS I/O + 1 LVDS clock)
- FMC connector to SoC platform





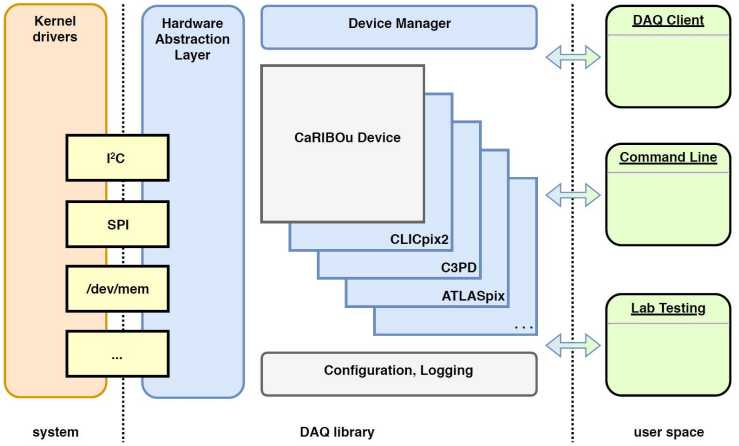
Current CaRIBOu System - Firmware

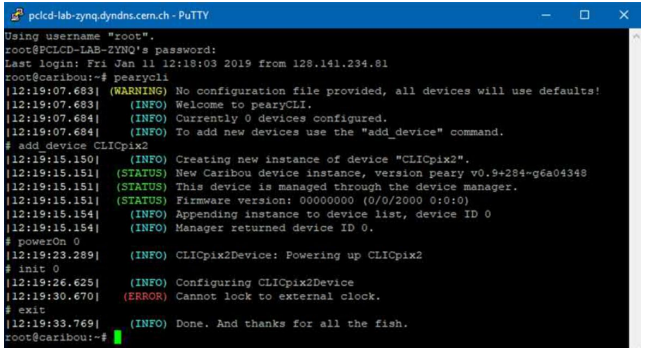


- Minimal core image : https://gitlab.cern.ch/bnl-caribou/cariboucore
- Processor configured for CaR board
- Firmware IP to read FW version
- Base script for project generation, CI

Current CaRIBOu System - Software

- System: Yocto- and OpenEmbedded-based Linux ("Poky")
- DAQ library ("Peary") containing:
  - Hardware Abstraction Layer (HAL), allowing to handle hardware peripherals as objects in C++
  - C++ templates for implementing a new user device
  - Logging with multiple verbosity levels
  - Device manager supports multiple devices in parallel
  - Command line interface for standalone operation
  - Client interface for integration with another DAQ



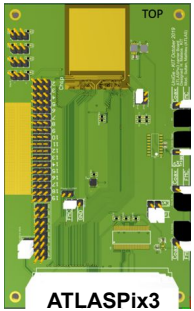


Current CaRIBOu - In Several Experiments

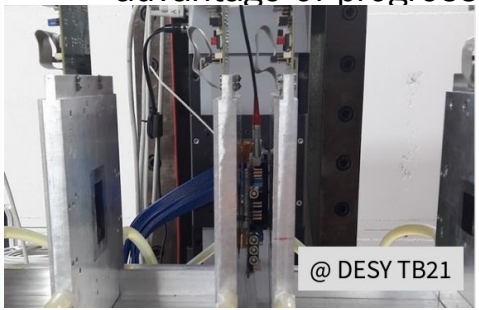

RD50-MPW1/2

The CaRIBOu system have been developed and widely used for many R&D projects by a large community:

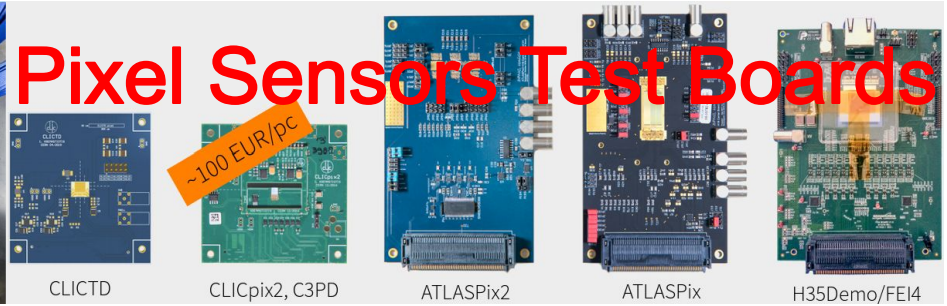
- Various monolithic pixel sensors (HV-CMOS/HV-MAPS CCPD, H35DEMO, ATLASPix, ATLASPix2, CLICpix2, C3PD, CLICTD) **have been characterized in the test beam with the CaRIBOu system** and **FELIX**-based readout at **DESY, CERN and FNAL**
- Adopted by **CERN EP-DT, RD50 Collaboration, IPHC Strasbourg, DESY, and NASA** for ongoing R&D
- Future development will focus on reducing costs while increasing resources by taking advantage of progress in FPGAs



ATLASPix3



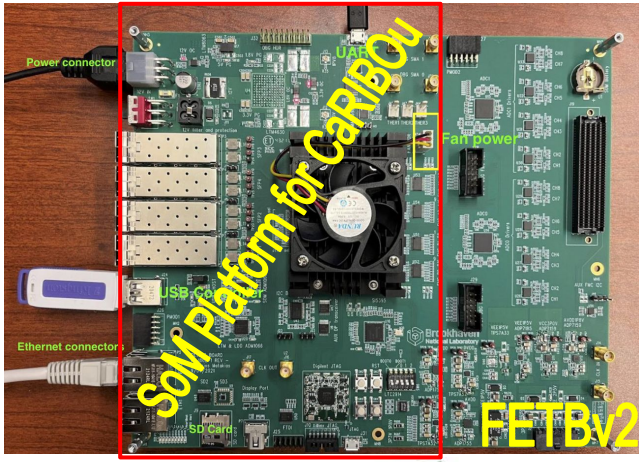
Pixel Sensors Test Boards



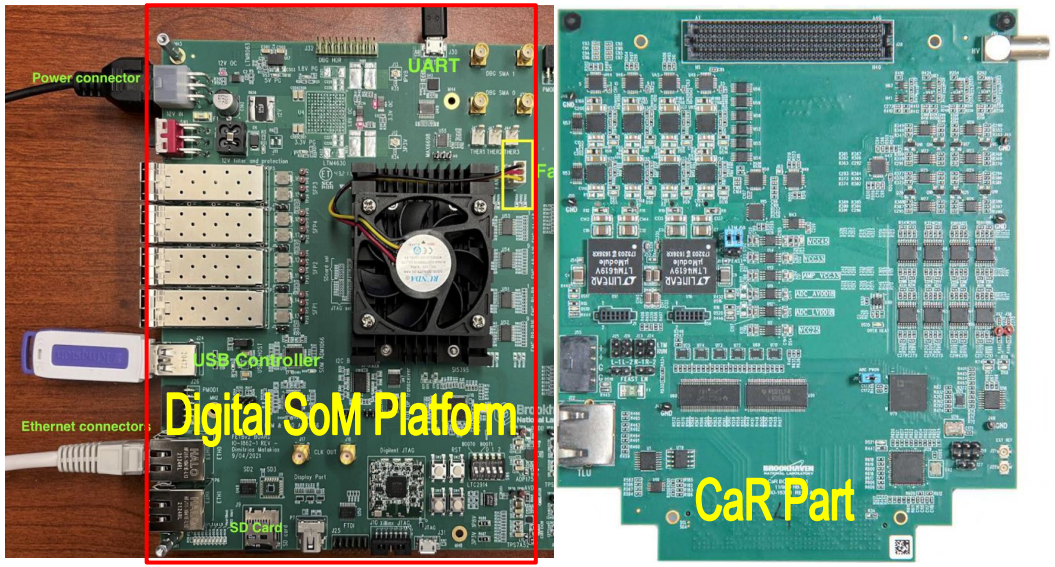
Upgrade of CaRIBOu System

Future development will focus on reducing costs while increasing resources by taking advantage of progress in FPGAs:

- using commercial System-on-Module (SOM) to optimize the system cost for easy deployment in different experiments.
- possible utility of AI/ML
- The user community is being expanded with **collaboration** of:
  - CERN EP R&D program
  - EU H2020 Innovation Pilot program
  - in addition to the collaboration on advanced monolithic silicon sensors studies with RD50, CLIC, ALICE and NASA

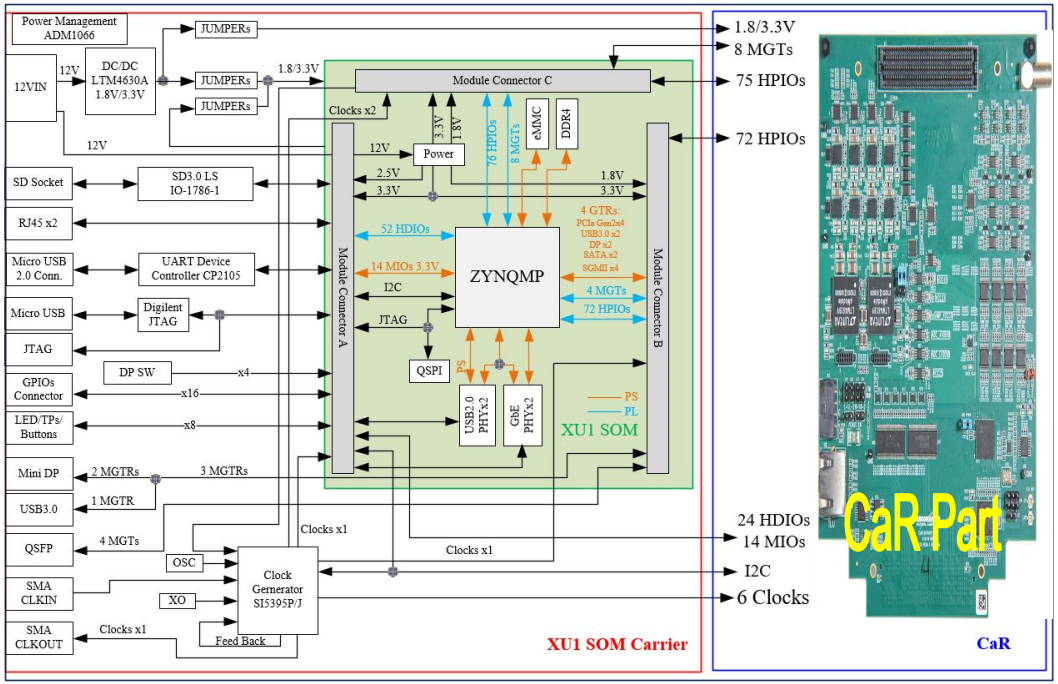


New CaRIBOu Hardware Block Diagram



- ZYNQ US+ SoC FPGA based SoM
  - More resources, AI/ML supported
  - More interfaces, ARM CPU processing power
- More GPIOs and up to 12.5 Gb/s MGT links
- Power management
- Integrated with CaR functionalities

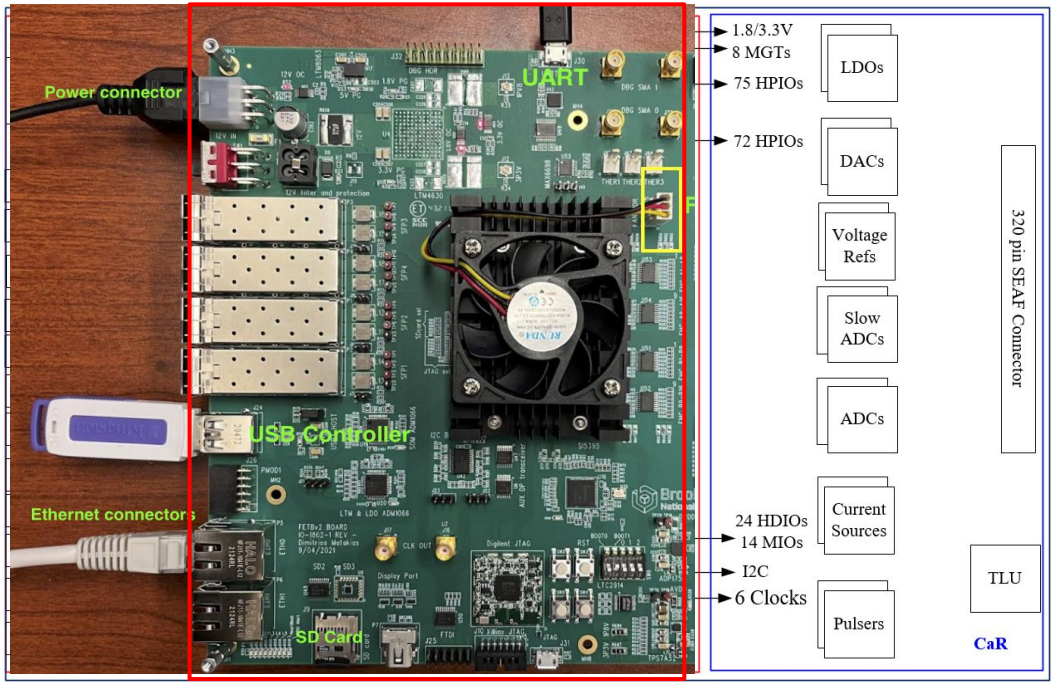
New CaRIBOu - SoM Based Platform



SoM Platform interfaces

- 12V power inputs
- SD card for boot and storage
- 2 RJ45 GbE ports
- JTAG/GPIOs
- USB3.0 for storage
- 4 SFP+ for optical data transfer (10Gb/s)
- SMA external clock inputs
- SMA clock outputs
- 144 HPIOs/24 HDIos/Clocks/I2C/8 GTHs

New CaRIBOu - CaR Functionalities



The CaR is planned to be integrated together with SoM platform. It includes:

- LDOs
- DACs
- Voltage references
- Slow ADCs
- High speed ADCs
- Current sources/references
- Pulsers
- TLU
- 320 pin connector

Summary

- The focus of the BNL TDAQ R&D program is the **integration of unique capabilities in detector technology, readout, and signal processing**
- **CaRIBOu** and **FELIX** have been developed with our collaborators and widely used in different experiments by large community
- The future work of **CaRIBOu** is well planned and the R&D is ongoing

Backup Slides

Collaborators

- Bern
- Carleton
- CERN
- CNRS/IN2P3 OMEGA
- Columbia
- DESY
- FNAL
- IFIN-HH
- LBNL
- Liverpool
- MIT
- MIT-LL
- NASA
- NIKHEF
- SUNY Polytechnic
- Stony Brook
- Stanford
- Wuppertal
- Yale
- CLIC
- CERN RD50

- ***Students, through collaborations or training programs are often part of these efforts.***

CaRIBOu V0 and V1