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The upgrade of the versatile data acquisition system -CaRIBOu

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Developing new detectors requires the design of an adequate readout and control system. Such a system typically consists of hardware in form of a readout board containing programmable logic to provide an interface to the detector chip, power supplies for biasing the sensor, as well as DACs and ADCs for setting and measuring operation parameters, generating test pulses, etc. The CaRIBOu system, a generic hardware, firmware and software platform for the quick development of a read-out solution for detector R&D activities [1] [2] has been designed. This system is designed to promote re-usability and sharing of code between users to reduce development time when integrating new sensor readout ASIC or connecting to larger detector systems like beam telescopes [3]. Various monolithic pixel sensors (e.g., HV-CMOS/HV-MAPS CCPD, H35DEMO and AT-LASPix) have been characterized in the test beam with the current CaRIBOu system and FELIX-based readout at CERN, FNAL and DESY [4]-[6]. Due to its versatility, this platform is being adopted by a large community such as CERN EP-DT, RD50 Collaboration, IPHC Strasbourg, DESY, and NASA for their ongoing R&D [7]-[11]. An upgraded CaRIBOu system development will take advantage of progress in FPGA technology, using commercial SOM to optimize the system cost for easy deployment in different experiments. The user community is being expanded with collaboration of the CERN EP R&D program, EU H2020 Innovation Pilot program, in addition to the collaboration on advanced monolithic silicon sensors studies with RD50, CLIC, ALICE, and NASA [12] [13].

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Presenter: TANG, Shaochun (BNL)

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