A 3ps Cryogenic Time-to-Digital Converter for Time-Correlated Single Photon Counting

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11/29/2022

CPAD 2022

Better TDC Precision Looks Like…

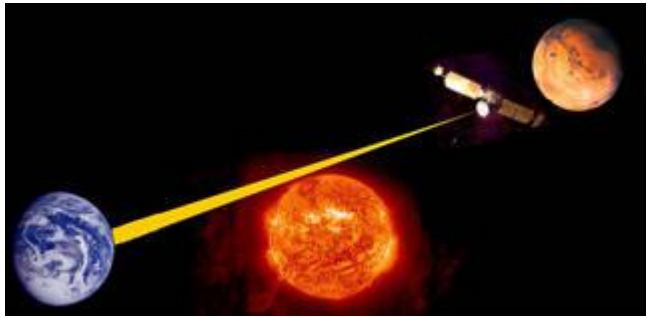


Image Credit NASA [1]

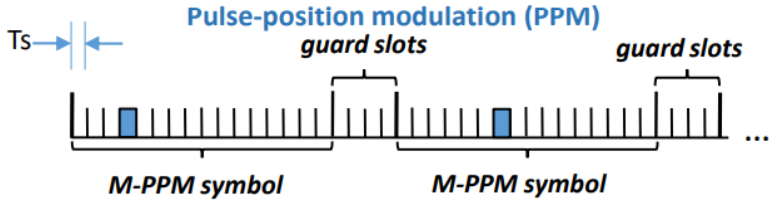
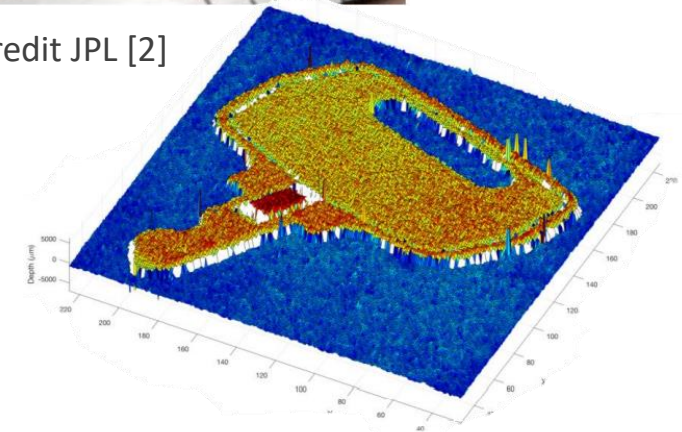


Image Credit JPL [2]

… higher bit-rates in DSOC.

Image Credit JPL [2]



… ultra-high resolution range-finding.

$(1\ \mathrm{ps} \approx 0.3\ \mathrm{mm})$

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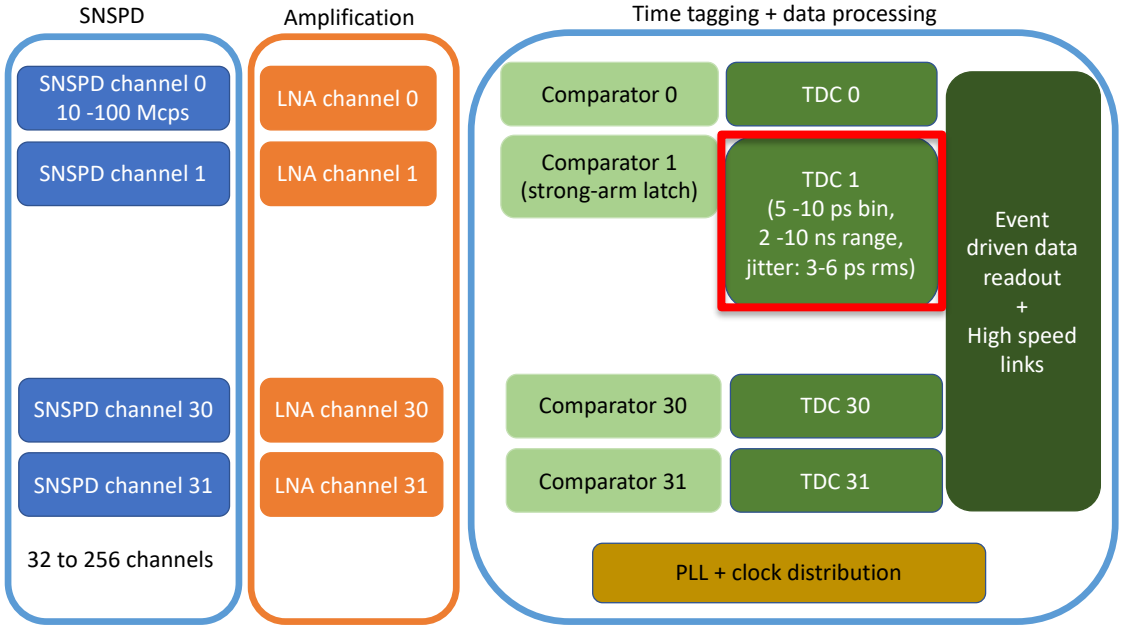
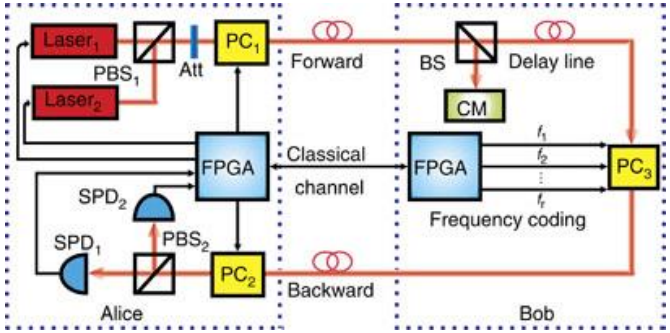
Why (This) TDC?

The Challenge: High-bandwidth time-correlated single photon counting in a cryogenic environment.



DOE NASA RFI 86 FR6315 [4]

1 – 10 Gcps



A Quantum Secure Direct Communications System (Hu [10])

Proposed Application: SNSPD-based space-to-ground quantum communications terminal for the ISS

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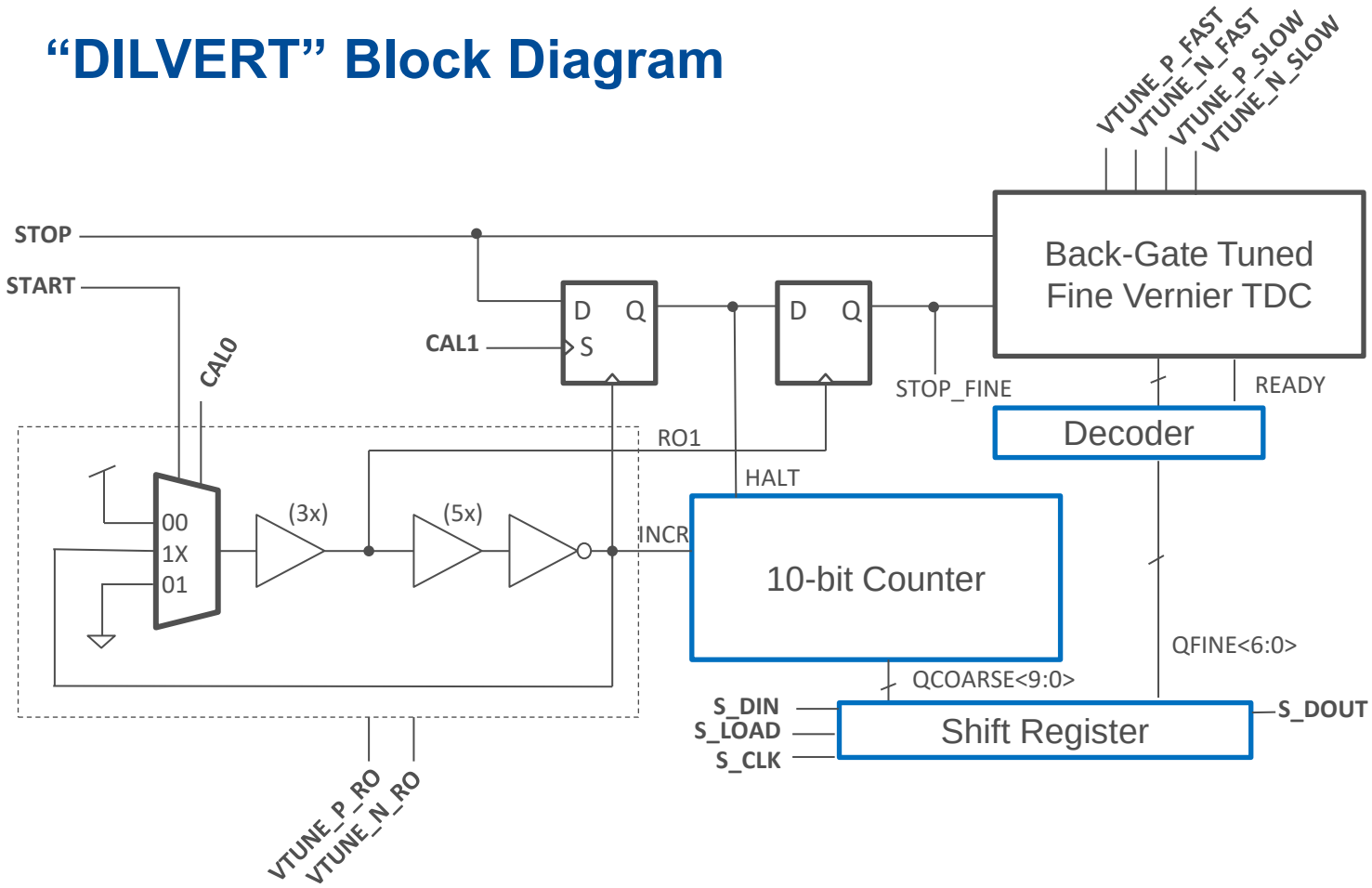
“DILVERT” Block Diagram

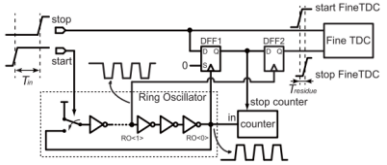


Total Pins: 22

- 6 analog inputs
- 7 digital inputs
- 3 digital outputs
- 6 power pins

Not Shown:

* RO1, HALT, INCR, and STOP_FINE are mux’d to **two** digital outputs with the select done by 4 shift register bits.
* RESET pin



Enomoto et al. [2]

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Fine Vernier TDC

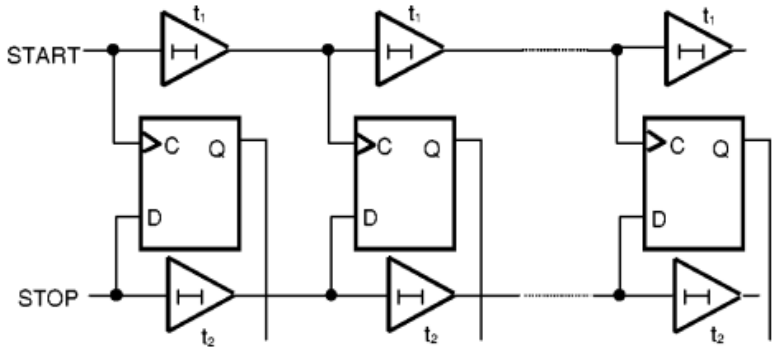

Illustration from Dudek [1]
(in our TDC, latches are used instead of DFFs)

- t_1 and t_2 are tuned to be very close to each other.
- 1 LSB = $t_{R(fine)} = (t_2 - t_1)$
- STOP is always faster than START.
- If START arrives first at stage *n*, Q[n]=1
- Result is thermometer-coded: “How many LSBs does it take for STOP to catch up to START?”

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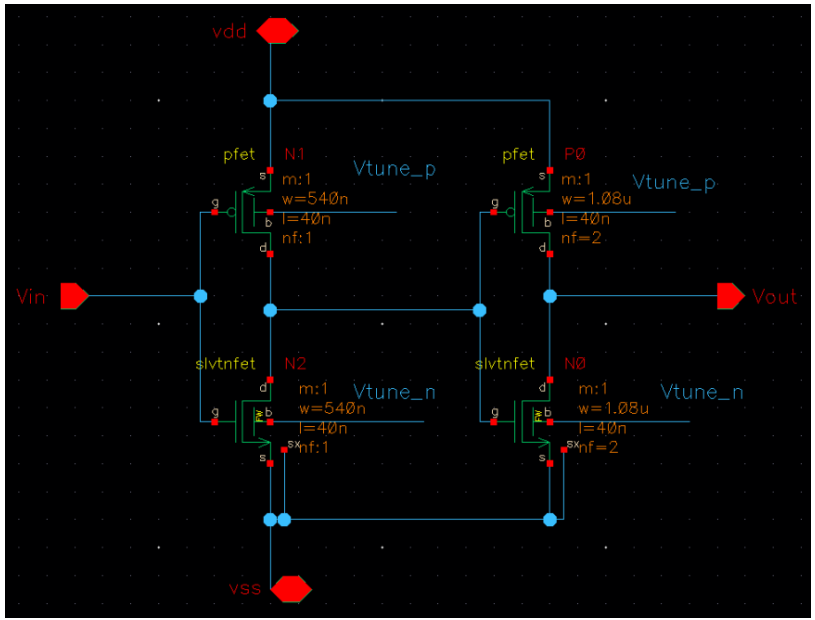
Delay Tuning with Back-Gate Bias



Fine TDC Delay Stage

- Fine TDC delay cells and RO delay cells are same architecture (different sizing)
- Speed is tuned by FDSOI back-gate biasing
  - Low complexity
  - Small footprint
  - No noise contribution from bias circuits
- 6 separate tuning voltages:
  - Fine TDC fast chain, slow chain, and coarse TDC ring oscillator
  - Tune NMOS and PMOS separately.
  - Both 0~2V w.r.t VSS

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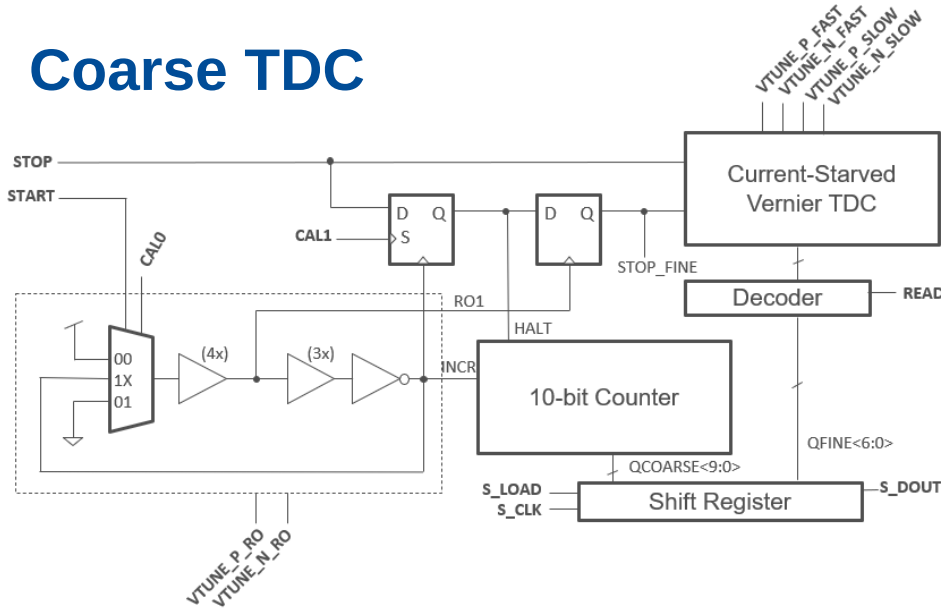
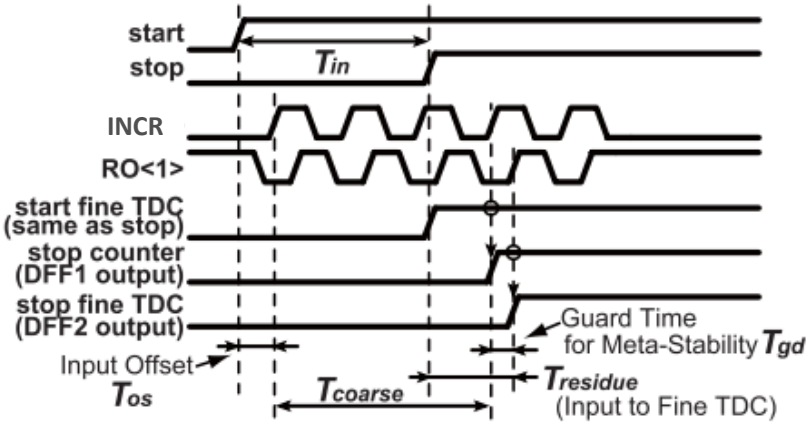
Coarse TDC





Enomoto et al. [2]

START starts the ring oscillator. The counter counts up until STOP, and the residue is encoded by the fine TDC:

$$T_{in} = T_{OS} + T_{coarse} + T_{gd} - T_{residue}$$
$$= (T_{OS} + T_{gd}) + N_{coarse}(t_{R(coarse)}) - N_{fine}(t_{R(fine)})$$

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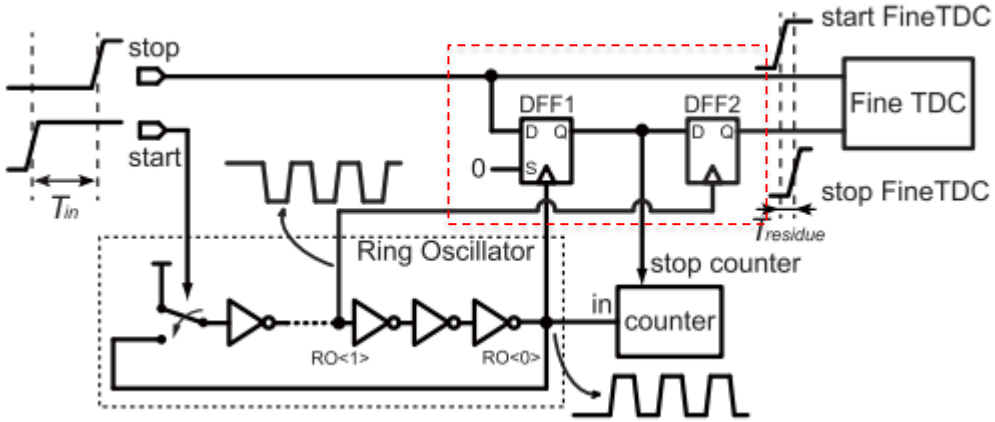
Coarse-to-Fine Coupling with DFFs



Enomoto, et al. [2]

- Traditional TDCs couple with a multiplexer → unwanted $T_{D\to Q}$, possibly different for different inputs. ☹
- In our design, DFF1 is triggered on the *first coarse TDC increment after STOP arrives.* (With constant offset $T_{clk\to Q}$)
- The remainder ($t_{incr} - t_{STOP}$) is digitized by the fine TDC.
- Why have DFF2? STOP and RO<0> are asynchronous, so we need to suppress any metastability in DFF1's output before the fine TDC.
- DFF2 is triggered slightly after DFF1 ($T_{incr} + T_{gd}$). We assume DFF1's output has settled within T_{gd}.

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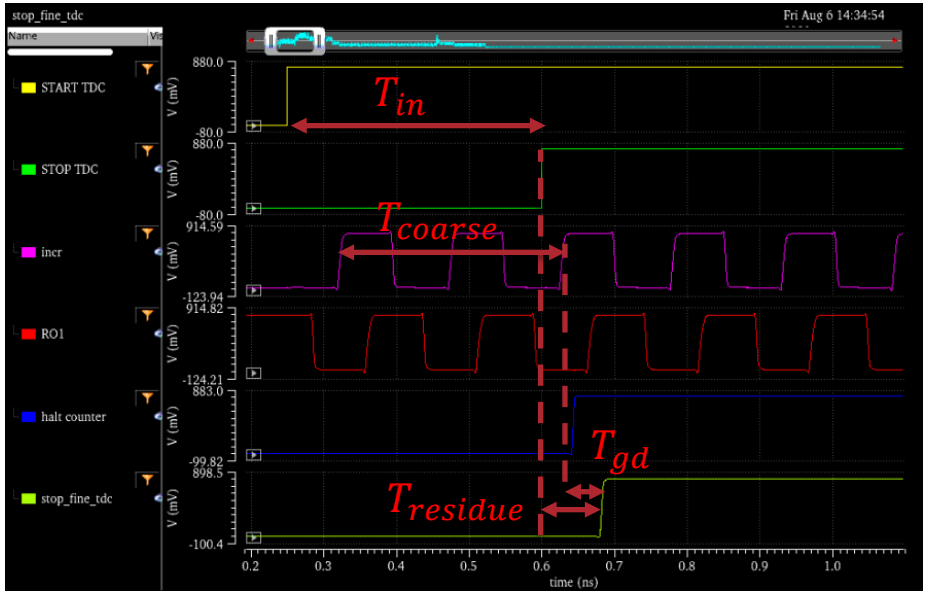
Example Measurement



From Three Point Calibration, we have:

$$t_{R(fine)} = -2.6375 \text{ ps}$$
$$t_{R(coarse)} = 152.75 \text{ ps}$$
$$T_{OS} + T_{gd} = -173.62 \text{ ps}$$

For this measurement, $Q_{fine} = 33$ and $Q_{coarse} = 4$, so:

$$T_{in} = T_{OS} + T_{coarse} + T_{gd} - T_{residue}$$
$$\approx 350.343 \text{ ps}$$

(Actual T_{in} was 350 ps, within 1 LSB of the measured value.)

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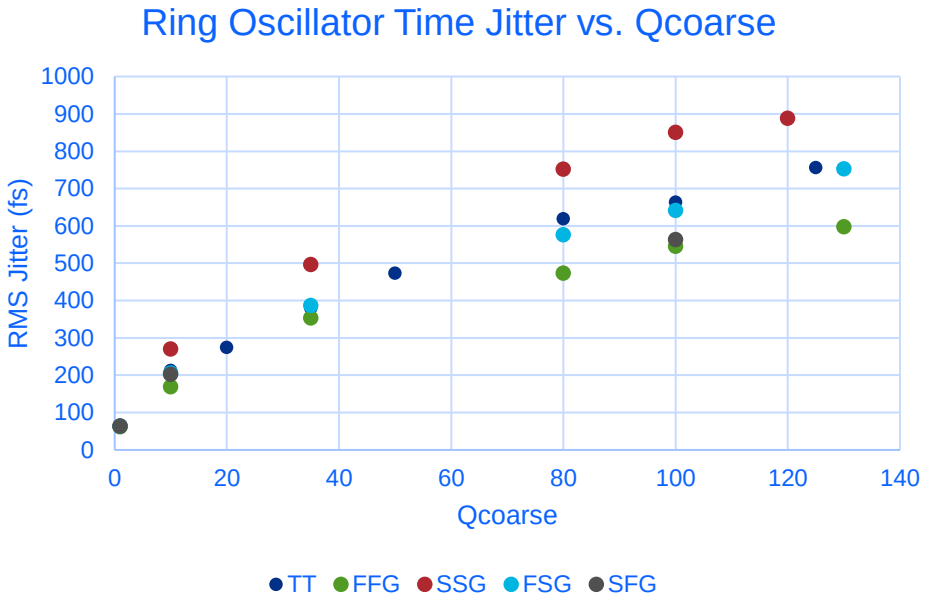
Simulation Results: TDC Jitter vs T_{in}

$$\sigma_{jitt} = \sigma_{tp} \times \sqrt{N_{stage} \times 2} \times \sqrt{Q_{coarse}}$$
$$= \kappa_{jitt} \sqrt{Q_{coarse}}$$

Assuming that maximum allowable jitter is approximately ½ LSB:

Corner:	TT	FF	SS	FS	SF
κ_{jitt} [fs]	66.18	55.9	80.7	65.0	61.7
$\sigma_{jitt(max)}$ [fs]	1.3	1.0	1.8	1.4	1.2
$Q_{coarse(max)}$	385	320	497	463	378
Dynamic Range [ns]	**55.4**	40.2	83.7	68.5	53.1



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State of the Art

	Chen ‘17	Sesta ’18	Enomoto ‘19	Palaniappan ‘19	Khaki ‘21	Lee ‘21	DILVERT (sim) ’21
Architecture	ΔΣ TDC	Counter + Vernier Delay Line	Counter + Pulse-Shrink Delay Line	Cap Boost Vernier Delay Line	ΔΣ TDC w/ GSRO	SAR TDC	Counter + Vernier Delay Line
Process	65nm	0.35 μm	0.18 μm	180 nm	40nm FPGA	130nm	22nm SOI
Resolution	0.48 ps	7 ps	2.0 ps	1.74 ps	0.18 ps	6.6 ps	2.7 ps
Dynamic Range	-	80 ns	120 ns	0.112 ns	4.5 ns	1.7 ns *	55.4 ns
Power	3 mW	-	18 mW	0.217 mW	9.24 mW	0.504 mW	0.5 mW
Rate	-	20 MS/s *	3.3 MS/s	50 MS/s	1600 MS/s	10 MS/s	100 MS/s
FoM	-	-	3.33	0.30	2.71	0.51	41.04

$$FoM = \frac{[\text{Dynamic Range in ns}]}{[\text{Power in mW}][\text{Resolution in ps}]}$$

* = calculated from available data

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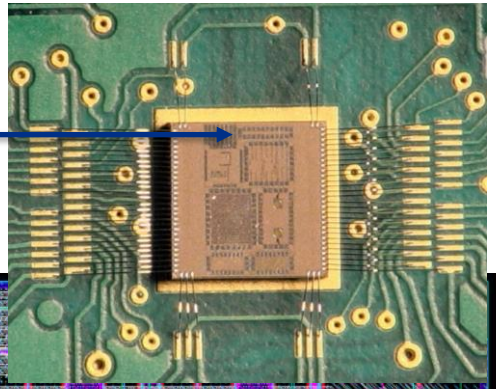
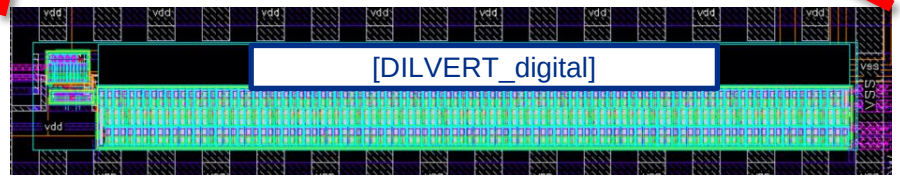
Test Chip 11/2021



≈ 250 µm

≈ 1000 µm

≈ 20 µm



≈ 150 µm

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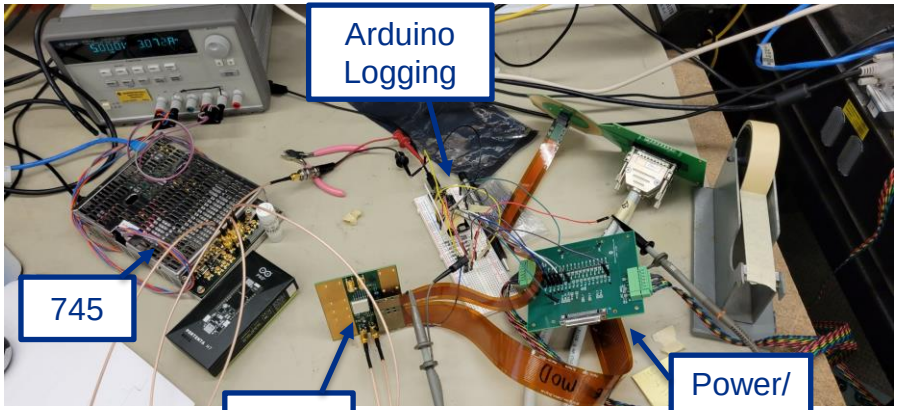
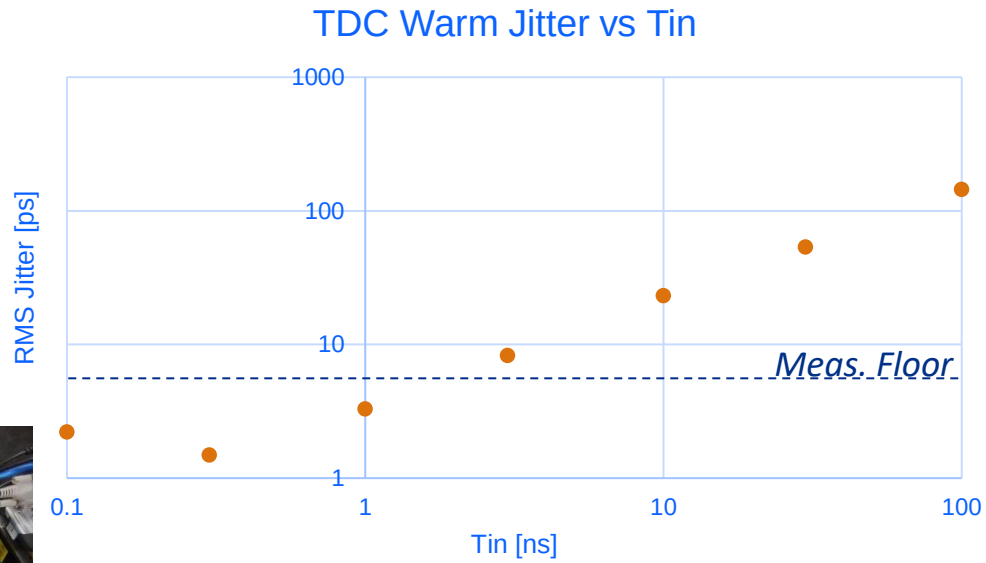
Preliminary Test Results (Room Temperature)

- Two pulses generated with Berkley Nucleonics 745-OEM (~ 5 ps rms jitter)
- RO runs slower and with more excess jitter than expected at room temperature.
- Cryo testing in progress.





Warm Simulation:

tR(coarse)	220.2 ps
tR(fine)	-6.0 ps
tOS	486.3 ps

Measurement:

tR(coarse)	524.4 ps
tR(fine)	-8.1 ps
tOS	-463.1 ps

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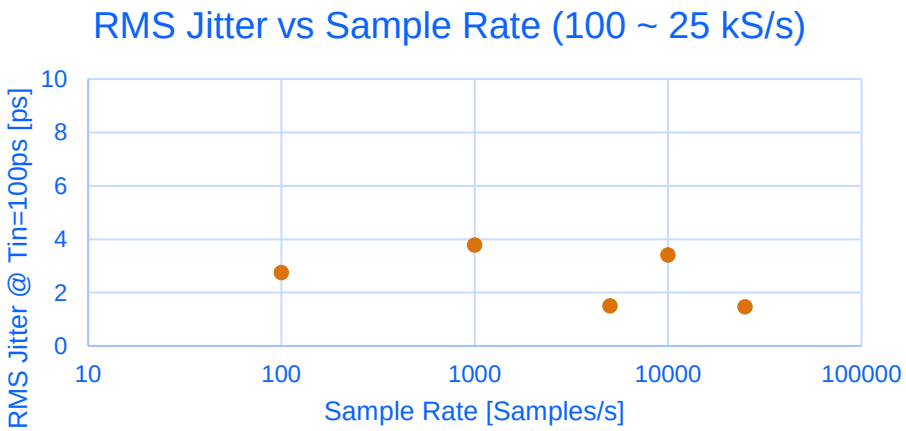
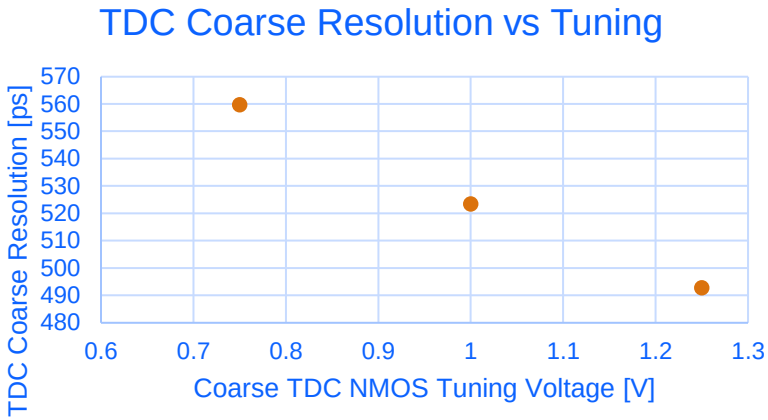
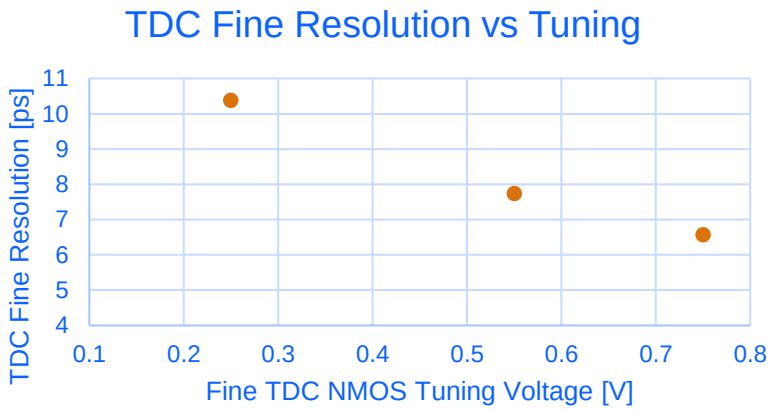
Performance vs Tuning Voltage & Sample Rate (Room Temperature)

- Demonstrated 25 kS/s, limited by readout chain.
- TDC Tuning slope: ≈**134 ps/V (coarse)**
  ≈**7.6 ps/V (fine)**







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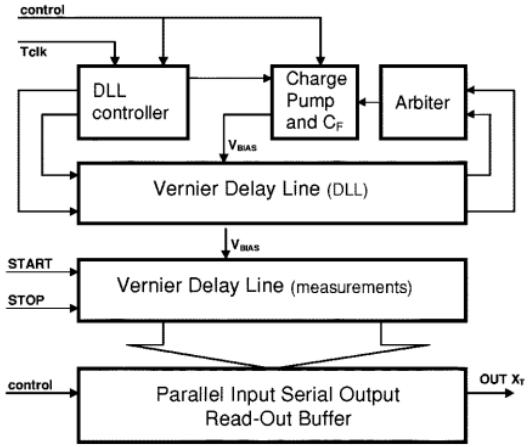
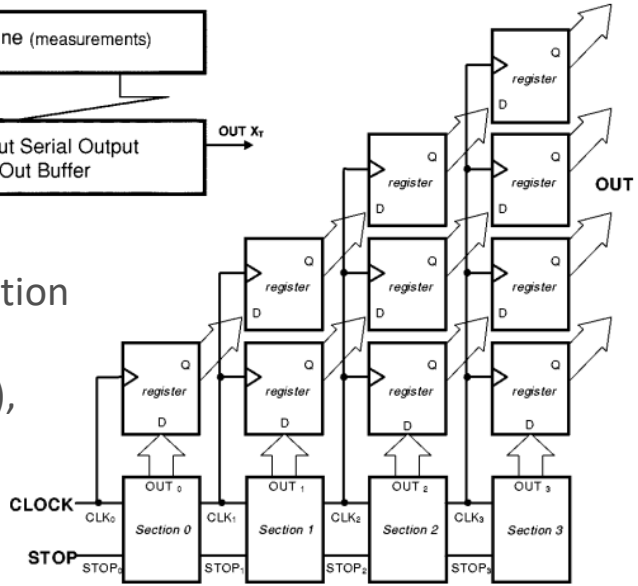
What's Next?

- Continue test chip characterization
- **Multi-Channel Prototype:** Power Saving in Ring Osc. / Clock Distribution
- **Full-Channel Integration** (SNSPDs, Comparators, etc.)
- Replica TDC for Delay-Locking
- High-Speed Read Pipelining
- Skewed Inverter Topologies





DLL implementation (top) and read pipelining (right), from Dudek [6]

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Thanks to Contributors

Fermilab ASIC Department:

D. Braga, F. Fahim, L. Dal Monte, P. Rubinov, P. Klabbers

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[7] R. Enomoto, T. Iizuka, T. Koga, T. Nakura and K. Asada, "A 16-bit 2.0-ps Resolution Two-Step TDC in 0.18- μm CMOS Utilizing Pulse-Shrinking Fine Stage With Built-In Coarse Gain Calibration," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 27, no. 1, pp. 11-19, Jan. 2019, doi: 10.1109/TVLSI.2018.2867505.

[8] B. V. Bockel, P. Leroux and J. Prinzie, "Tradeoffs in Time-to-Digital Converter Architectures for Harsh Radiation Environments," in *IEEE Transactions on Instrumentation and Measurement*, vol. 70, pp. 1-10, 2021, Art no. 2005710, doi: 10.1109/TIM.2021.3100355.

[9] Global Foundries. *22FDX Design Kit and Technology Training Book.* TTM-000022 Revision 9.

[10] Hu, Jianyong & Yu, Bo & Jing, Ming-Yong & Xiao, Liantuan & Jia, Suotang & Qin, Guo-Qing & Long, Gui. (2016). Experimental quantum secure direct communication with single photons. Light: Science & Applications. 5. e16144. 10.1038/lsa.2016.144.