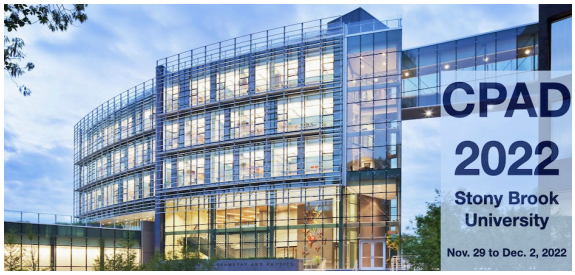

Contribution ID: **24** Type: **Contribution Talk**

A 3ps Cryogenic Time-to-Digital Converter for Time-Correlated Single Photon Counting

Thursday, 1 December 2022 08:30 (20 minutes)

We present a time-to-digital converter (TDC) that simultaneously achieves very low power and picosecond timing resolution when operated in a cryogenic (4K) environment. Such a TDC is an enabling technology for quantum secure direct communications which require high bandwidth time-correlated single photon counting. The proposed TDC uses a two-step architecture in which the input time delay is first coarsely digitized through a ring-oscillator based counter, and the residue is then finely digitized by a Vernier delay line "fine TDC." The TDC is implemented in an FD-SOI process, and back-gate tuning is used both to correct threshold variation due to cryogenic operation and to enable tuning of the fine TDC delay elements with very little overhead. Simulations show a fine TDC resolution of 2.7 ps with a dynamic range of > 50 ns at ½ LSB rms jitter, with power consumption of < 500 μW per channel. A prototype chip has been fabricated and is currently undergoing test.

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