





Front-End Evaluation for Pixelated Liquid-Argon Particle **Detectors**

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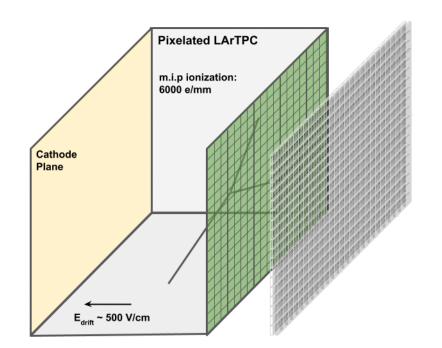




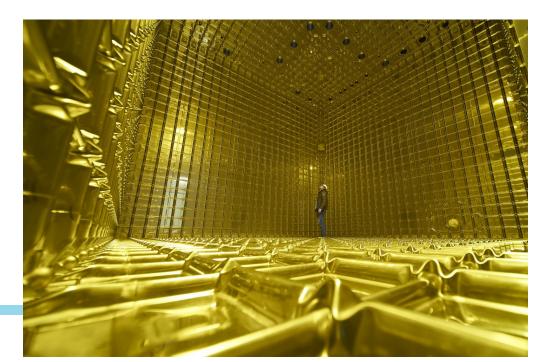


Introduction

- Time projection chambers detect spatial and temporal data of an event in order to reconstruct a 3-dimensional particle trajectory or interaction
- Modern TPC's utilize multi-wire planes held at a high voltage relative to the cathode
- The volume of the detector is filled with a charge sensitive bath (Liquid Argon for example)
- Q-Pix Collaboration aims to develop a pixelated self-triggering ASIC
- Front-end Investigation at Fermilab
 - Dynamic Vision Sensing
 - Charge Replenishment

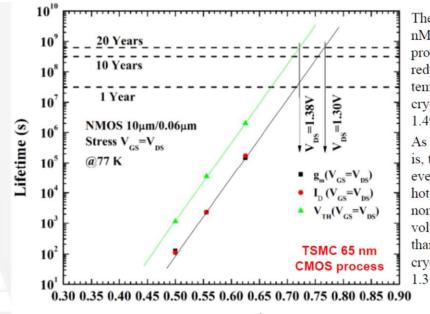


time



Q-Pix and 65nm

- Custom CMOS models at LAr temperatures
- Custom standard cell library
- IP extensively tested and validated at LAr temperatures
 - SLVDS Rx/Tx
 - PLL
 - Bandgap Reference
 - POR
 - 1.28Gbps line driver
 - Serializer
- Long-term availability and investment towards models and libraries
- Process for LHC upgrades
- Aligns with other experiments (MIDNA
 - CCD readout)



The predicted lifetime for 130 nm nMOS devices reaches 20 years provided the drain voltages are reduced from the nominal, room temperature value of 1.5 V to a cryogenic temperature value of 1.49 V.

As noteworthy as this prediction is, the 65 nm nMOS device is even more resistant to cryogenic hot carrier degradation. Its nominal, room temperature voltage of 1.2 V is already lower than the maximum allowable cryogenic temperature voltage of 1.3 V.

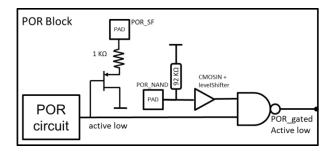
$$1/V_{DS} (V^1)$$

FERMILAB/SMU: J. R. Hoff, et al., IEEE TRANS. ON NUCLEAR SCIENCE, VOL.59, NO.4, AUGUST 2012

BNL: Shaorui Li, et al., IEEE TRANS. ON NUCLEAR SCIENCE, VOL.60, NO.6, DECEMBER 2013

FERMILAB/SMU: Guoying Wu, et al., IEEE TRANS. ON DEV. AND MATERIALS RELIABILITY, VOL.14, NO.1, MARCH 2014

FERMILAB/SMU: J.R.Hoff, et al., "Cryogenic Lifetime Studies of 130nm and 65nm CMOS Technologies for High-Energy Physics Experiments, in publishing in IEEE TRANS. ON NUCLEAR SCIENCE



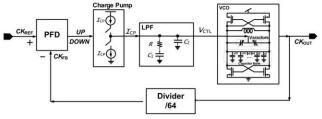
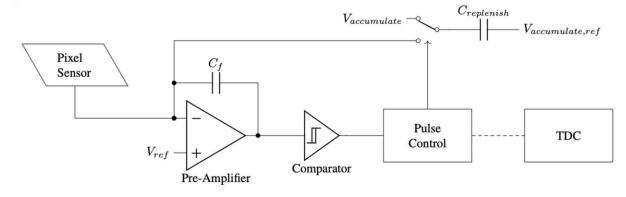


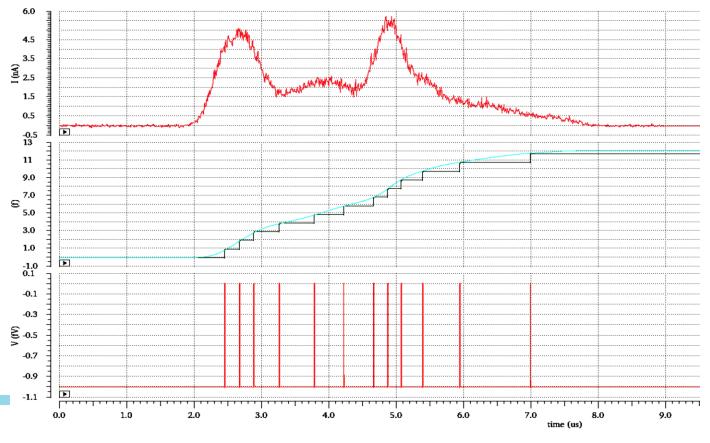
Fig. 4. The block diagram of a single path Phase Locked Loop (PLL)



Charge Replenishment Front-End

- Accumulation
- Replenishment
- Holes and Electron calibration
- Output of front-end is a timestamp of each packet of detected charge
- Reset time delays allow reconstruction of event





Performance & Future Work

- Simulation shows
 - ENC(@ 27 C): ~385 e⁻
 - ENC(@ -189 C): ~50 e⁻ @ 3pF pixel capacitance
 - Front-end readout limited to 10uW per channel
- 65nm 16 Channel Prototype
- Scale to full-chip with periphery and digital readout

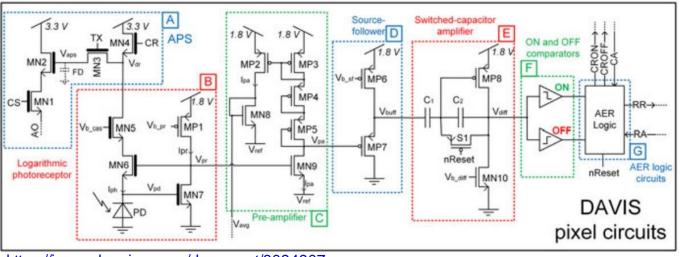
Front-end Block	Power (@ 1.2V)
Integrator + Leakage Compensator	<9.0 uW
Comparator	0.5 uW
Replenishment Control	<100 pW
Total (perpixel)	<10 uW



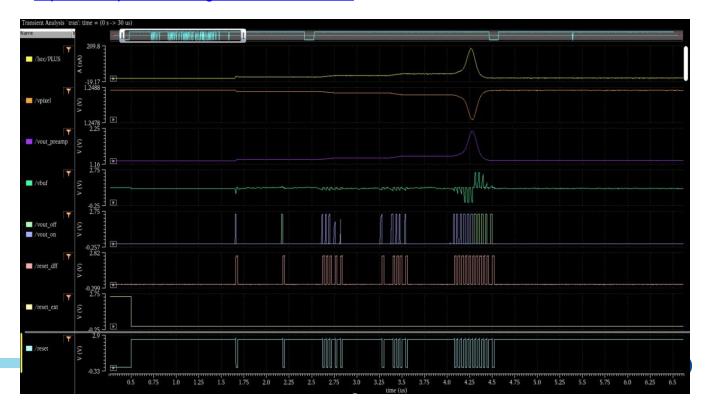
Dynamic Vision Front-End

- Dynamic Vision Sensor (DVS)
- Used for detecting changes in light intensity
- Potential candidate for photon detection front-end

$$\Delta V_{integ} = (-rac{C_i}{C_f})(\Delta i_{pix}R_f) = (-rac{C_i}{C_f})(rac{dq_{pix}}{dt}R_f)$$



https://ieeexplore.ieee.org/document/8094907



Summary

- Investigated a charge sensitive front-end for a 65nm process
- Investigated dynamic vision for a 65nm process
- Looking for collaborators for partnering on chip submissions









Thank You





















