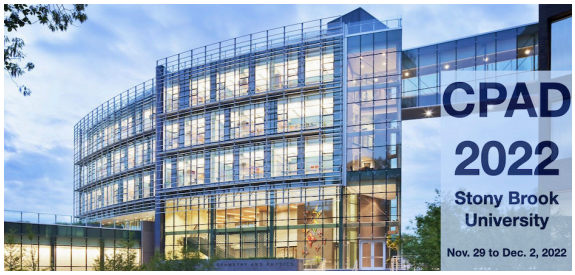

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Front-End Evaluation for Pixelated Liquid-Argon Particle Detectors

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Front-End Evaluation for Pixelated Liquid-Argon Particle Detectors

The physics reach and performance of high energy physics experiments based on multi-kiloton scale noble element time projection chambers, could benefit significantly from the development of a pixellated, large scale low power readout electronics.
As part of the Q-Pix collaboration, we investigated a low power front-end in a 65nm CMOS process, for operation in liquid Argon (-189°C).

Introduction

Large-scale noble element time projection chamber (TPC) detectors play a prominent role in existing and planned high-energy physics experiments, by virtue of their high detection efficiency, background rejection, and spatial and temporal resolution.
The current design for multi-Kiloton scale liquid Argon (LAr) TPCs, such as those being developed for the far detectors of the Deep Underground Neutrino Experiment [], rely on meter-scale sensing wires.
Conversely, a fully pixellated readout, as demonstrated for the smaller DUNE near detector \cite{LarPixConcept2020}, could lead to improved low-energy threshold and directional reconstruction, as well as easier module assembly.

The Q-Pix collaboration \cite{AsaadiSupernova,Nygren2018} aims at addressing the ensuing large channel count, higher data rate, and power constraints, by developing a self-triggering front end with free-running clocks and dynamically established data networks robust against single-point failure.

The Q-Pix collaboration is nearing completion of a first front-end prototype ASIC in a 180nm CMOS process. In this paper, we present the results of a parallel effort to investigate Q-Pix front-end design in a 65nm CMOS technology, the same used for the existing ASICs for the wire LAr TPC detector of the DUNE experiment \cite{CDP12019,GRACE2022}.
The process has been validated for operation in LAr, and would allow the collaboration to leverage existing resources, including device models for operation in LAr (-189°C), a fully characterized custom digital library with more than 300 standard cells, and a number of proven IPs \cite{BRAGA202136}.

The following sections describe the pixel design architecture and simulation results.

Front-End Design Architecture
Two analog front-end architectures were investigated. The first being dynamic vision sensing (DVS), which has increased dynamic range and reduced redundancy of information in controlled light environments such as noble element TPCs. DVS designs have demonstrated low power consumption as well as low latency \cite{MOEYS2017}.

The second front-end that was investigated is a charge replenishment architecture. This front-end works on the principle of detecting accumulated charge and is the focal point of this article.

Dynamic Vision Investigation
Dynamic vision sensing is investigated in the context of sensing the rate of change of charge, rather than accumulated charge. A transimpedance amplifier drives a switched capacitor differentiator, followed by a set of comparators for discrimination between positive or negative changes at the pixel.

%The minimum current detected, i_{min}, can be set by the threshold of the comparators by calculating the gain of the preamplifier and the gain of the charge sensitive amplifier:

$\%\Delta V_{threshold} = (-\frac{C_i}{C_f})(i_{min}R_f)$

It was concluded that this front-end was particularly attractive for photon detection within the Q-Pix array. However, for charge detection, we focused on the charge replenishment scheme.

Charge Replenishment Evaluation The charge replenishment front-end consists of a preamplifier, comparator, digital feedback control, and a switched capacitor charge replenisher. Ultimately, the digital feedback control will also feed a time-to-digital converter (TDC). This is illustrated in the front-end block diagram in Fig.
reffig:qpix$_frontend.$

Preamplifier

A minimum detectable charge, Q_{min}, is chosen such that a comparator trigger will be generated and time-stamped by the TDC. This triggering event will subsequently controls the replenishment of the pixel charge. This causes the eventual de-triggering of the comparator in order to reset the replenishing capacitor, $C_{replenish}$, and effectively resetting the front-end.

The preamplifier is configured as an integrating amplifier. We define ΔQ_{pix} as the change in charge at the pixel. The voltage at the output of the integrating preamplifier is given as:

$\Delta V_{integrator} = (-\frac{1}{C_f})(\Delta Q_{pix})$

Comparator and Charge Replenishment

The comparator threshold is determined by the minimum amount of detectable charge and the amplification of the integrating preamplifier. We define the threshold of the comparator to be when ΔQ_{pix} reaches Q_{min}:

$\Delta V_{threshold} = (-\frac{1}{C_f})(Q_{min})$

We define two modes of operation with respect to the feedback control.

• Accumulation mode • Replenishment mode

When the control block is in the accumulation mode, the switched capacitor is said to be accumulating charge. This charge can be calculated and should be equal to the minimum detectable charge Q_{min}.

$Q_{accumulate} = C_{replenish}(V_{accumulate} - V_{accumulate,ref})$

It is worth noting that this implementation has the added benefit of controlling whether to accumulate holes or electrons by simply calibrating $V_{accumulate}$. The voltage $V_{accumulate,ref}$ is a reference voltage that should be equal to the quiescent voltage of the integrating preamplifier for proper operation.

When the control block is in the replenishment mode, the charge that is accumulated during the accumulation mode is now deposited onto the pixel thereby replenishing the charge that was detected.

Conclusions

Simulation results of the charge replenishment front-end can be seen in Fig.
reffig:rtd$_patterns.Thisincludesthegenerationofreset-time-delays(RTDs)andthesignalreconstruction.$

A power consumption summary of the charge replenishment front-end can be seen in Table reftab:performance. The ENC was simulated to be approximately $385e^-$ at the integrator output when operating at $27°C$. The ENC is projected to be approximately $50e^-$ at the integrator output when operating at $-189°C$. This investigation demonstrates a promising path forward towards a scalable pixellated front-end architecture in a 65nm CMOS technology.

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