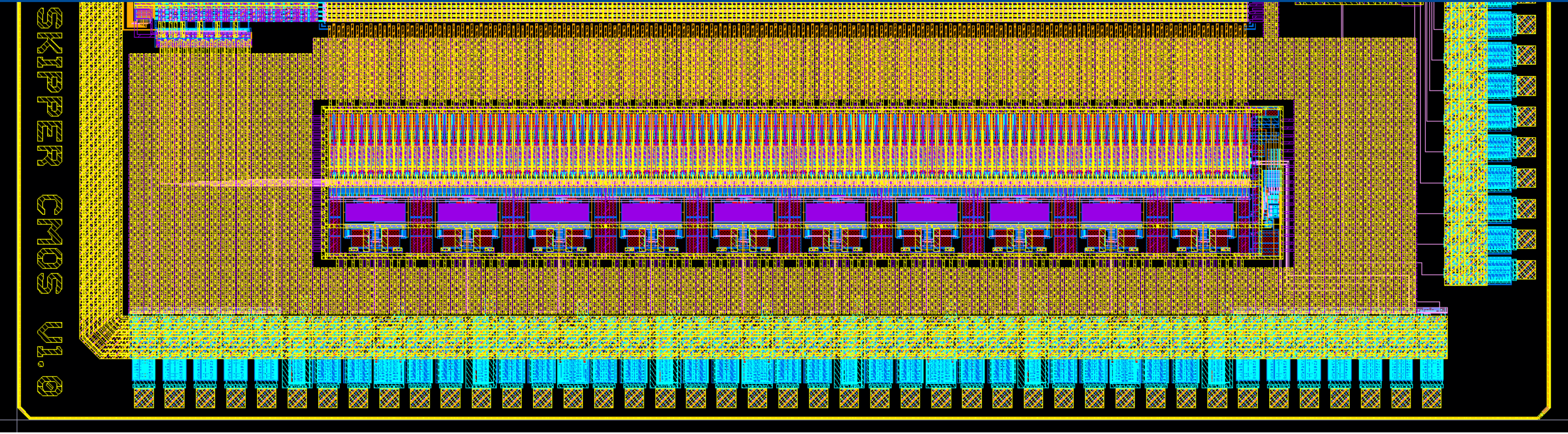


Skipper CCD-in-CMOS Sensor Readout Co-Design

(FNAL) Benjamin Parpillon, Honghzi Sun, Shaorui Li, Juan Estrada, Farah Fahim
(SLAC) Lorenzo Rota, Aseem Gupta, Angelo Dragone, Christopher Kenney, Julie Segal
(Centro Atomico Bariloche) Miguel Sofo Haro, Fabricio Alcade
(Tower Semiconductor) Adi Birman, Amos Fenigstein

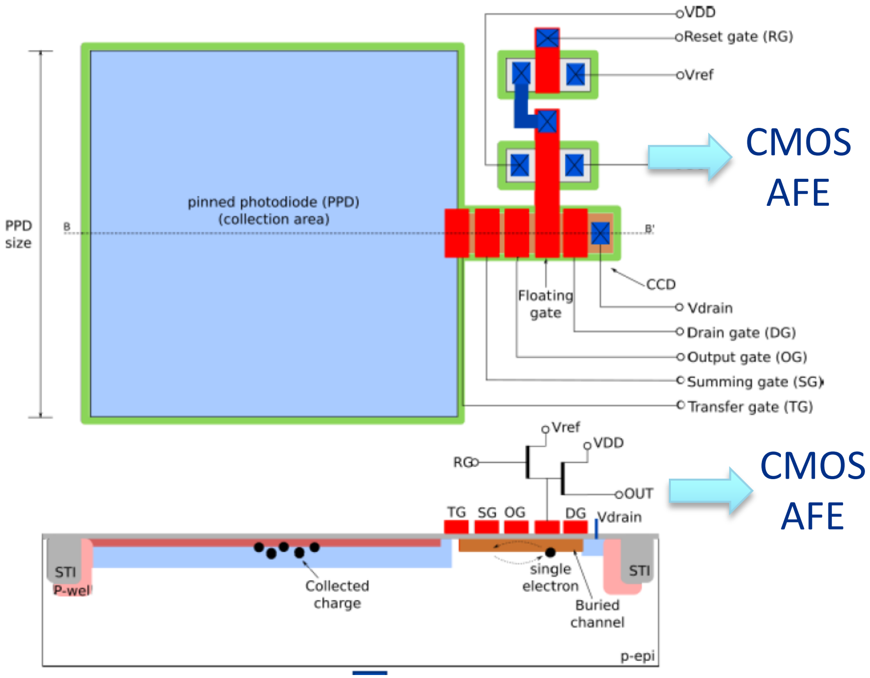
CPAD 2022

Background

In a nutshell

- **Project**: Skipper CCD in CMOS Sensor with **Non-Destructive Readout** Co-Design
- **Goal**: Design and Fabricate **Single-Photon** Image Sensor Prototype
- **Innovation:**
  - **Sensor with Pinned PhotoDiode (PPD) for conversion**
    - ✓ Much higher Conversion Gain than CCD (100uV/e- vs 3uV/e-)
    - ✓ Low leakage
    - ✓ Lower noise per measurement than CCD
  - **Skipper CCD for charge manipulation**
    - ✓ High charge transfer efficiency
    - ✓ Enables Non-Destructive Readout (NDR) capability
    - ✓ Enables noise averaging feature
  - **Co-integrated CMOS process**
    - ✓ Readout **parallelization** capabilities
    - ✓ Much **faster** readout time than CCD*
    - ✓ **Finer** feature size
    - ✓ **High-Volume** capability

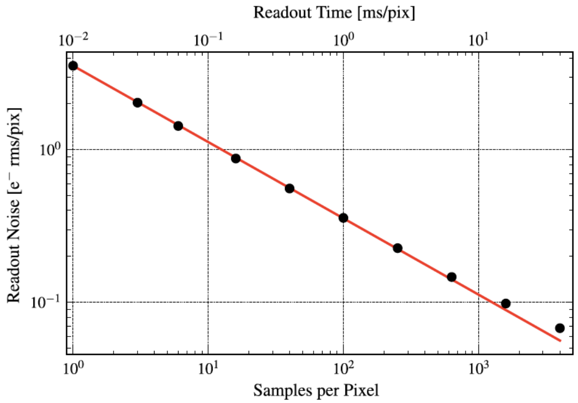
Proposed Pixel: MAPS with CCD

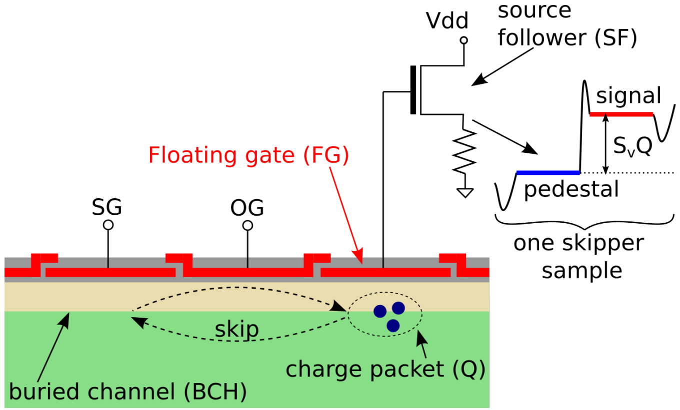


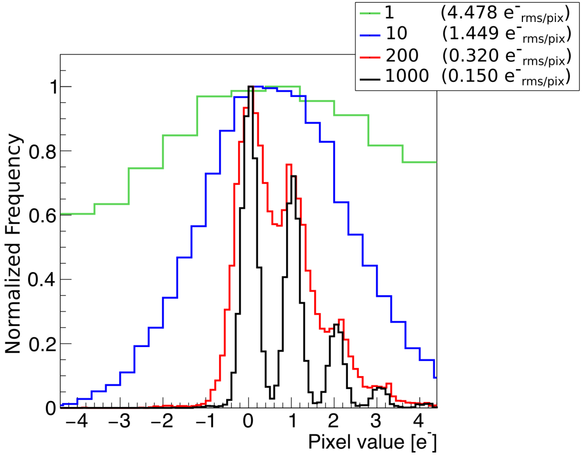
Ref: Stefanov, K. D. (2020). Simulations and Design of a Single-Photon CMOS Imaging Pixel Using Multiple Non-Destructive Signal Sampling. Sensors , 20(7)

What is Skipper CCD?

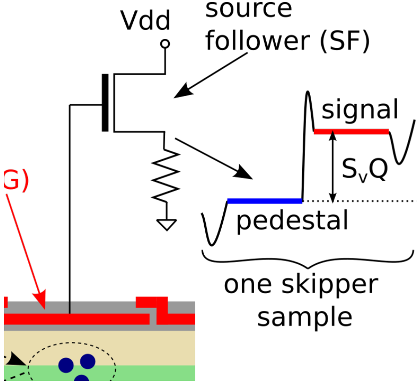
- Originally developed for CCD readout technique
- Allow to perform Non-Destructive Readout of the charge
- Signal is correlated, noise is not; improve SNR by $\sqrt{N}$
- Integrated noise < 1 e- is possible!
  - ➔ Allow to do single photon imaging

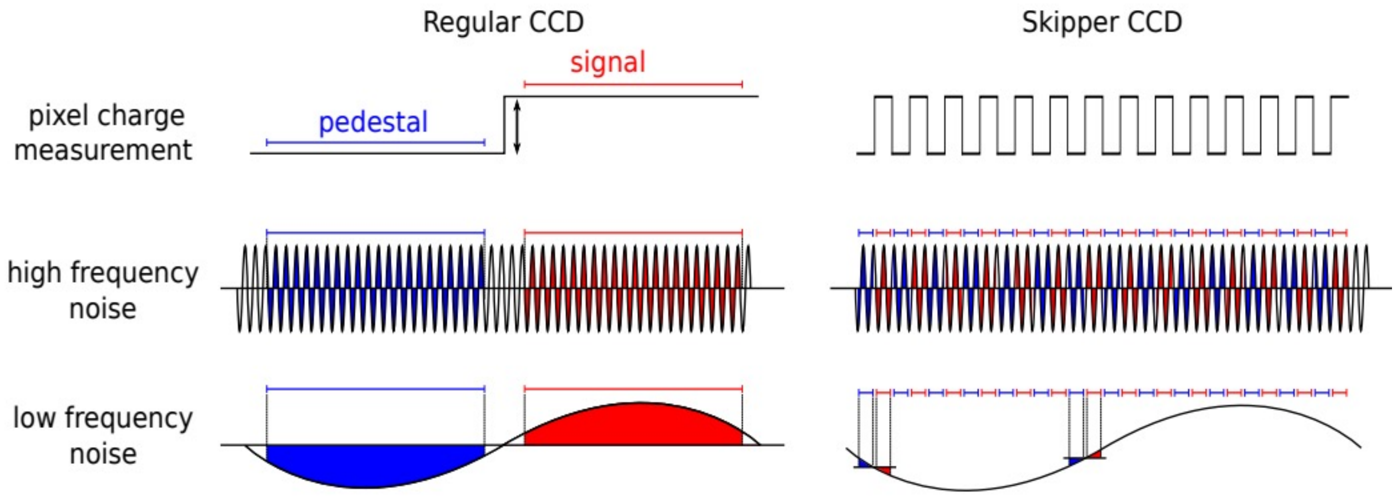






Skipping versus Correlated Multiple Sampling





Final pixel value is *pix = avg(signal – pedestal)*, noise scales as √*#samples*

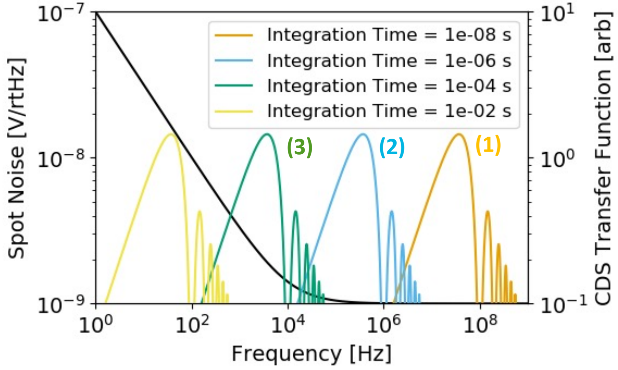
Skipper readout is NOT the same as Correlated Multiple Sampling (CMS)

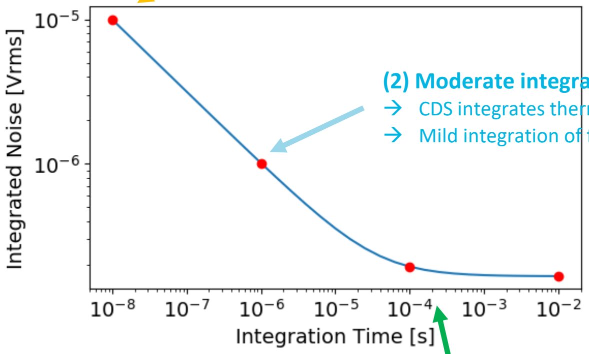
Thanks to the non-destructive read-out, pedestal and signal are sampled close to each other → filter low frequency noise too

Ref: https://indico.cern.ch/event/782953/contributions/3515721/attachments/1889519/3115804/dpf_instrumentation_eca.pdf

Limit of Correlated Double Sampling

CDS





(1) Fast integration time:

→ CDS Integrates all the thermal noise over large bandwidth

(2) Moderate integration time:

→ CDS integrates thermal noise over smaller bandwidth

→ Mild integration of flicker noise

(3) Slow integration time:

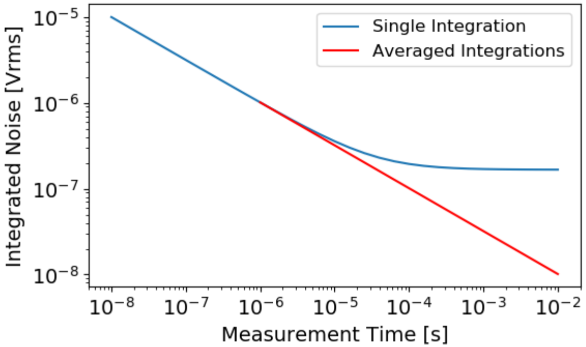
→ CDS integrates only flicker noise

→ The CDS bandwidth times 1/f noise is constant

→ We have reached the **limit** of the CDS

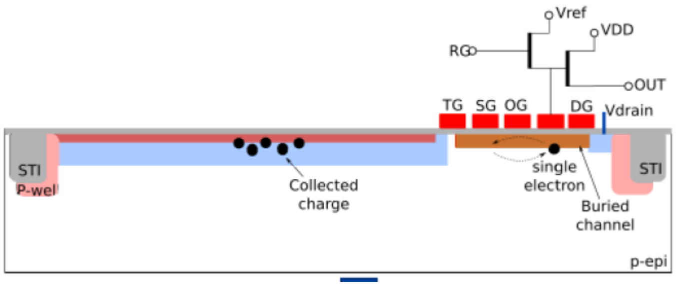
CDS + Skipper

Skipper doesn't have this limitation



Ref: Troy England

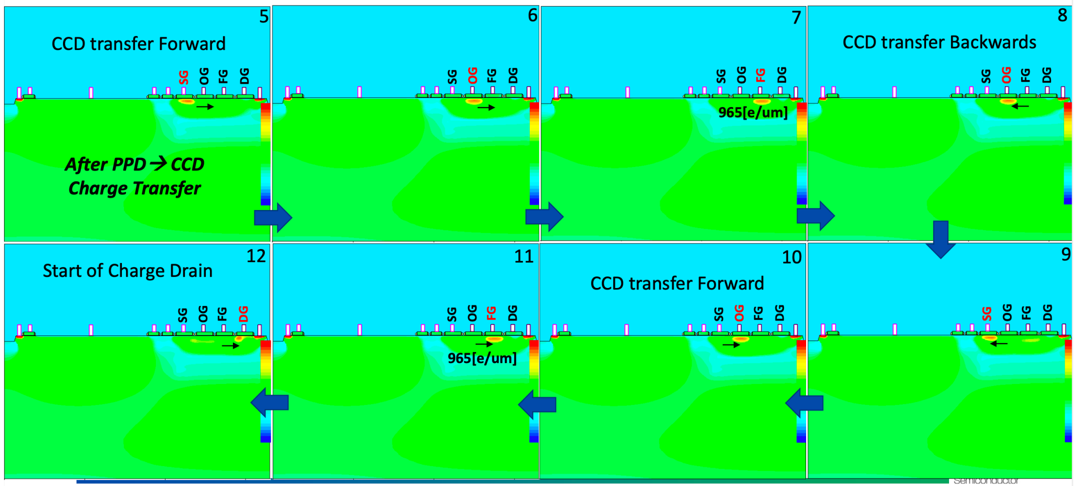
Non-Destructive Readout Operation



Operation:

1. Reset of the PPD and CCD
2. PPD charge integration
3. Pulse Transfer Gate (TG)

5. Transfer forward to the Summing Gate (SG)
6. Transfer forward to the Output Gate (OG)
7. Transfer forward to the Floating Gate (FG) for first NDR
8. Transfer back to OG
9. Transfer back to SG
10. Transfer forward to OG
11. Transfer forward to FG for second NDR
12. Transfer to the Drain Gain (DG) to flush the charges



$$ENC_{final} = \frac{ENC_{initial}}{\sqrt{n}}$$

Prototype Overview

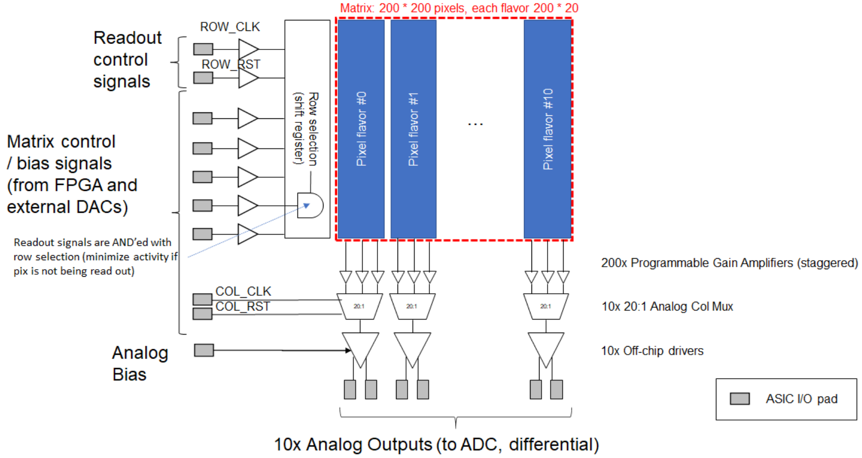
Main objectives:

1. Demonstrate low noise capabilities for a single measurement (< 2e- RMS including pixel and AFE)
2. Demonstrate **photon counting** with **micro-second scale readout time** capabilities
3. Fabricate and characterize pixel variations and AFE blocks:
   - → Identify pixel variant and split with best performance (Quantum Efficiency, Conversion Gain, Transfer efficiency)
   - → Identify AFE structures with best performance (noise, power, speed)
   - → Characterize and improve spice modeling of pixel

Physics Applications

1. Low mass dark matter searches
2. Soft x-ray spectroscopy
3. Astrophysics: deep measurements of dark energy and dark matter signatures
4. Single-photon quantum sensing

Architecture: 20 variants – 5 splits



Collaboration Landscape:

1. Tower Semi: CMOS and Pixel Technology
2. Centro Atómico Bariloche: Pixel and Matrix Implemention
3. Fermilab: Front End Readout Design
4. SLAC: Digital blocks and top-level implementation

AFE Specification

- Achieve single-electron CMOS Imaging
- High dynamic range
- Microsecond readout time

Pixel

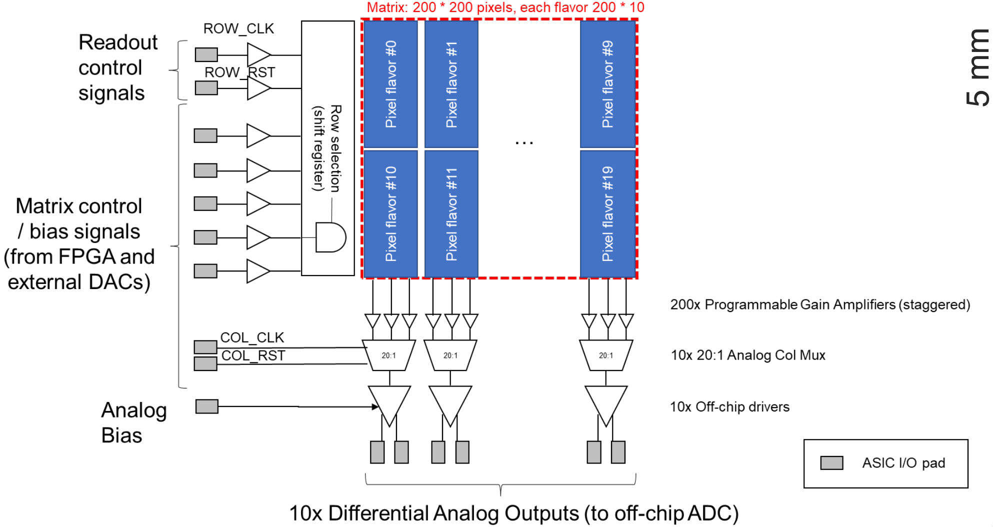
Variable	Value	Unit
Conversion Gain	115	µV/e^-
Dynamic range	11000	e^-
White Noise	<10e-9	V/√Hz
Fnc	>100	MHz
ENC (single Meas)	<1	e-

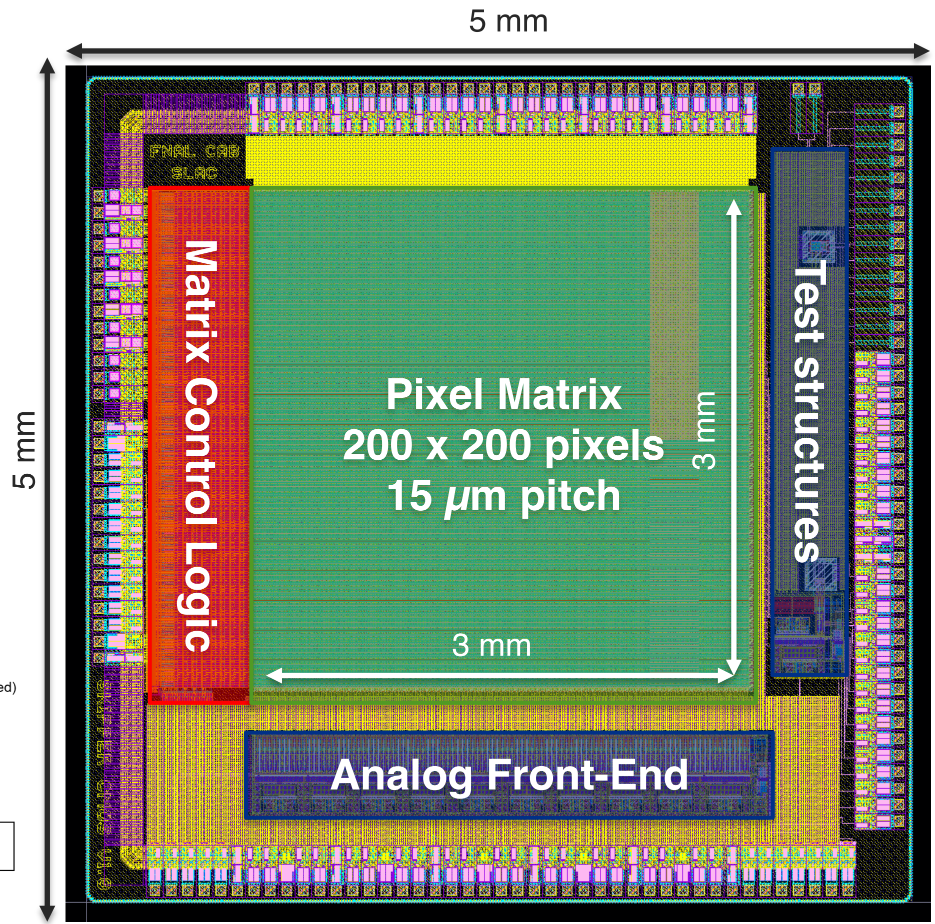
Analog Readout

Variable	Min	Target	Max	Unit
Input Amplitude	1		11000	e^-
Input Amplitude	0.125		1375	mV
PGA gain (trimmable: 4-bit)	1		64	V/V
measurement time	1	10		µs
Temperature	-40	27		C
ENC (single measurement)		<2		e-

Top-Level Overview

- MPW with front-side illumination
- Size: 5x5 mm^2
- Active area: 3x3 mm^2
- Pixel design compatible with Back-Side Illumination (BSI, not for this run)

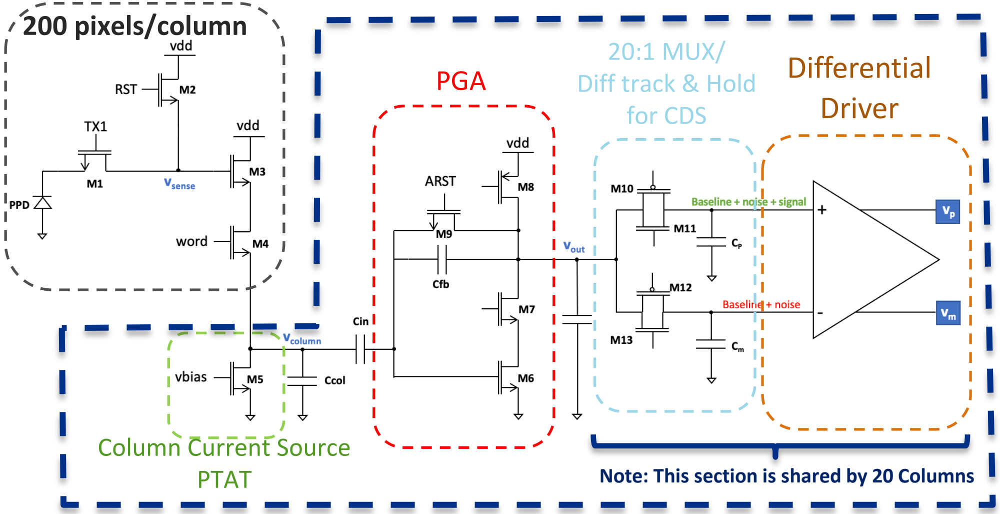




Top-Level Overview: why a rolling-shutter architecture

- **Goal of 1st prototype:** demonstrate low-noise readout based on Skipper operation
- Implemented **rolling-shutter** architecture:
  - Control signals are common to all pixels in a row
  - Only one row is active, readout signals are gated in non-active rows (pixel under RST)
  - Avoid redundant charge transfer across PD/gates in non-active rows
  - Reduce digital activity, minimize noise coupling
- Read-out is not fully-parallel: 20 columns are multiplexed to 1 readout channel
  → In non-active columns, redundant charge transfer is still happening

AFE Single Column Readout Chain Overview



To off-chip test board

Will perform readout, CDS and skipper operations

Spec	min	typ	max	unit	condition
IDC		24		mA	Nominal corner
Power		120		mW	Nominal corner
Output referred noise		188		uV	Noise tran, 0e-, cds=4pF, gain=1
ENC		1.6		e-	Noise tran, 0e-, cds=4pF, gain=1
ENC		<1		e-	Noise tran, 0e-, cds=4pF, gain=35
linearity: 1-R^2		9.8E-08		NA	gain =1, from 0e- to 11Ke-
Dynamic Range	1		11000	e-	Gain =1 and 2
Gain	1		35	V/V	

Architecture Selected:

1. Small, Fast, Low noise
2. Gain tunable with Cin/Cfb capacitance ratio
   → High gain desirable in low light condition to improve SNR
3. Skipper operation effective up to the track & hold
4. Other noise sources (ie: KTC noise from track & hold, or sources from differential driver) are made insignificant due to the PGA gain

Single-photon Imaging – Peter Seitz/Boyd Fowler

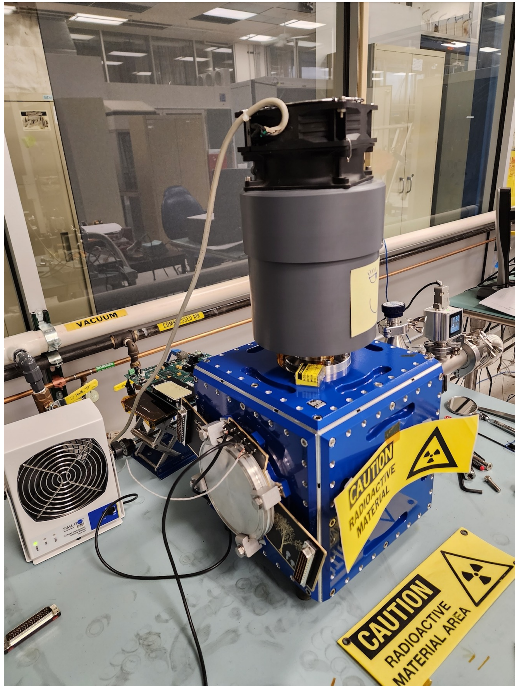
Springer Series in Optical Science 160

Ongoing Test Effort

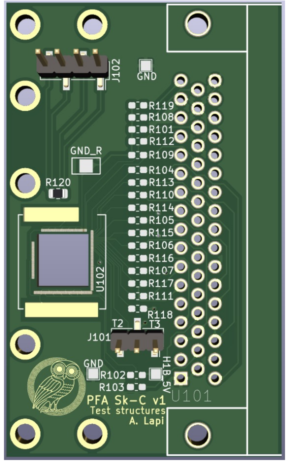
Silicon is back and test just started

1. Test board is being fabricated
2. Expecting preliminary result in the next couple of months

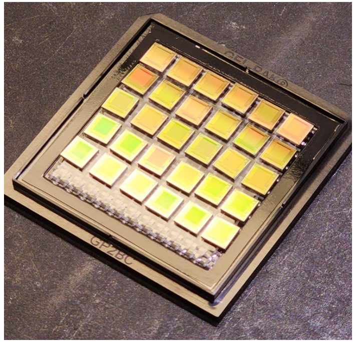
Test setup



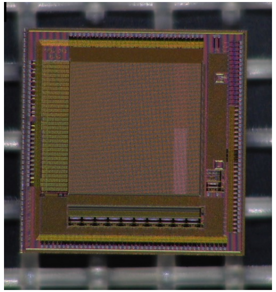
Test Board



Chip Samples:
20 variants – 5 split



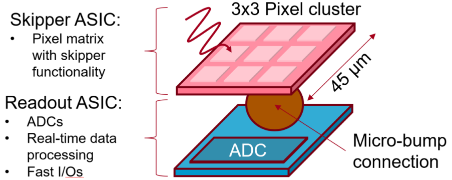
Closeup



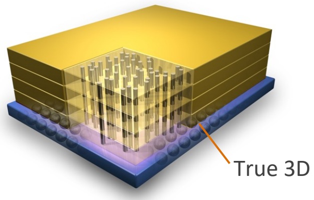
Conclusion

<u>If our prototype is successful :</u>

- Upgrade the design and build a Single Photon CIS circuit:
  1. Leveraging accurate models and best pixel variation
  2. Leveraging best analog front-end architecture and IP blocks
  3. Implement new features (e.g: on the fly gain selection)



- Hybridize the fabrication (3D or bump bonding)
  1. Pixel on its own tier : Improved detection area
  2. Highly parallel architecture -> implementing amplification and ADC every 3x3 pixels could enable 1Kfps readout speed capabilities
  3. Will use best pixel for full reticle chip: Sprocket readout chip



Synergetic Effort to Develop Skipper Devices:
and associated Fermilab talks at CPAD 2022

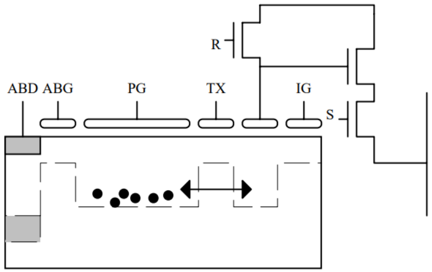
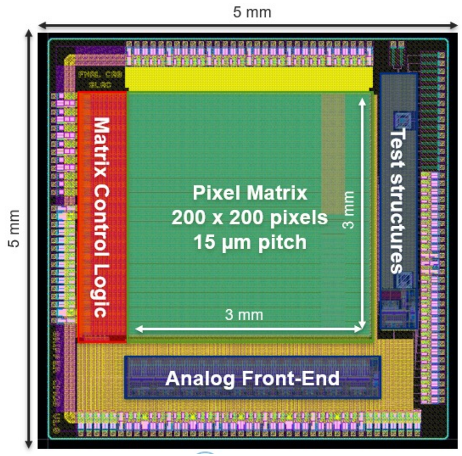


Fig. 10. JPL CMOS-compatible lateral APS.

Skipper-CCD

↓

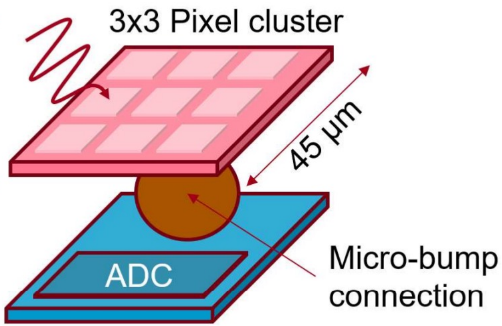
Talk by D. Braga (9:30a Thu)



Skipper-CCD-in-CMOS

↓

This talk!



Hybrid Readout for Skipper-CCD-in-CMOS

↓

Talk by A. Quinn (8:50a Thu)

CNEA SLAC NATIONAL ACCELERATOR LABORATORY Fermilab

Thank you!