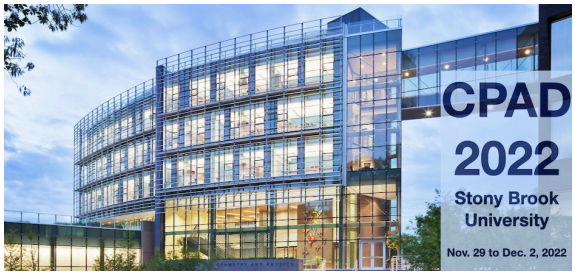

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Design of a skipper CCD-in-CMOS active pixel sensor

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The Skipper-in-CMOS Application Specific Integrated Circuit (ASIC) is an image sensor prototype fabricated in a 180nm CMOS imaging process and intended for a wide range of scientific applications such as low-mass dark matter searches, deep measurement of dark energy and dark matter signatures or single-photon quantum sensing.

The goal of this prototype is to integrate the non-destructive readout capability of skipper Charge Coupled Devices (CCDs) with a high conversion gain pinned photodiode on a CMOS imaging process, while taking advantage of in-pixel signal processing.
Our prototype integrates a 200x200 pixel matrix with 18 different CCD-in-CMOS pixel structures, connected to 10 analog readout channels. The pixel matrix is readout in a rolling shutter scheme. The different pixel designs will allow the study of several process parameters like PPD to CCD charge transfer, conversion gain, CCD charge transfer and full well capacity.
Each readout channel consists of a pre-amplifier, a 20:1 analog MUX with differential track / hold capabilities and a differential buffer to drive an off-chip ADC. The channels have 4-bit gain settings, 2-bit trimmable bandwidth. The simulated equivalent noise charge for a single readout is 1.6e-. Sub-electron noise can be achieved by reading out multiple samples of the same charge packet using the skipper technique and averaging the output signal. A high-speed readout with a minimum integration time of 250ns is possible and the unity-gain linear dynamic range is 11,000e-.

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