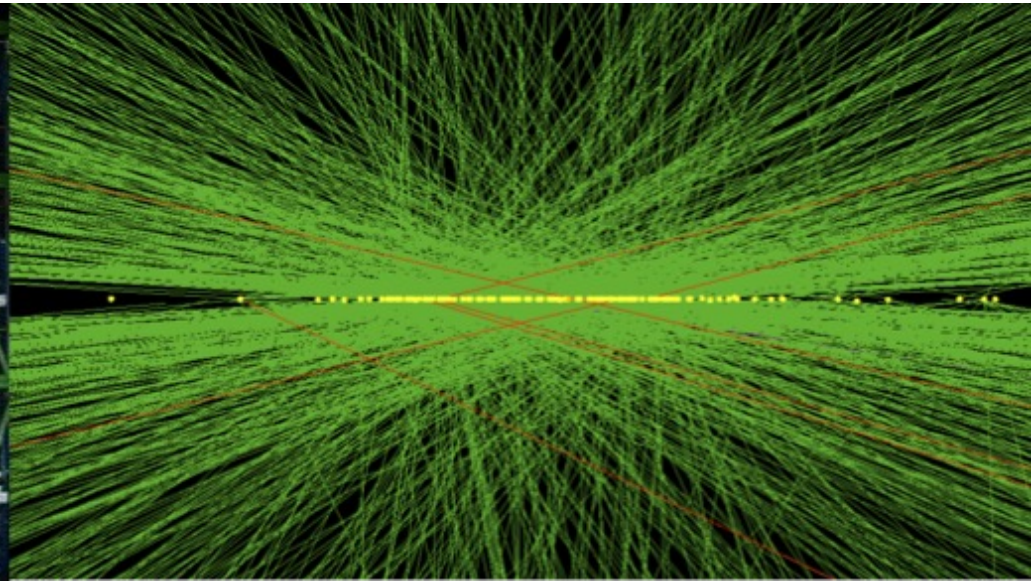
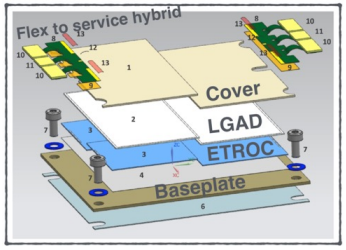
Precision timing ASIC (ETROC) development for LGAD-based detector for CMS upgrade,
and future prospect and challenges

Ted Liu (Fermilab),

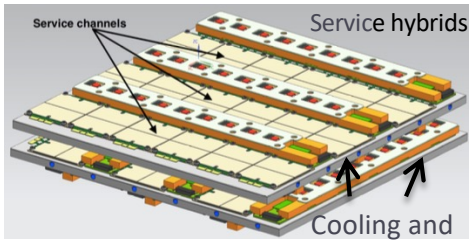
Dec 1st, 2022, CPAD meeting

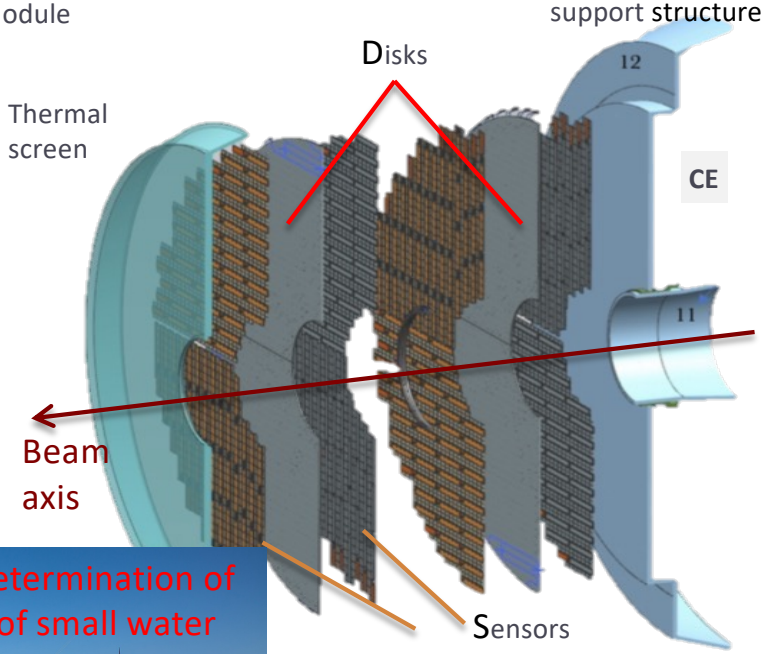


ETL precision timing *challenges*



Module





- Low Gain Avalanche Detectors (LGADs)
  - Basic unit:
    - 2x2 cm^2 LGAD bump-bonded to ETROC ASIC mounted on two sides of cooling plates
  - Two layers/disks per endcap (~2 hits per track)
  - $1.6 < |\eta| < 3.0$, surface ~14 m^2; ~9 M channels
  - Nominal fluence: ***1.7x10^{15} n$_{eq}$/cm^2*** (@ 3000 fb^{-1})
- LGAD gain modest: 10-30
  - LGAD Landau contribution: ~ 30ps
  - Front-end contribution should be kept < 40ps
  - < 50ps per hit, or 35ps per track (with 2 hits)
- ***Extract precision timing from***

  Small LGAD signal (typical 10-20 fC)
  - ***With low power: < 4mW/channel on average***

Challenges:

Low power and fast/precision timing,
Precision clock distribution,
Minimizing readout digital activities

Design considerations for precision timing detector

- System power and cooling constraint and how it influences ASIC design
- Design methodology to optimize front-end from system point of view
- Single layer detector vs multi-layer (ETL design: 1 layer →2 layer)
- TDC design choice: needs ultra low power → new design
- Precision clock distribution considerations: from system to detector, to chip, to pixel and to each TDC delay unit (using H-tree approach)
- Design to enhance physics reach:
  - such as detection/trigger for long live particles, with wide TDC window
- Design for monitoring and calibration considerations: waveform sampler
- Time-frame of ASIC development: "several mini-ASICs vs. single full ASIC"
- …

Will not have time to get into these in this talk ….

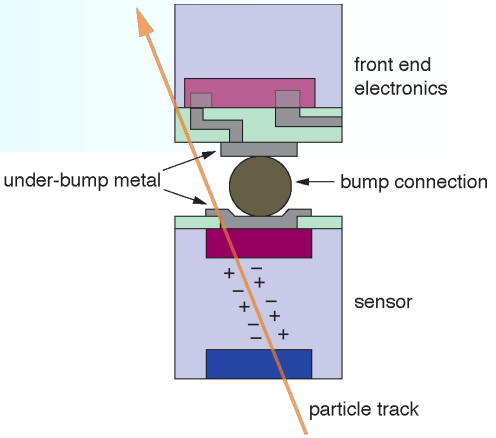
Proper System Design is the Key to the success of any challenging ASIC project

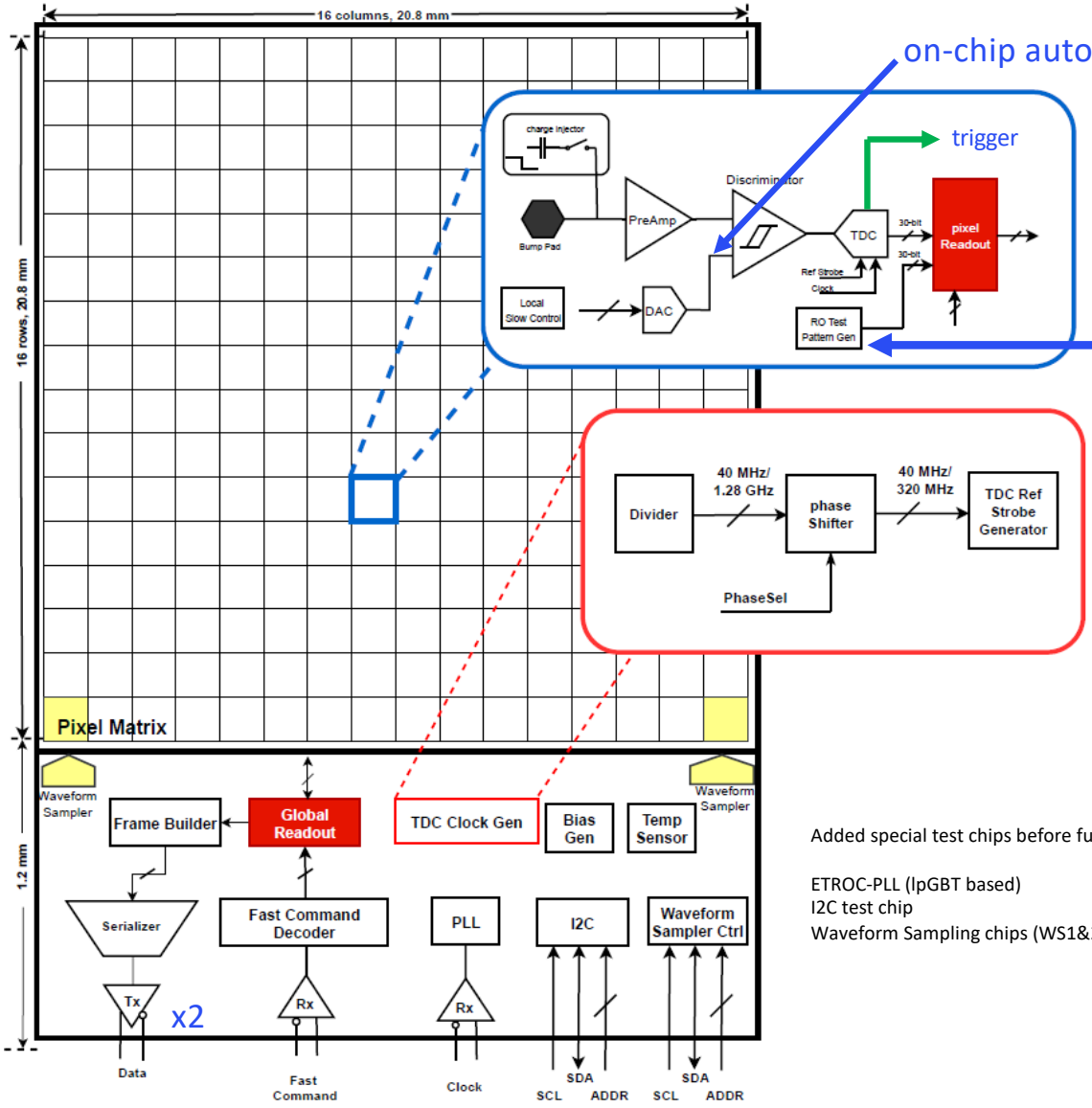
A good design is a compromise between system design and ASIC design

The approach: "ASIC == A System design Including a Chip"

ETROC Design: from TDR to now

Blue: not described in MTD TDR





on-chip auto threshold calibration

Self-test capability (for ***design verification*** & chip and system level testing with backend)

- Measuring arrival time of LGAD signal
  - Front-end: PA + Discriminator + TDC
  - L1 latency circular buffer
  - L1A-driven readout with zero suppression
  - A coarse map of ***delayed*** hits for L1 trigger
- Interface of ETROC2
  - 40 MHz reference clock
  - I2C-based slow control
  - 320 Mbps fast control
  - Serial data link 320/640/1280 Mbps
- Waveform Sampling of preamp output (only 1 pixel)
  - For test & monitoring purpose

2.5 V for efuse (will require 2.5V once)

Added special test chips before full-size ETROC2:

ETROC-PLL (lpGBT based)
I2C test chip
Waveform Sampling chips (WS1&2)

ETROC2 is designed in such a way as if it is the final design for full functionalities

(with extra flexibilities for performance study purpose)

For technical details, please see ETROC papers and recent talks.
This talk only has few highlights, then on future prospect and challenges

Characterization of the CMS Endcap Timing Layer readout chip prototype with charge injection

https://iopscience.iop.org/article/10.1088/1748-0221/16/06/P06038

The Analog Front-end for the LGAD Based Precision Timing Application in CMS ETL

https://arxiv.org/abs/2012.14526

In-pixel automatic threshold calibration for the CMS Endcap Timing Layer readout chip

https://iopscience.iop.org/article/10.1088/1748-0221/16/09/T09006

FERMILAB-CONF-20-549-E

A New Scheme of Redundant Timing Crosschecking for Frontend Systems

https://ieeexplore.ieee.org/document/9447027

A 2.56 GS/s 12-bit 8x-Interleaved ADC with 156.6 dB FoM_S in 65 nm CMOS

IEEE Transactions on Very Large Scale Integration Systems (TVLSI), Volume: 30, Issue: 2, Feb. 2022) Page(s): 123 – 133

1984 IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 68, NO. 8, AUGUST 2021

A Low-Power Time-to-Digital Converter for the CMS Endcap Timing Layer (ETL) Upgrade

https://ieeexplore.ieee.org/document/9446843

2022 TWEPP talks related to ETROC:

From ETROC1 to ETROC2:

https://indico.cern.ch/event/1127562/contributions/4904521/ (***TWEPP 2022***, Tuesday)

ETROC Emulator:

https://indico.cern.ch/event/1127562/contributions/4904781/ (***TWEPP 2022***, Wed)

ETROC Waveform Sampler:

https://indico.cern.ch/event/1127562/contributions/4904540/ (***TWEPP 2022***, Thursday)

TDC with Uncontrolled Delay lines: calibration approach and method

https://indico.cern.ch/event/1127562/contributions/4904530/ (***TWEPP 2022***, Thursday)

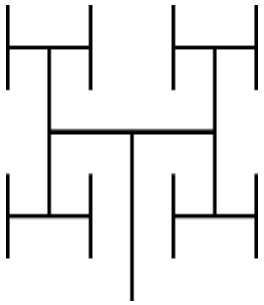
ETROC Development Strategy & Schedule

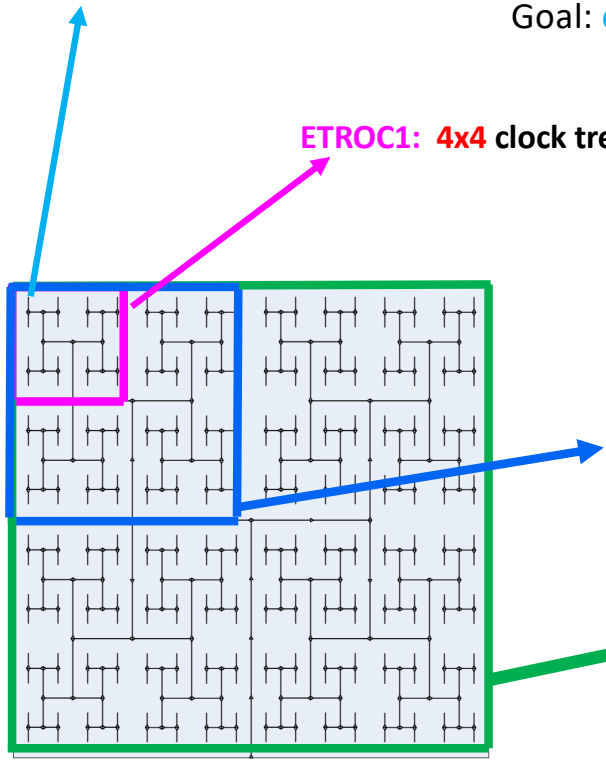
ETROC0: **1x1 pixel channel with preamp + discriminator (submitted Dec 2018)**

Goal: core front-end analog performance

ETROC1: **4x4 clock tree, preamp + discriminator + TDC.** **(Submitted Aug 2019)**

Goal: full chain front-end, 4x4 clock tree





16 x 16 clock H-Tree

Added here a few test chips to prototype all other key building blocks

ETROC2: 8x8 → 16x16, *full functionality and full size* **(Oct 2022)**

Goal: first full size full functionality prototype

ETROC3: **16x16 (full size & functionality)** **(Q1 2024)**

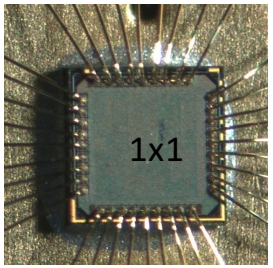
Goal: intended as final design

ETROC prototyping history

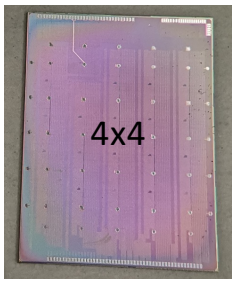
Sept 2018 | Dec 2018 | May 2019 | Aug 2019 | March 2020 | May 2020 | July 2021 | Sept 2021 ...

Project started

ETROC0 submitted



ETROC1 submitted

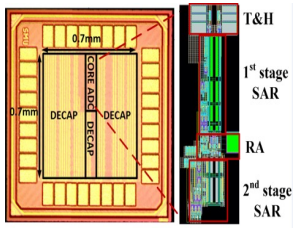


Covid

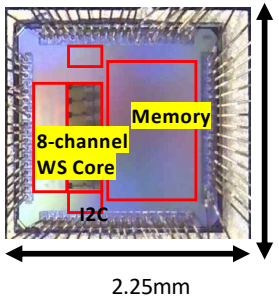
ETROC2: 8x8 → 16x16

Decision to go for full size full functionality ETROC2, Delay submission and add few test chips …

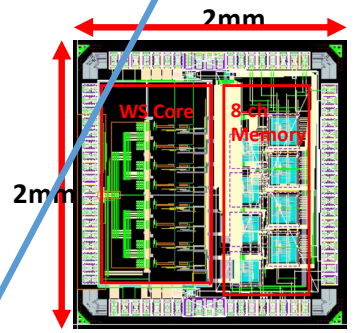
Single channel ADC submitted



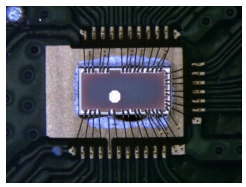
8-channel ADC Waveform Sampler (WS1) submitted



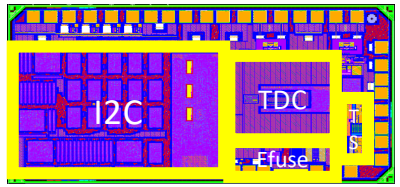
Rad-hard version of Waveform Sampler (WS2) submitted



ETROC-PLL mini ASIC submitted



I2C Test chip submitted



Total of 7 testing chips so far, all successful

All analog blocks have been silicon proven in test chips
ETROC2 FPGA emulator: has verified digital readout and system interfaces

Now ETROC2 is submitted! (Oct 21, 2022)

Design team: FNAL/SMU/LBNL/UCSB
Testing team: FNAL/SMU/UIC/UCSB with students from KSU/CNU

ETROC Overall Status

ASIC design: FNAL/SMU/LBNL
Testing: FNAL/SMU/UIC/KSU/KNU/CNU
& in collaboration with lpGBT team,
with help from:
ETROC God Parent Committee
CERN ASIC Support & CHIPS for ETROC2,
Torino/UCSC groups (sensor),
and Barcelona group (bump bonding)

- ETROC0 (single channel, preamp + discriminator)
  - Charge injection/Cosmic/Laser done
  - TID test to 100Mrads done
  - Beam testing: ~30ps achieved in beam.
- ETROC1 (4x4), preamp + discriminator + new TDC
  - New TDC extensively tested: excellent performance and low power (<~6ps resolution)
  - Bare ETROC1 charge injection testing: excellent performance (~10ps resolution with charge injection)
  - ETROC1 and 5x5 LGAD sensor bump-bonded
    - ***Encountered noise related to 40MHz memory activity after bump bonding with sensor***
      - ***Noise source identified and understood, addressed in ETROC2 design***
    - ***Beam testing: results from beam telescope with LGAD at higher gain***
      - ***Obtained down to ~ 40ps per hit at system level in beam in 2021***
      - ***Second round of beam testing in 2022, results consistent***
  - *ETROC1 TID testing (to be done, delayed due to COVID)*
- Towards ETROC2 (16x16)
  - ETROC PLL mini-ASIC (with lpGBT PLL core)***: test results very good, including SEU***
  - Waveform Sampler prototypes and I2C test chip work well.
  - ETROC2 emulator (for pixel and global readout) works well
  - ***ETROC2 design submitted in Oct 2022***
- ***ETROC3: intended as final version, submission in 2024***

Due to limited time, this talk will only have few highlights

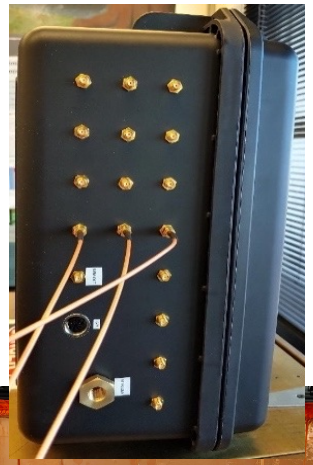
Dedicated Technical Reviews in the past (by God Parents and CERN CHIPS and ASIC Support):
Three God Parents reviews (2018-2021)
ETROC2 features review (Oct 2021)
ETROC2 pre-submission review (July 20th, 2022)
ETROC2 final submission review (Oct 7th, 2022)
ETROC2 final submission to IMEC (Oct 21, 2022)

The ETROC2 design has been extensively reviewed by experts

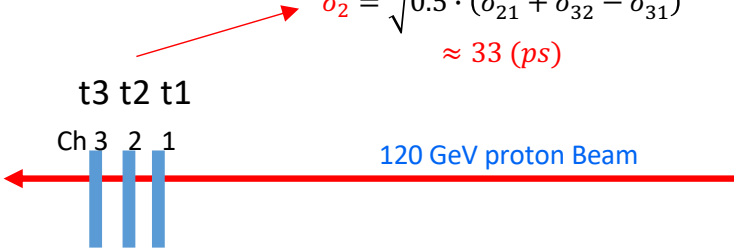
A simple ETROC0 Beam Telescope (with 3 HPK-ETROC0 boards)

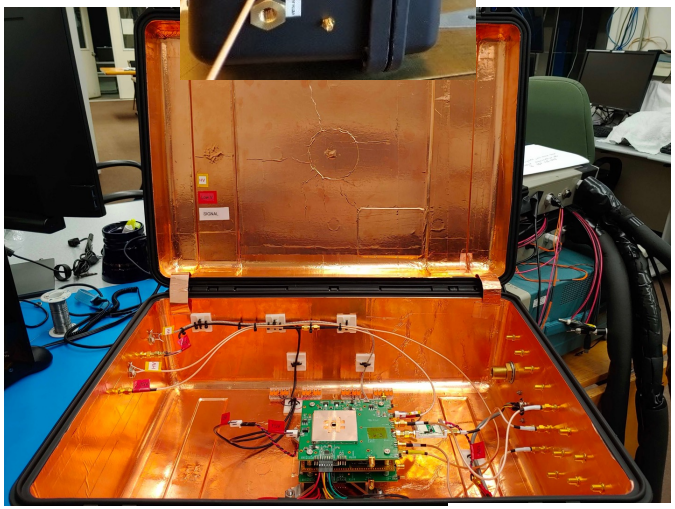
Jan-Feb 2020

Simple "suitcase" setup in parasitic mode running at FNAL MTest

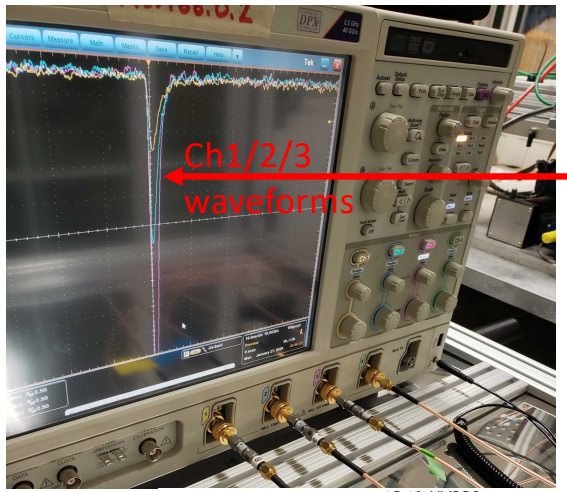


$$\sigma_2 = \sqrt{0.5 \cdot (\sigma_{21}^2 + \sigma_{32}^2 - \sigma_{31}^2)} \approx 33\ (ps)$$

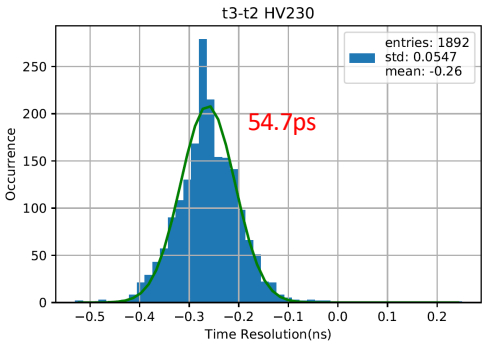


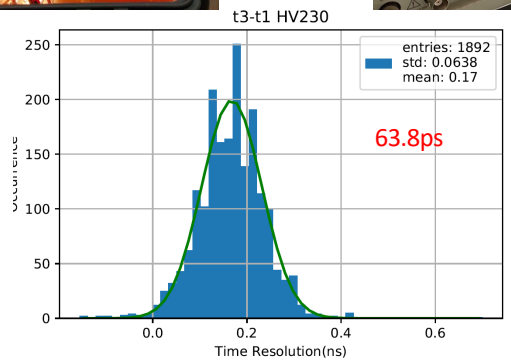


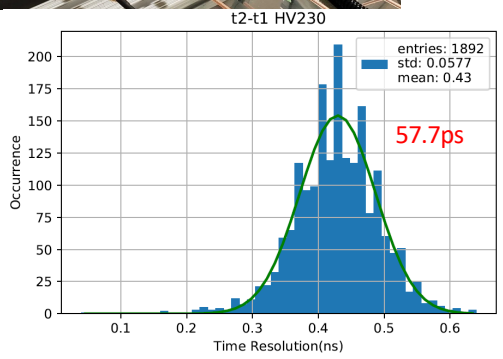
At room temperature



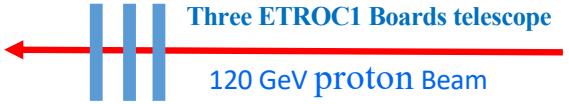
preamp waveform

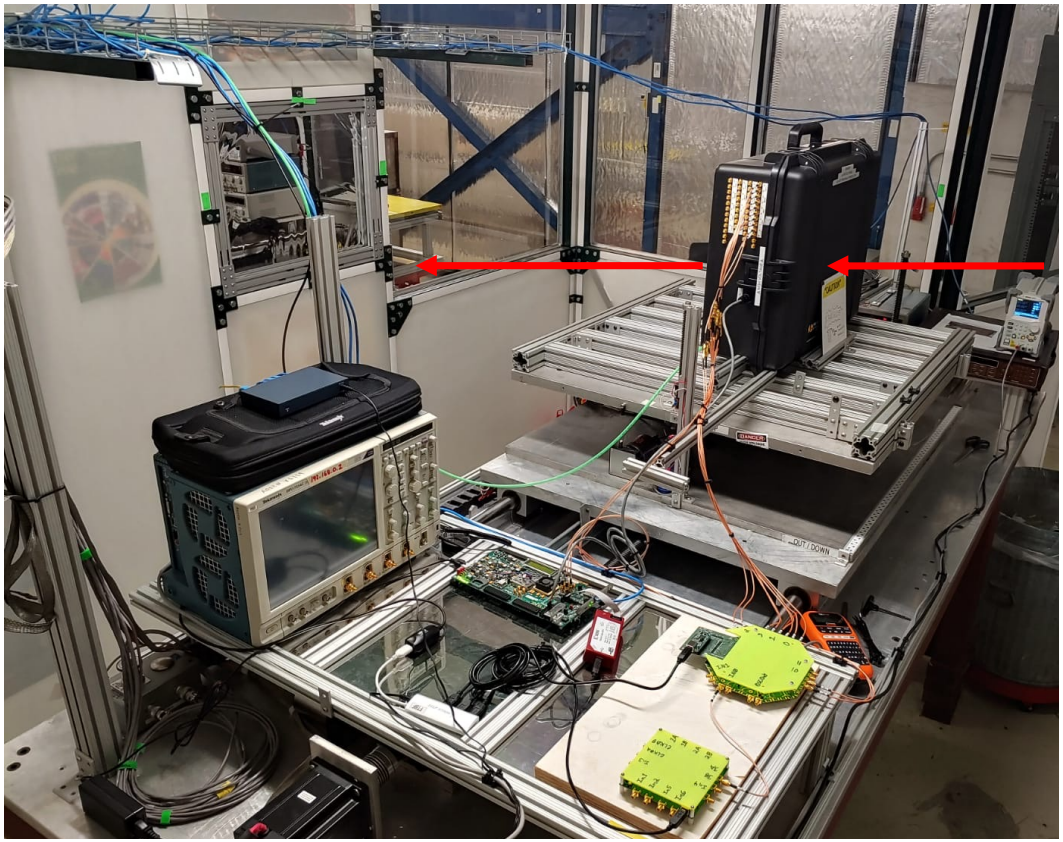


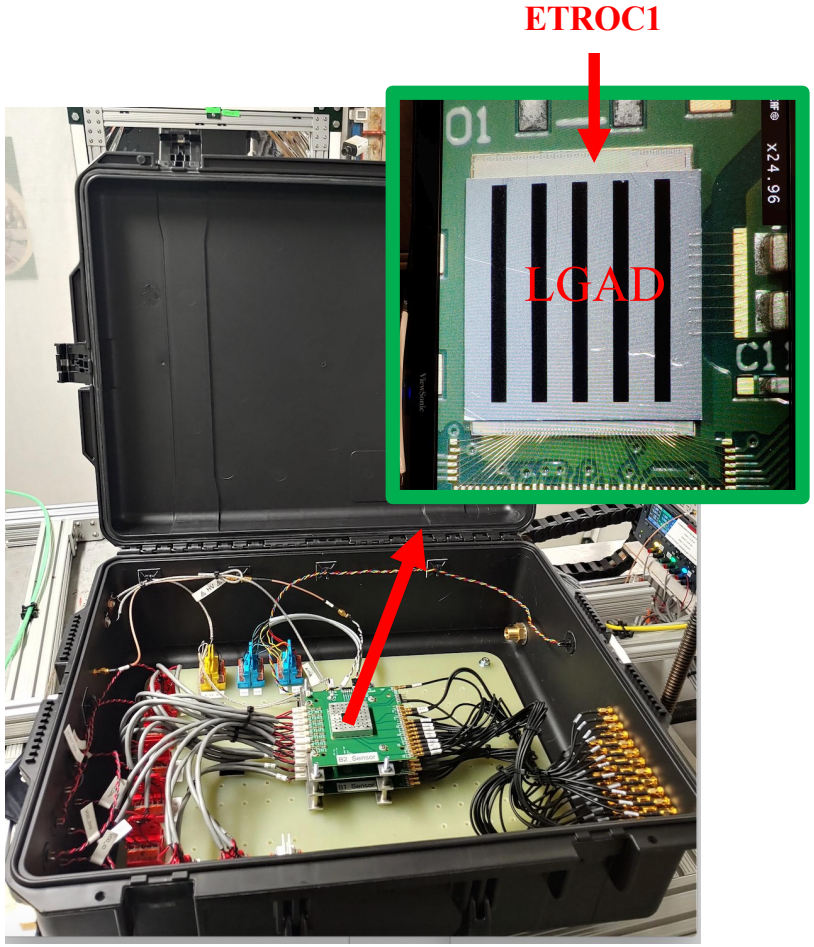




ETROC1 Beam Telescope @ FTBF



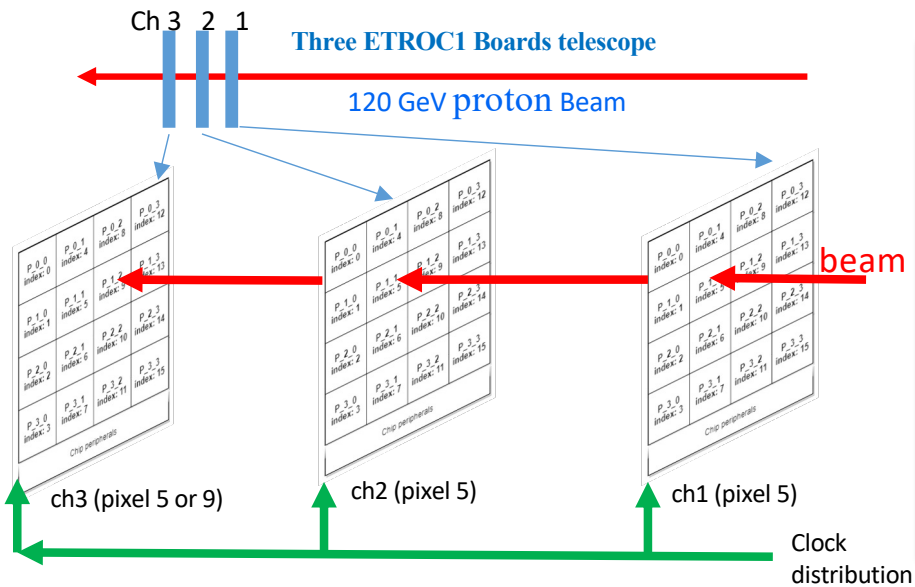




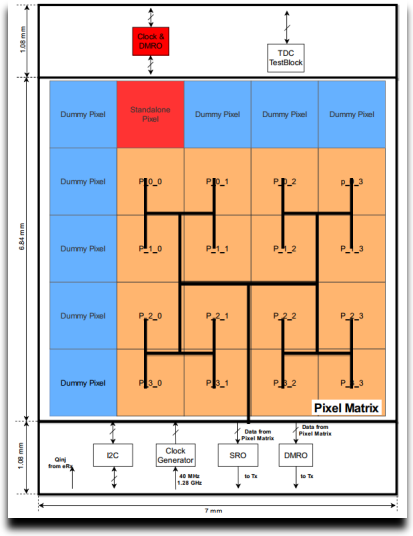
Precision timing full chain signal processing: preamp → discriminator → TDC (TOA/TOT)→ output with external and internal precision clock distributions

2021 vs 2022 Test Beam test results

- Testing team (UIC/SMU/FNAL + students from KSU/KNU/CNU)



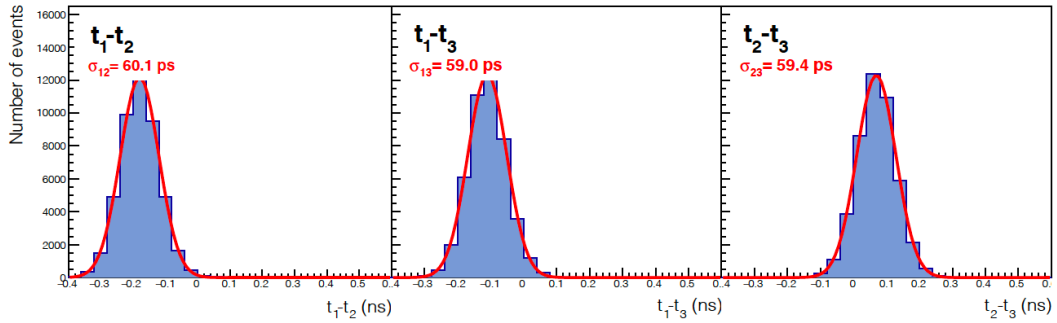
ETROC1 4x4 H-tree clock distribution within chip

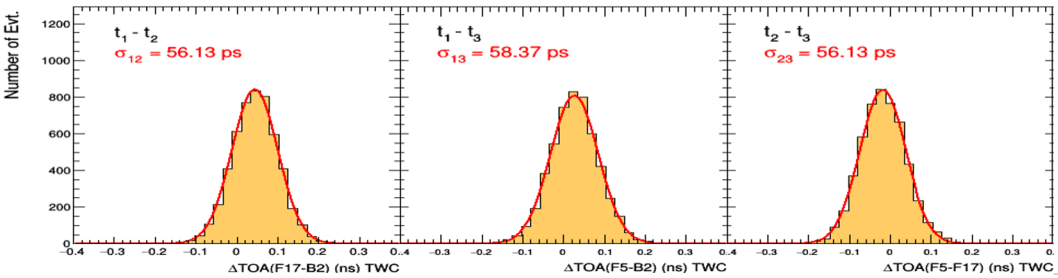


ETL Time resolution

		Simulation /expectation vs spec
LGAD+ preamp/discriminator + TDC bin	35 ps	
Time-walk correction residual	< 10 ps	
Internal clock distribution	< 10 ps	
System clock distribution	< 15 ps	
Per hit total time resolution	41 ps	50 ps
Per track (2 hits) total time resolution	29 ps	35 ps

(with LGAD HV=230V for all three channels)





The measured time resolution includes all four contributions in the table

Single-hit timing resolution (ps) with TWC:

$$\sigma_i = \sqrt{0.5 \cdot \left(\sigma_{ij}^2 + \sigma_{ik}^2 - \sigma_{jk}^2\right)}$$

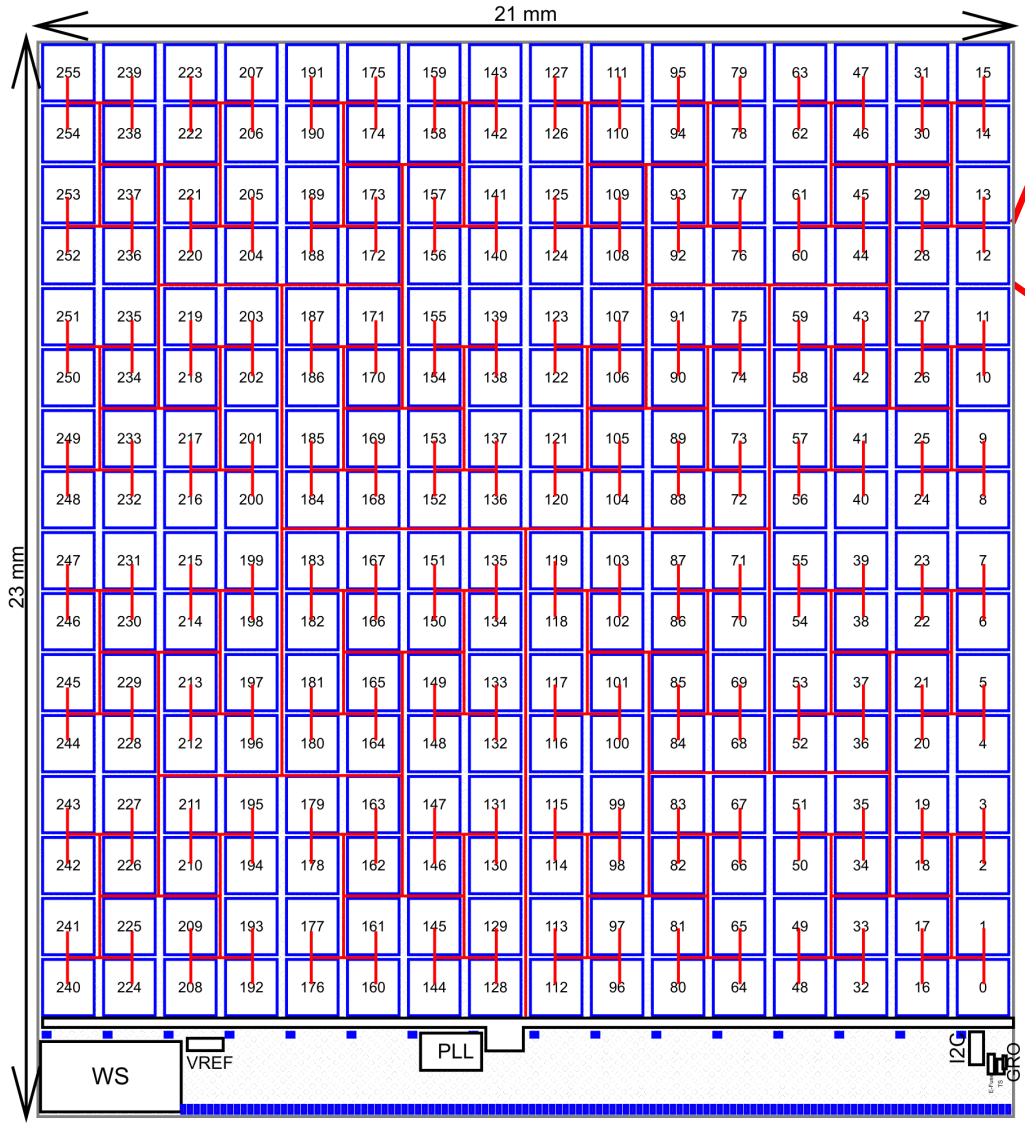
~ 42.0/42.7/41.3 ps (2021 beam test)

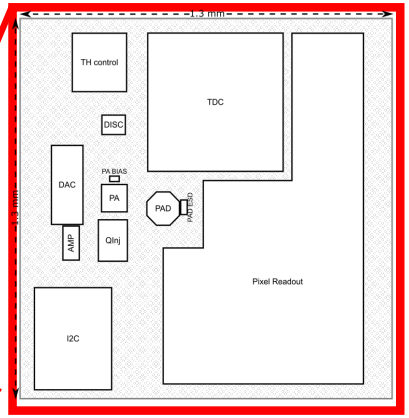
~ 41.3/38.0/41.3 ps (2022 beam test)

reproduced last year's beam test results, with new ETROC1 boards and independent analysis

(2022 beam test mostly done by 4 graduate students)

ETROC2 design: most building blocks have been silicon proven

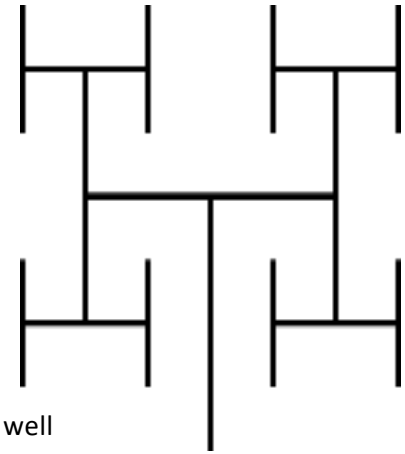




Front-end:
Charge injection/DAC
Preamp,
Discriminator
TDC

All tested in ETROC0/1,
and reused in ETROC2

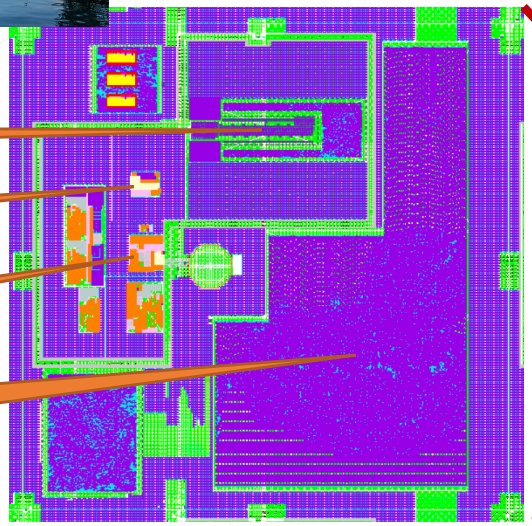
- PLL
  - PLL is based on lpGBT and validated with PLL test chip (+SEU)
- I2C
  - I2C design validated with I2C test chip, including SEU
  - In-pixel I2C register expanded and verified
- TS (Temp Sensor)
  - TS validated with I2C test chip
- Efuse
  - Efuse validated with I2C test chip
- VREF
  - VREF validated with I2C test chip
- GRO
  - Reusing the GRO in ETROC1
- Tx and Rx
  - reusing Tx in ETROC1
  - Reusing Rx in ETROC1(from lpGBT)
- WS (Waveform Sampler)
  - Rad-hard version tested and works well
- In-pixel threshold calibration
  - tested with ETROC0 via FPGA emulator

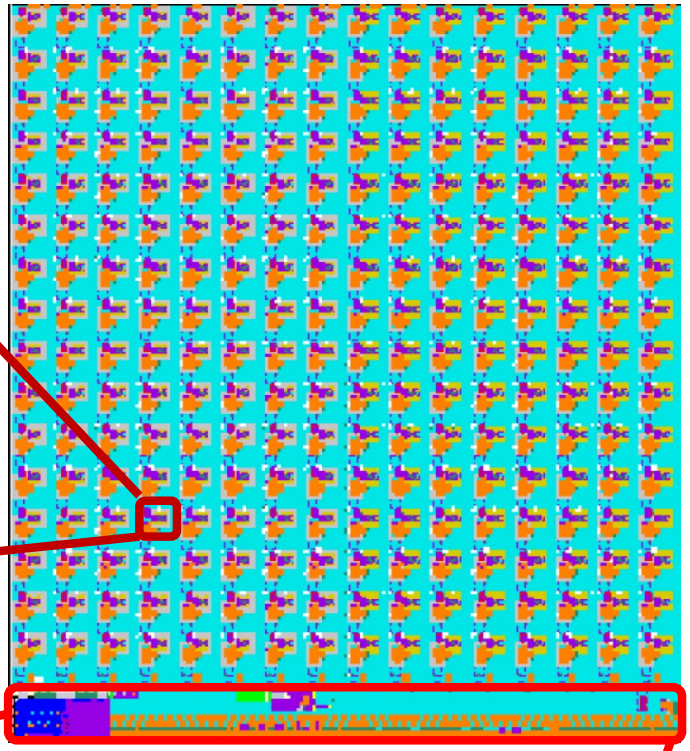


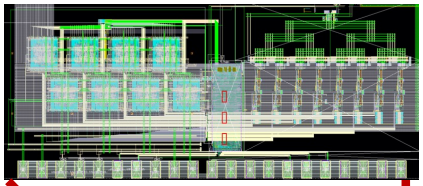
All critical analog building blocks have been silicon proven in testing chips,
and the digital building blocks have been emulated in FPGA and tested with the downstream readout board with backend.

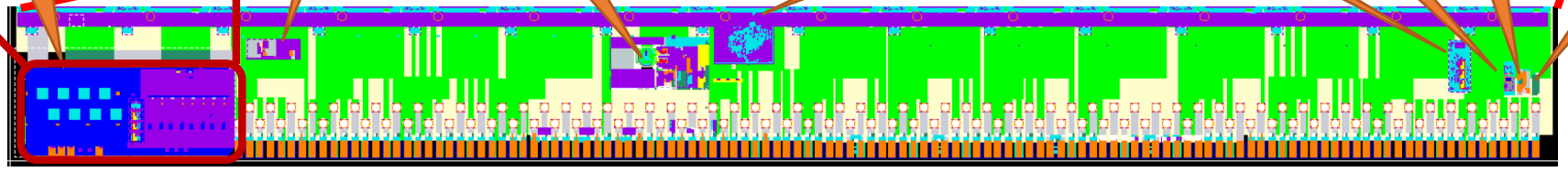
ETROC2 layout (submitted on Oct 21, 2022)

From Quan Sun



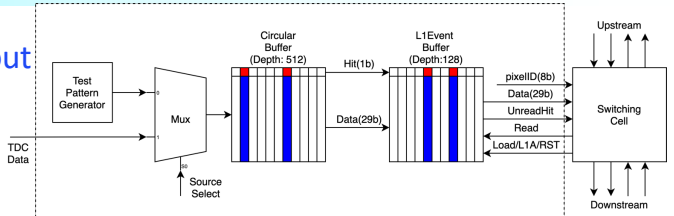




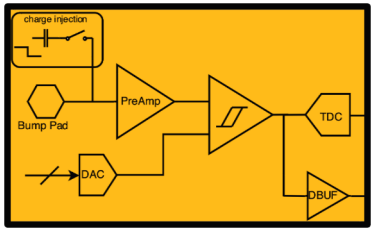


ETROC2 key features: from user point of view

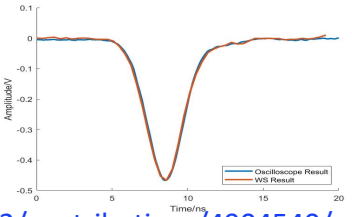
ETROC2 pixel readout



- Self-test pattern generator
  - Can be used to test the digital data flow and link interfaces. Users can dial the occupancy of pixels and change patterns
    - This feature has been used extensively to simulate and verify the readout design of ETROC2, at RTL level and post layout stage
    - First thing user can test with ETROC2 emulator, the same test can then be done for bare ETROC2 and bump bonded ETROC2
    - At chip level (as *build in self-testing capability*), board level, and system level (with DAQ backend)
- Testing with charge injection
  - *Test the full path from charge injection to preamp to discriminator to TDC to circular buffer to event buffer to global digital readout*
  - Discriminator threshold scan and jitter measurements (bare ETROC2 first, then bump bonded ETROC2)
  - User can define the window for TOA, TOT and CAL to filter/suppress hits before readout
  - User adjustable TOA measurement window (up to 12.5ns, 11.4ns effective)
  - Each pixel can be enabled or disabled for DAQ readout
  - The relative phases adjustable between the TDC clock, pixel readout clock and global readout clock

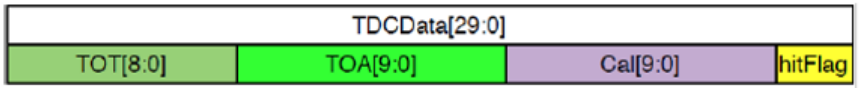


- Bump bonded ETROC2 testing with laser, source and then beam
  - Full path timing performance study including LGAD
- Auto-threshold scan within pixel
  - This new feature will be studied first by dedicated ETROC2 chip level testing
- Trigger path
  - Can be used for monitoring purpose initially, a coarse map of user defined hits continuously sent out every BC
  - Can be used for self triggering for beam test if so desired, user can define the window for TOA, TOT and CAL for triggered hit
  - Use flashing bits in empty BCID (beam gap), defined via I2C. Can be used as cross check and monitoring purpose.
- Waveform Sampler
  - Able to record waveform of one pixel up to 16 bunch crossing (400 ns), start and stop controlled via fast command, readout via I2C
  - power-down when not used, intend to use for monitoring purpose during detector operation
- Power consumption estimate is ~1W per chip, to be confirmed with ETROC2 chips



https://indico.cern.ch/event/1127562/contributions/4904540/

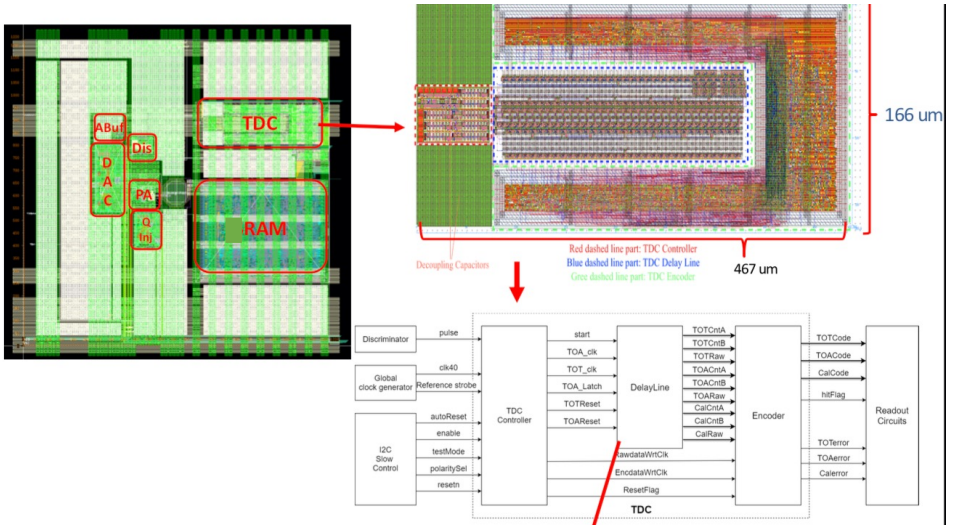
TDC operation

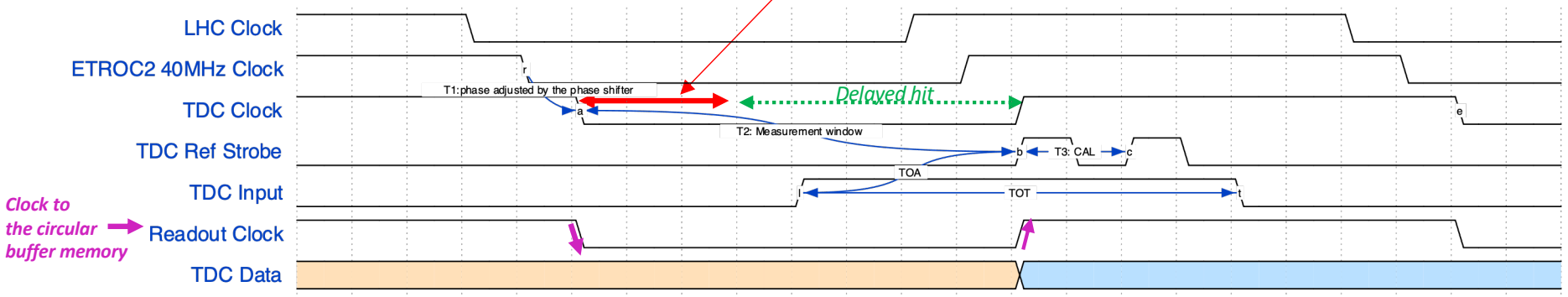


hitFlag: discriminator is fired or not

- ❑ bin= T3/Cal_code
- ❑ TOA=12.5 - bin*TOA_code

T3 is programable with, 3.125 ns by default.





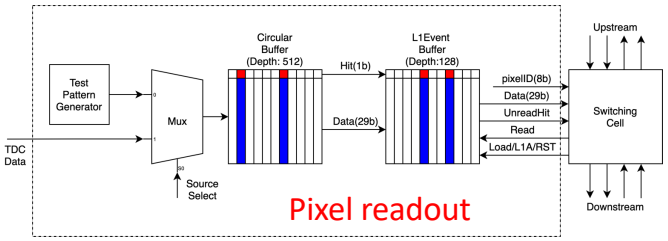
1984 IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 68, NO. 8, AUGUST 2021

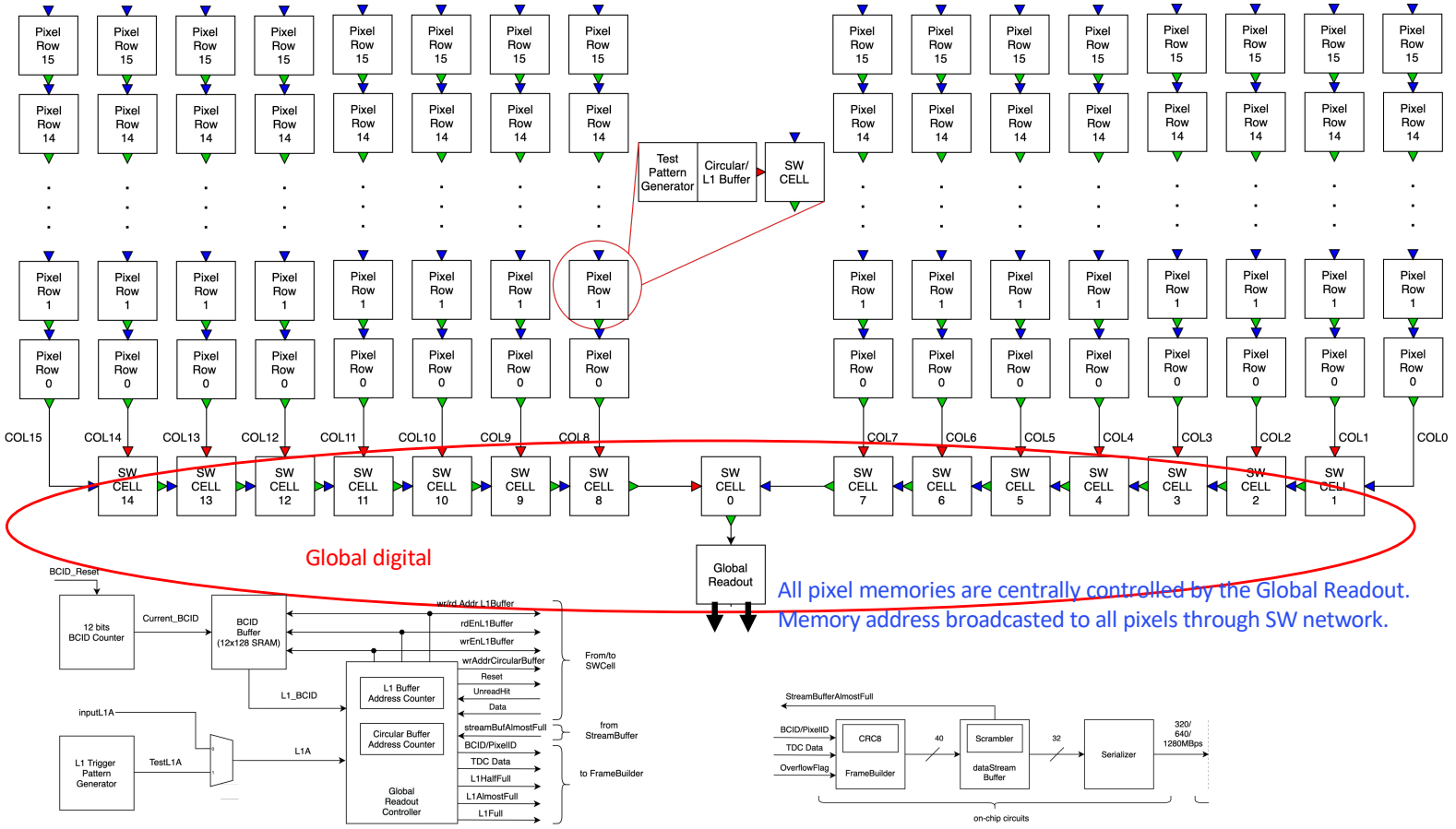
A Low-Power Time-to-Digital Converter for the CMS Endcap Timing Layer (ETL) Upgrade

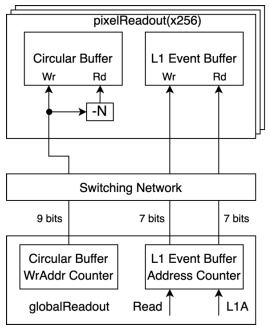
https://ieeexplore.ieee.org/document/9446843

The overall ETROC readout

Datao Gong



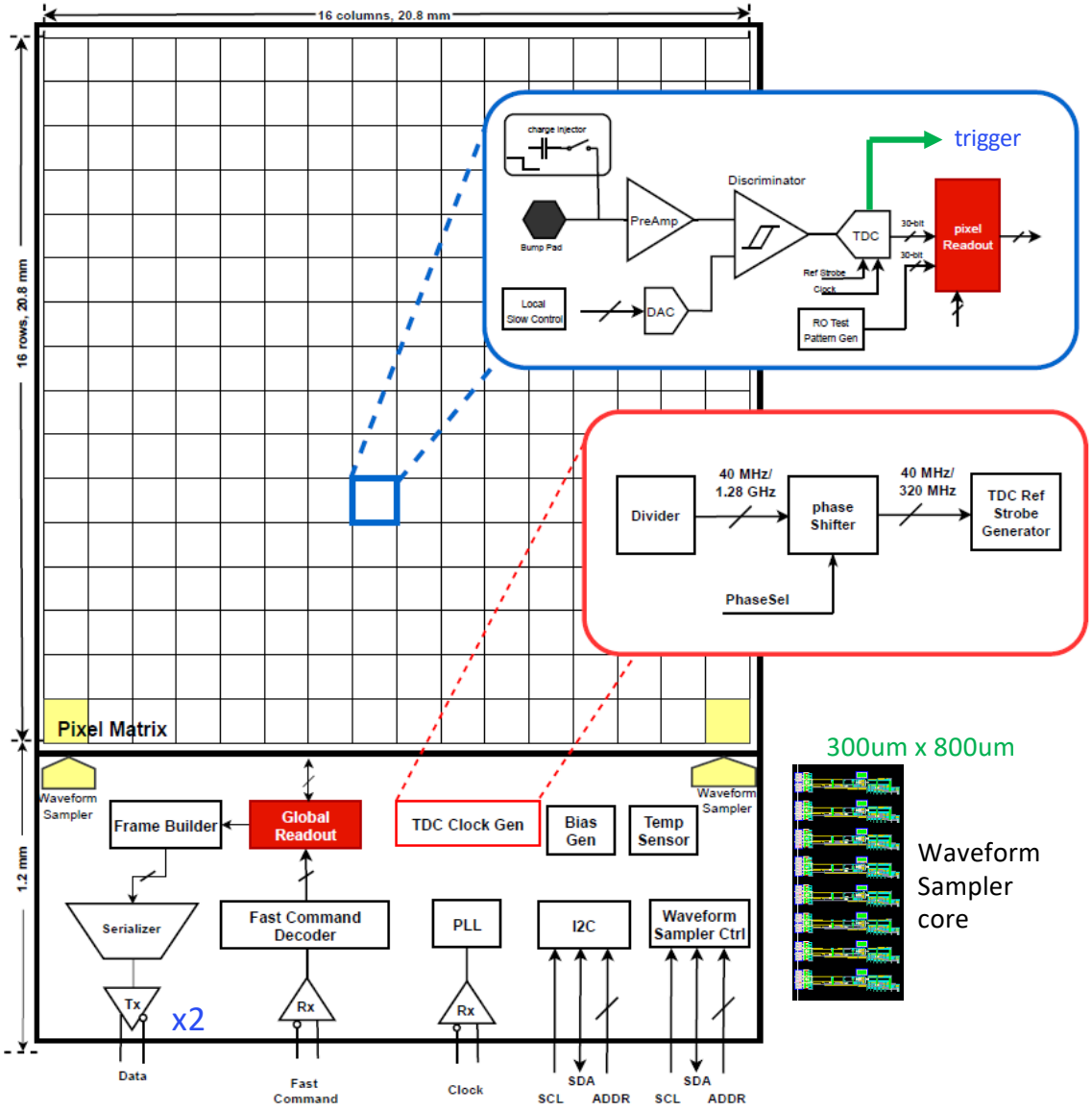


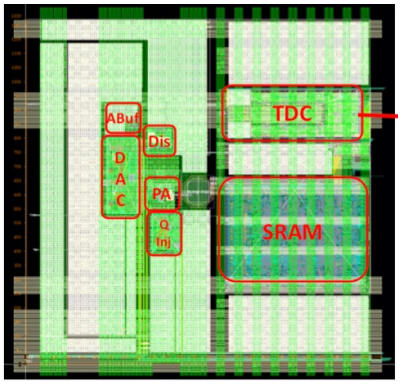


The ETROC2 emulator will emulate the entire ETROC2 digital processing chain. Details see talk at TWEPP 2022,
"An FPGA-based readout chip emulator for the CMS ETL detector upgrade" by Tiankuan Liu/Jinyuan Wu.
https://indico.cern.ch/event/1127562/contributions/4904781/

ETROC: pixel size vs design block size

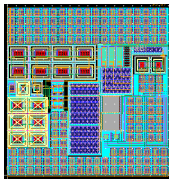
65nm implementation





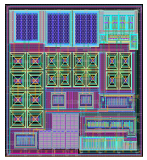
ETROC1 pixel layout

Preamp



90 um X 94 um

Discriminator

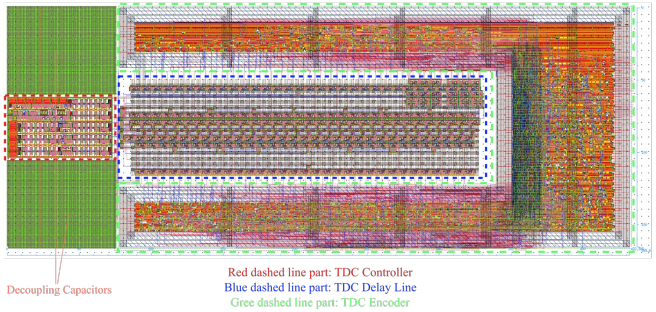


81 um X 67 um

300um x 800um

Waveform Sampler core

TDC: 467 um X 166 um (can be optimized and subdivided)



RAM hit buffer
250 um x 150 um

Hit circular buffer

Future challenges: how to reduce the pixel size from 1.3mm x 1.3mm to say 250µm x 250µm?

Towards the future: What can 3DIC VERTICAL INTEGRATION help?
→ repartition the design blocks into multi-tiers

Phase II SBIR proposal (EPIR-Fermilab):

"Versatile, high-density, high-yield, low-capacitance 3D integration for nuclear physics detectors" (phase 2)

For Proof-of-principle demonstration:

- 250µm x 250µm pixel
- 8×8 pixels

Sensor: for example, Small-pixel AC-LGAD

Vertically integrated chip

Front end preamp + discriminator + charge injector

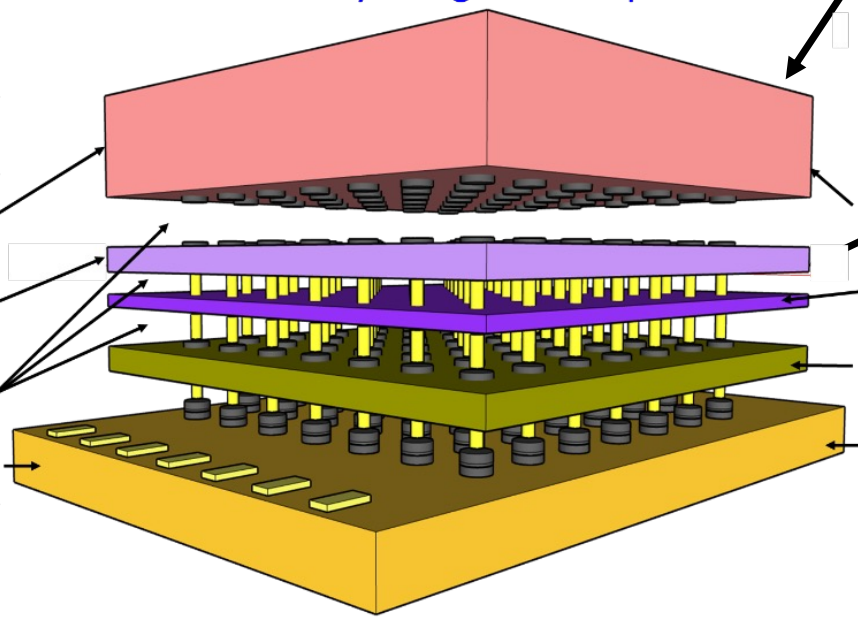
Low power TDC + H-tree clock distribution

Circular buffer memory array + readout logic

done

Task	Period
Detector: LGAD	Phase 1
Front end preamp + discriminator + charge injector	Phase 1
Modified direct bond interconnect	Phase 1
PCB: LGAD	Phase 1

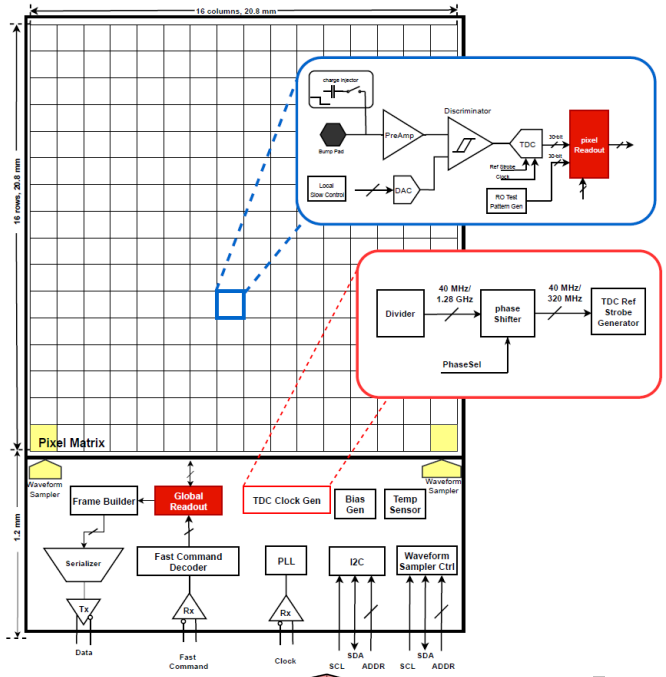
Task	Period
Detector: AC-LGAD	Phase 2
Low power TDC	Phase 2
Readout circuit	Phase 2
PCB: AC-LGAD	Phase 2

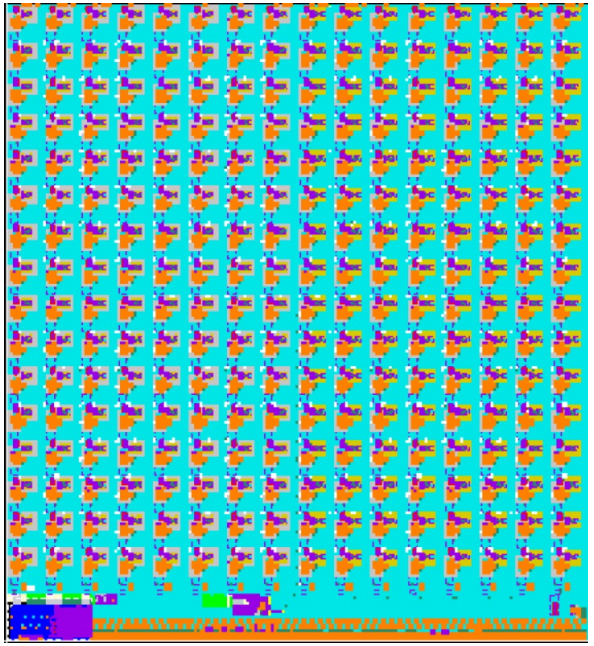


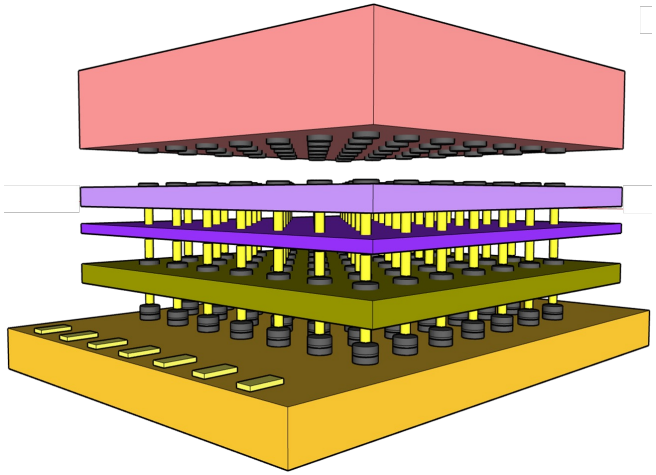
3DIC providing separation of low-noise analog circuitry from digital blocks.
Interconnections made by TSVs and Direct Bond Interconnect (DBI).

From CMS ETROC to future R&D

CMS ETL ETROC: from Concept (2019) to full chip design ETROC2 submission (Oct 2022)







"Versatile, high-density, high-yield, low-capacitance 3D integration for nuclear physics detectors" (phase 2)

Phase 1 done

Phase 2 proposal submission next week

VTROC R&D: From Concept to first demonstration for proof-of-principle