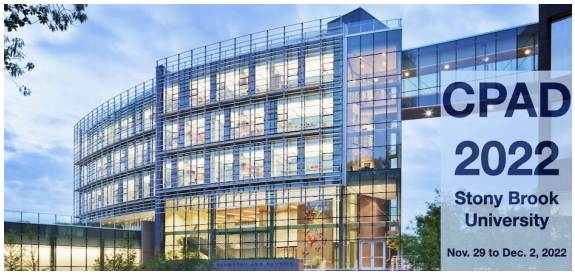

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The ETROC project: Precision Timing ASIC Development for LGAD-based CMS Endcap Timing Layer (ETL) upgrade

Thursday, 1 December 2022 11:35 (20 minutes)

The Endcap Timing ReadOut Chip (ETROC) is designed to process LGAD signals with time resolution down to about 40-50ps per hit, in order to reach 30-35ps per track with two detector layers. The most critical element of the ETROC is the analog front-end, namely the preamplifier and the discriminator and the TDC. The challenge here is to reach this level of time resolution while keeping the power consumption below ~3mW per pixel. In addition, the precision delivery of the clock signal to all pixels is also important, its contribution should be kept below 10ps. Due to the challenges described above, the development of the ETROC ASIC is divided into three prototyping phases: ETROC0 (single channel), ETROC1 (4x4 array) and ETROC2 (full size 16x16 with full functionality), with ETROC3 intended to be the final design. In this talk, the development strategy and the performance of ETROC0 and ETROC1 including lessons learned will be presented first, followed by the full size full functionality ETROC2 design (submitted in Oct 2022), with comments on future prospects and challenges for precision position and timing detector R&D.

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