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Automated Circuit Skeleton for All-Digital Implementation of Configuration-Testability-Readout Functionalities in Front-End ASICs

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There are three basic elements in every semiconductor radiation detector: the sensor, the readout chip front-end, and readout chip back-end. To achieve the best possible performance, each of these components must interoperate with each other as well as be optimized within its structure. While sensors and front-end components are often tailored to a specific application, and are relying on the analog domain processing, it may be tempting to develop a versatile but nevertheless sufficiently flexible back-end, that could be almost automatically grown from the code containing its parametrized recipe. The purpose of the back-end is to perform handling and storing of the configuration data, assuring testability, processing output data from the front-end before sending it to the acquisition system and sending the results off chip. Reaching the readiness of the parameterized code, which when executed results in unpacking the physical structure of the entire back-end contributes to reducing the workload of both the ASIC designer and the test engineer, thanks to the ability to reuse already developed solution. It also minimizes the risks of failure. We have developed such a generic and optimized framework, in which the readout part is based on the EDWARD architecture [1], along with a method for its implementation using CAD tools for synthesis and automatic P&R. We present this implementation flow here and hope that with this approach we can soon expand the portfolio of detectors being developed at BNL.

References

[1] D.S. Gorni et al 2022 JINST 17 C04027.

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