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U.S. DEPARTMENT OF ENERGY

Highly-scalable, Cryogenic Readout Electronics
LArPix & LightPix

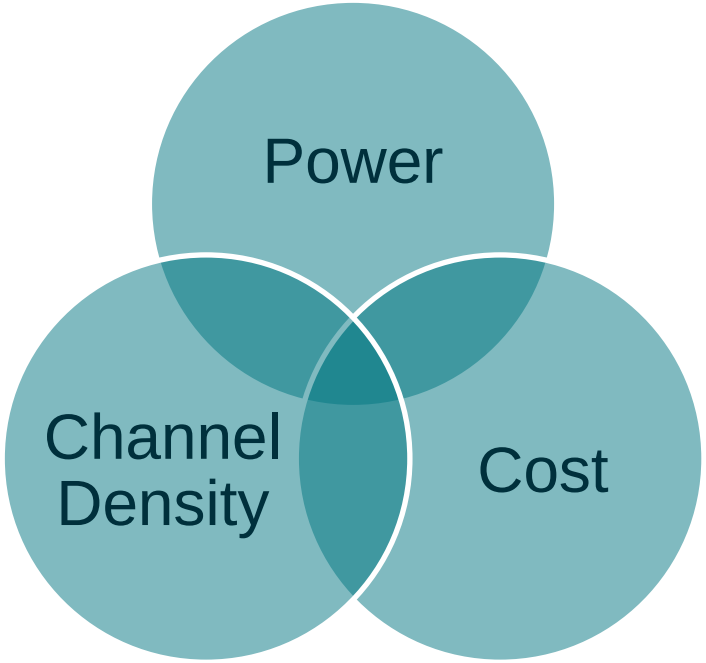
Brooke Russell

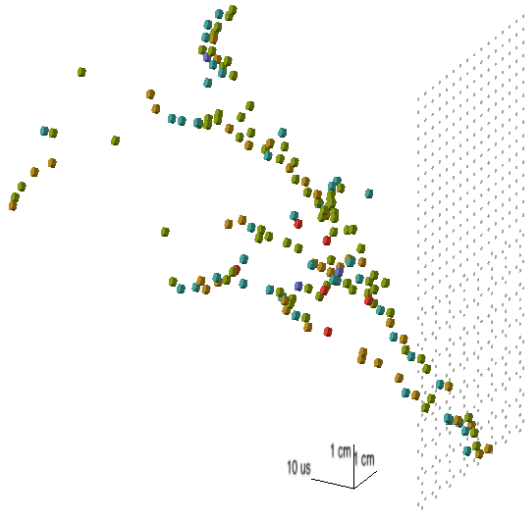
CPAD Workshop

December 1, 2022

Granular readout electronics for cryogenic applications

Key challenge: scalability





LArPix-v1 recorded cosmic EM shower

First proof of principle demonstration
by Dan Dwyer *et al. JINST 13 (2018) P10007*

LArPix: scalable LArTPC pixel readout

LightPix: scalable, cryogenic-compatible SiPM readout

LArPix

SLAC

Penn

Berkeley
UNIVERSITY OF CALIFORNIA

UCDAVIS
UNIVERSITY OF CALIFORNIA

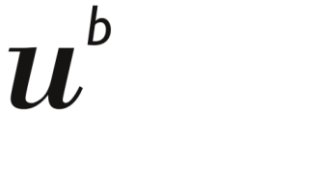
YORK
UNIVERSITÉ
UNIVERSITY

Yale

Caltech

UC SANTA BARBARA

UCI University of California, Irvine



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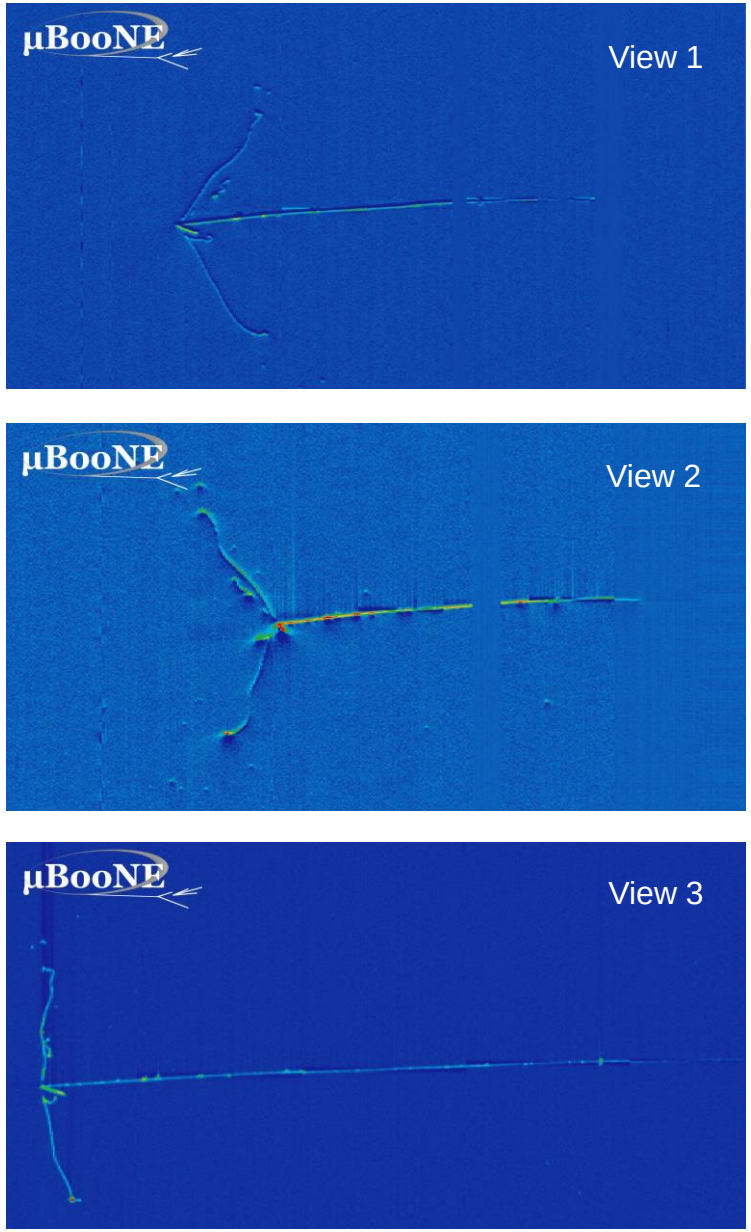
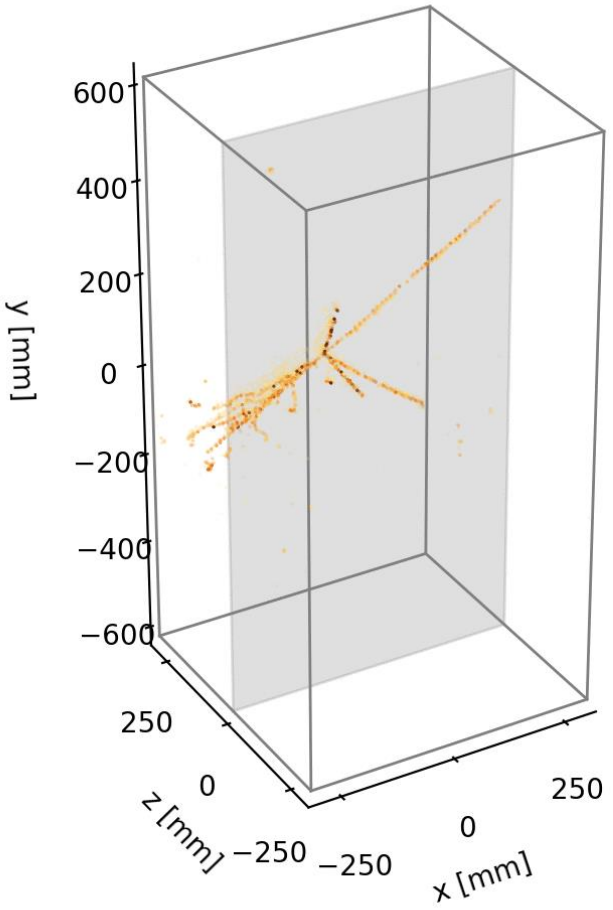
Why pixels?

- True 3D imaging
  Unambiguous, inherently 3D raw data
- Self-triggered pixel-by-pixel data
  ~100% livetime

Technical challenge: instrumenting ~1000 m^2 anode area at 4 mm granularity → **requires scalable design**



Traditional wire readout
(MicroBooNE ν data)



Pixel readout
(LArPix cosmics data)

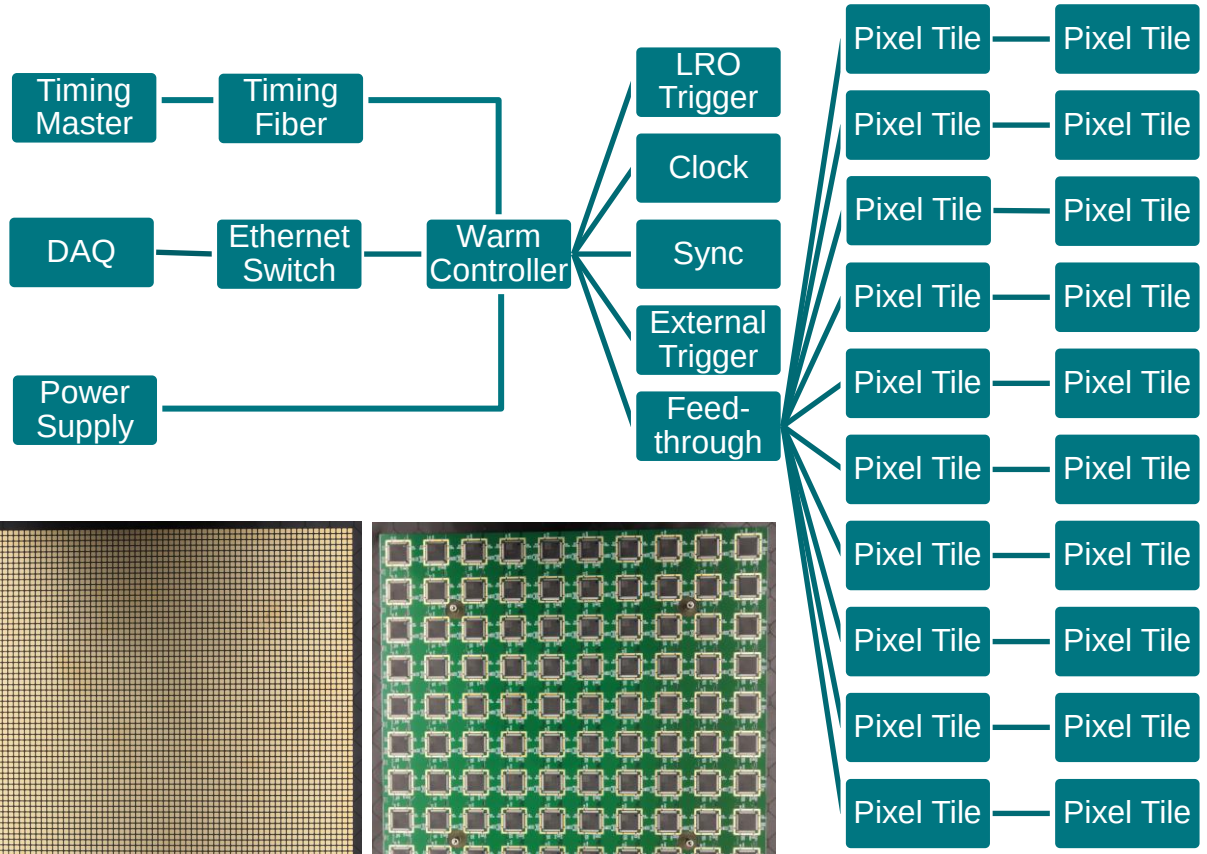
LArPix System Architecture

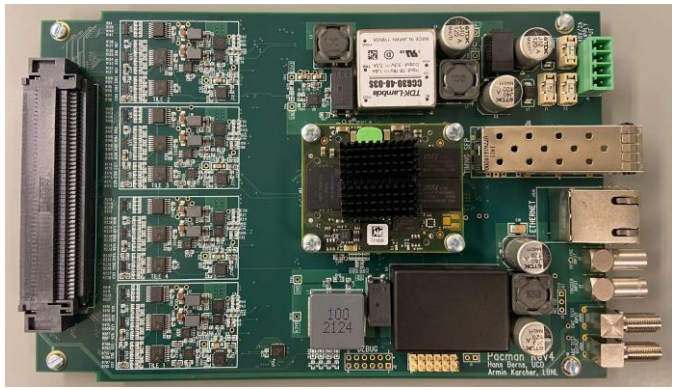
A contained, end-to-end system focused on reliability & robustness

- Limit single-point failures
- Scalable to O(M) channel systems

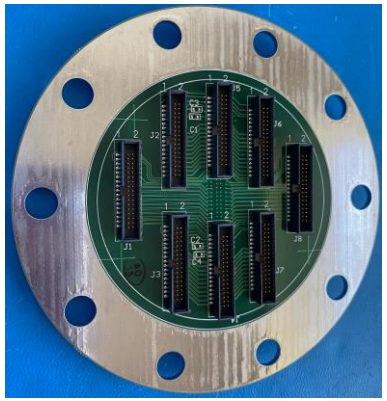
Design features

- Single active component in cryo environment
- Minimal and redundant connections to outside cryostat
- Mechanically and cryogenically robust





PACMAN Warm Controller



Feedthrough

32 cm by 32 cm anode PCB tile

LArPix ASIC Concept

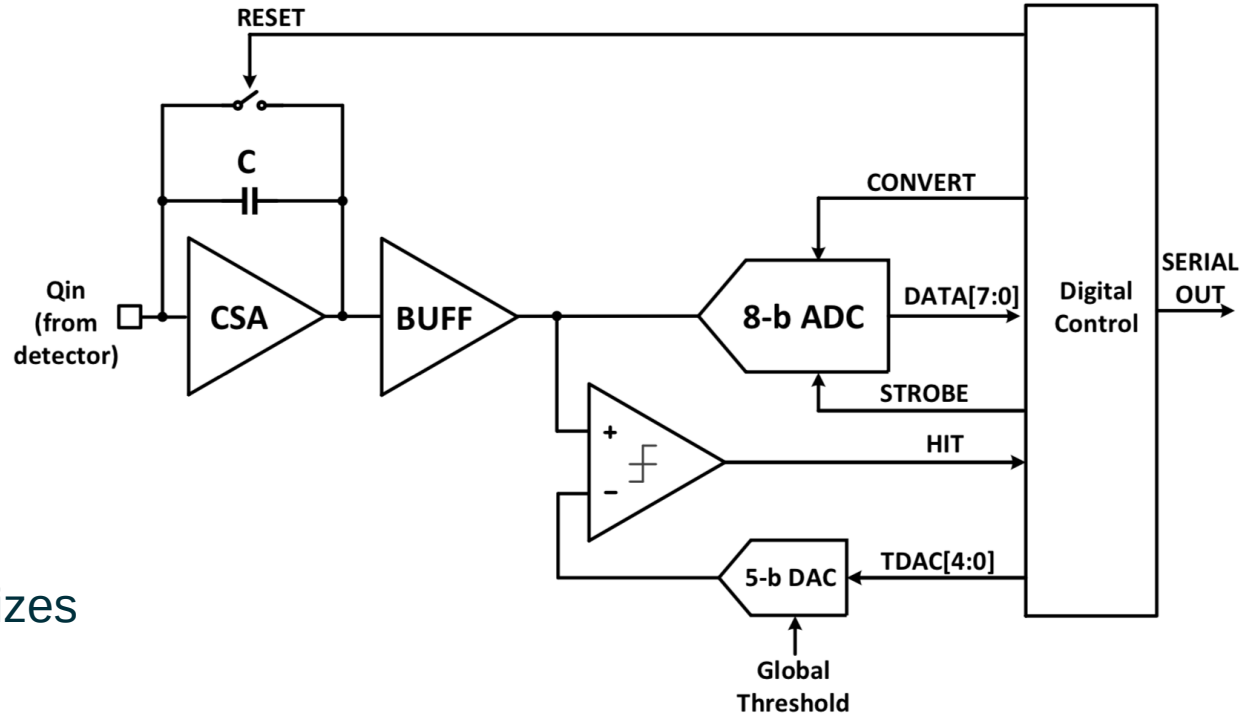
Low-power, integrating amplifier with self-triggered digitization and readout

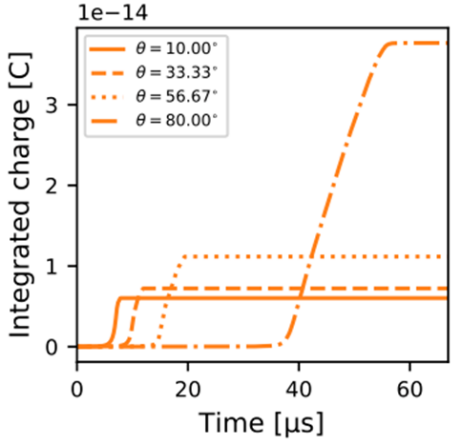
Pixel dormant until signal exceeds tunable threshold

- Integrates charge for ~3μs (~4 mm drift), then digitizes
- Ready for next signal

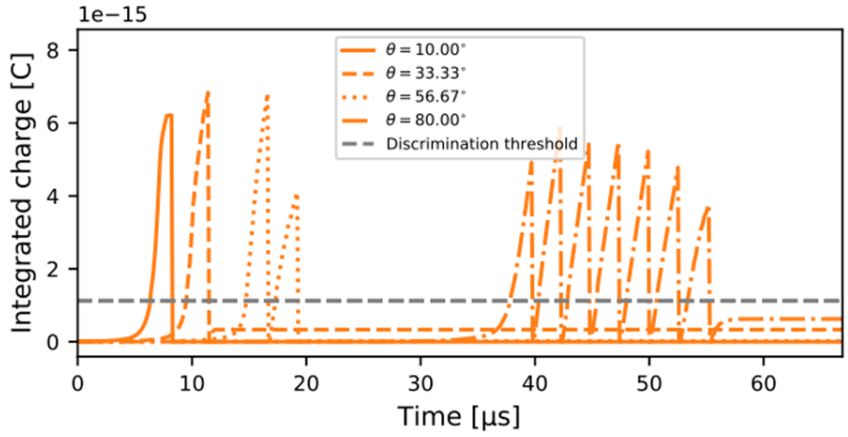
Pixels are continuously active

- Serial I/O data rate is slow (~5 Mb/s per I/O channel) to limit digital power
- Modest data volumes: ~1 MB/s per square meter of anode in surface cosmic flux





Simulated front-end charge integration



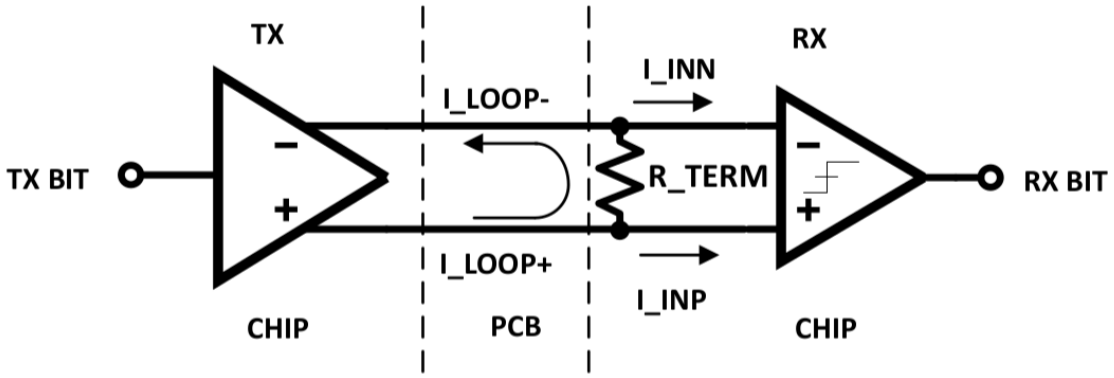
Incorporation of buffering, ADC sampling, and digitization

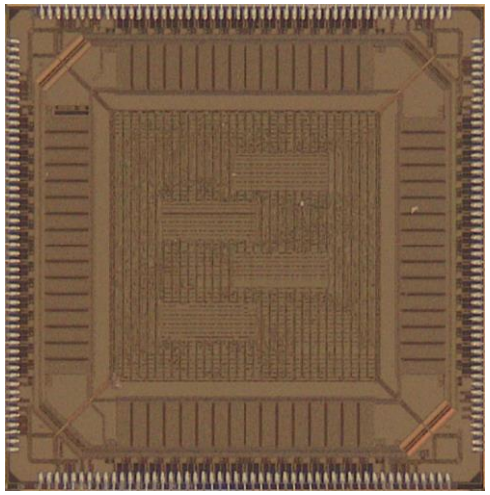
LArPix-v2 ASIC Implementation

Version	CMOS Process	Receipt	I/O
2a	180 nm	2/2020	Pseudo-differential
2b	180 nm	8/2021	True differential
2c	130 nm	11/2022	True differential

LArPix-v2b, -v2c ASIC: low-voltage, low-power digital I/O

- O(10 μW) per transmitter & receiver
- Highly-tunable loop current and termination resistance supports multiple modes of operation (chip-to-chip, multi-drop, etc.)
- Optional mode for automatic transmitter power-down when no data





LArPix-v2b ASIC

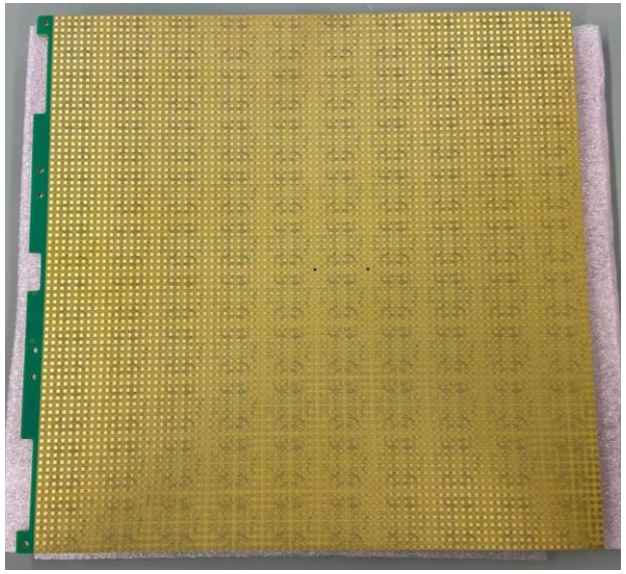
Specification	Value
Analog inputs	64
Dynamic range	1.5 V
ADC resolution	8 bits
ADC LSB	4 mV (chip configurable)
Threshold range	0 to 1.8 V (channel configurable)
Timestamp precision	100 ns (1 clock cycle)
FIFO event memory depth	2048

"LArPix-v2: a commercially scalable large-format 3D charge-readout scheme for LArTPCs"
publication in preparation

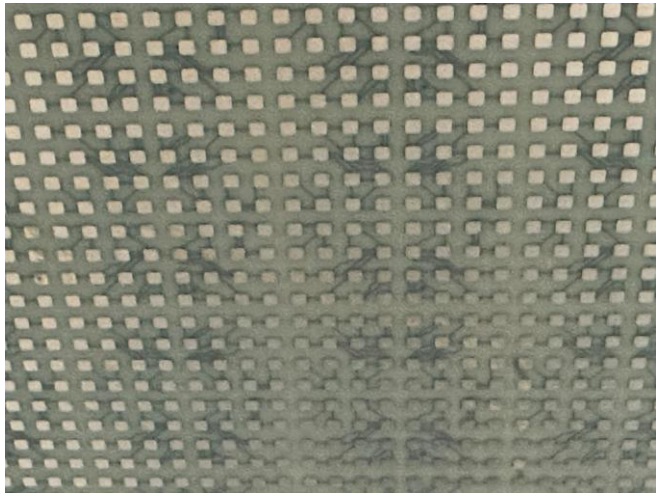
LArPix-v2b Performance

- Low-voltage I/O working as designed
- Prototype v2b-based pixel tiles deployed in LArTPC operation

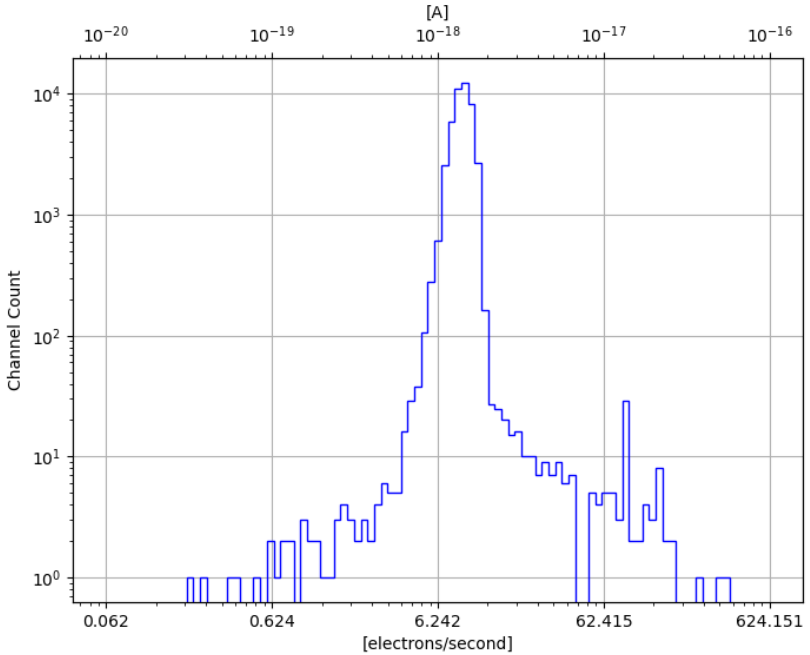
Specification	Value
Gain	4.5 μV/e-
Noise	~800 e- ENC
Leakage current	<< 100 aA
Power	O(100 μW) / channel

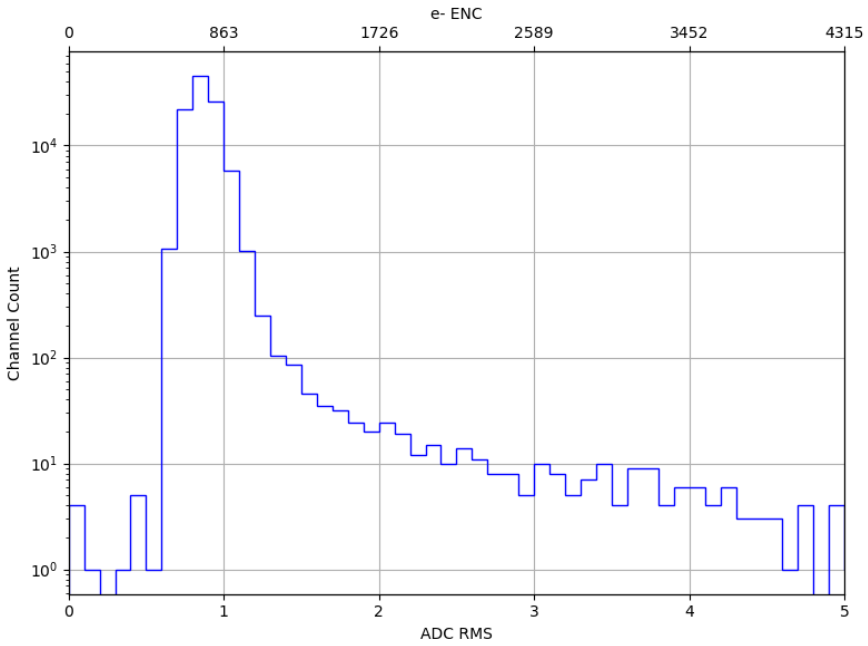


32 cm by 32 cm LArPix-v2b anode PCB tile



3.8 mm pixel pitch
100 ASICs/tile
6400 channels/tile





Hydra IO

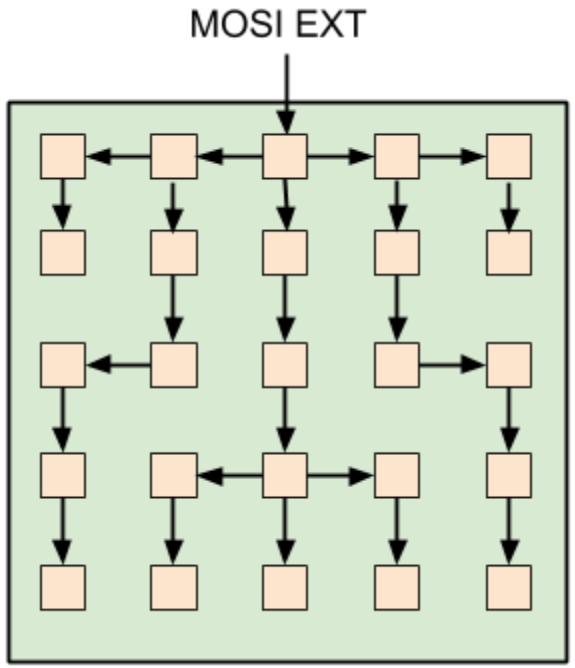
Dynamic I/O routing

AD-HOC NETWORK OF READOUT APPLICATION-SPECIFIC INTEGRATED CIRCUITS FOR RELIABLE DETECTOR INSTRUMENTATION
U.S. Patent Application Ser. No: 63/140,434

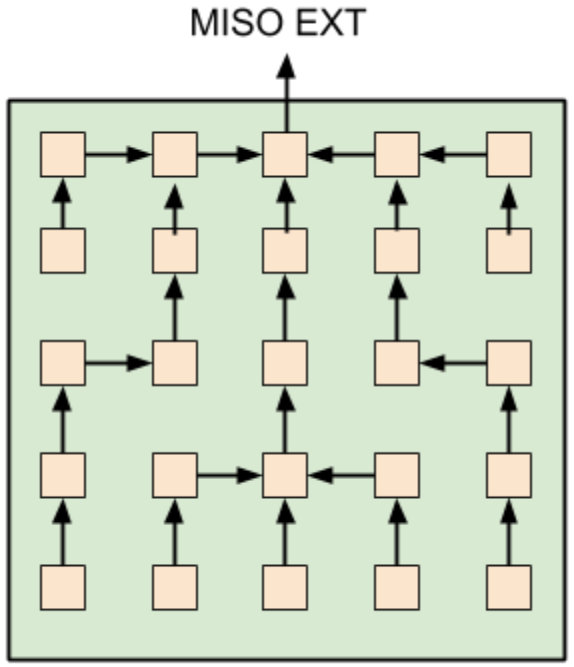
2022 R&D 100 Award

- I/O can occur between any neighboring chips on pixel tile
- Network constructed by explicitly connecting neighboring ASICs in a determined fashion

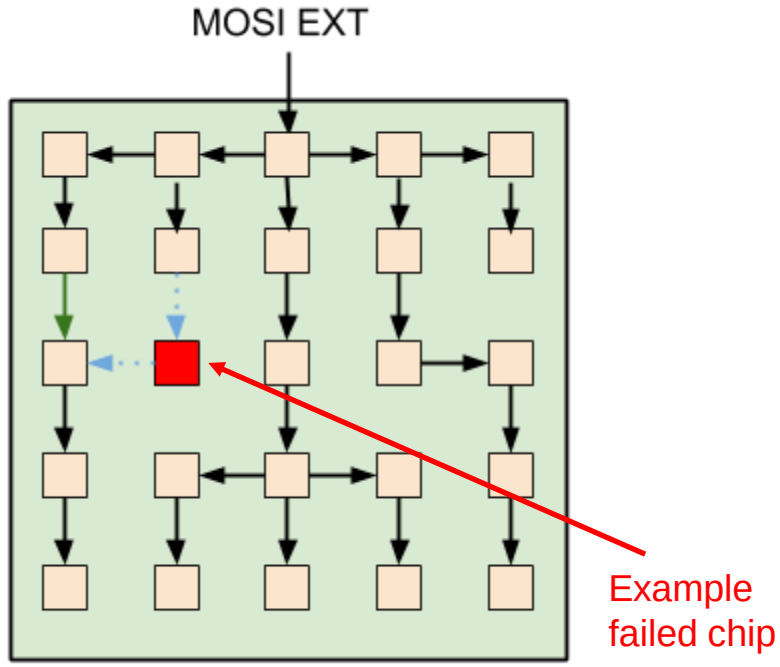
Realized and exercised with LArPix-v2



Upstream configuration commands



Downstream data flow

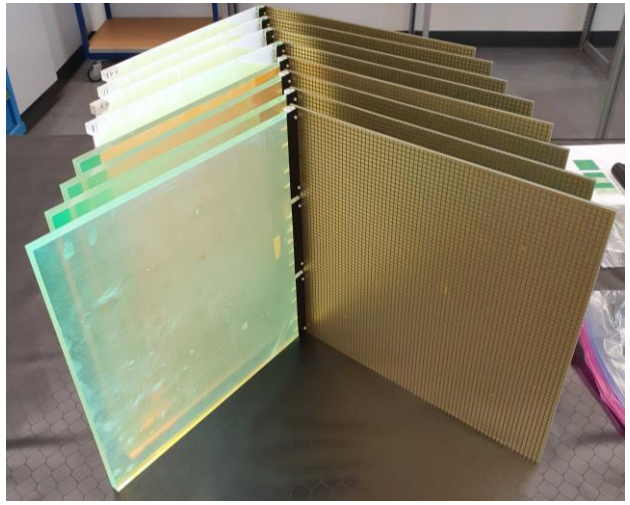


Network reconfigured to avoid failed ASIC

Digital multiplexing: *O(1k) pixels / I/O channel*

System Prototyping

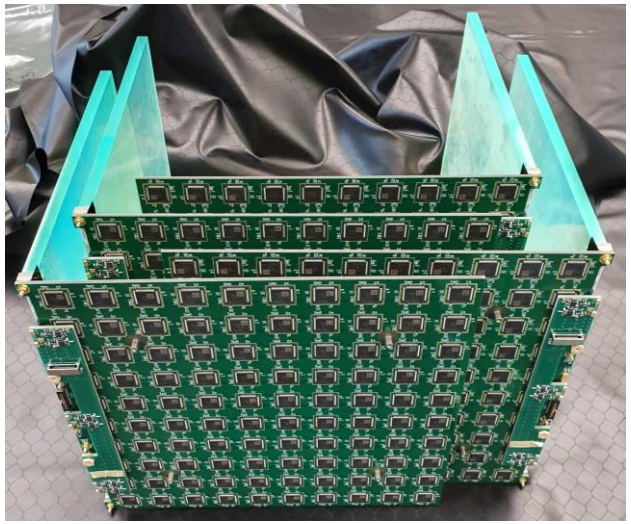
- All production and assembly performed by industry
- Individually tested O(10k) ASICs, O(100) pixel tiles
- Three ton-scale TPCs built and tested

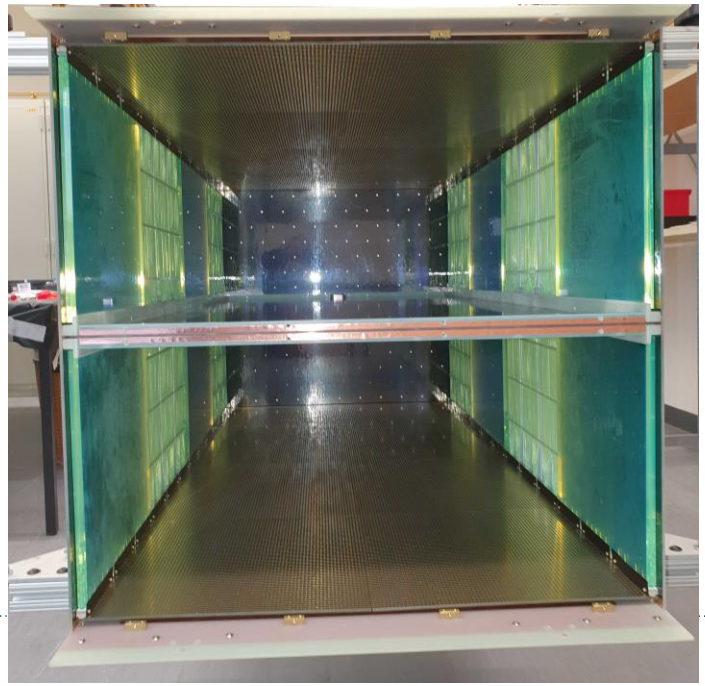


Single pixel tile & light module assemblies

One anode, fully-assembled

Fully-assembled LArTPC module



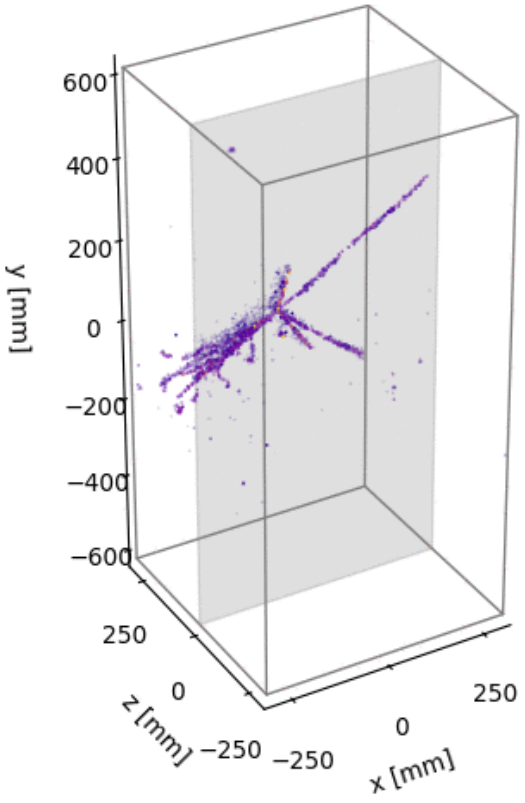


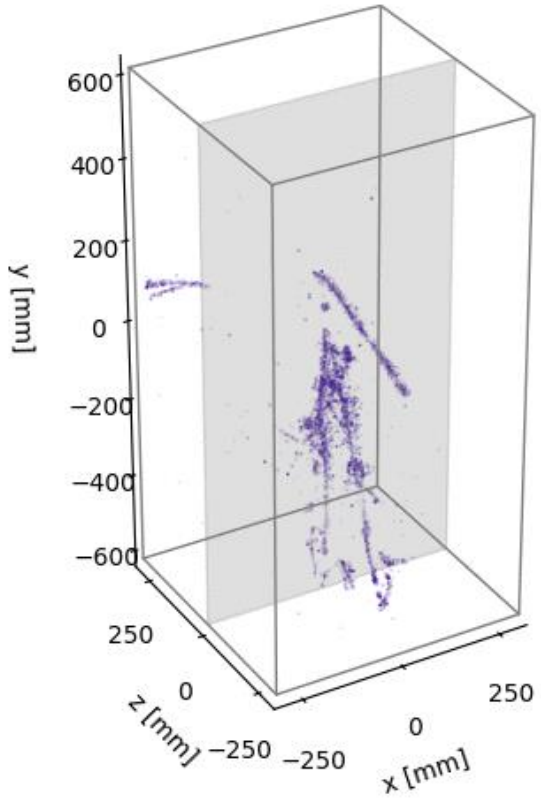
Two anodes installed inside field cage

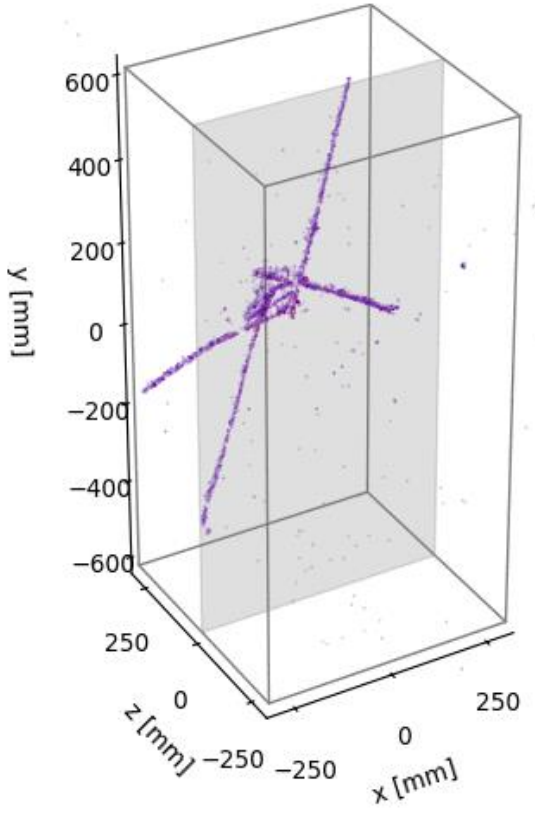
System Prototypes

Raw data with 200 keV channel threshold

- Successful deployment and operation of **three** O(100k) channel systems – *>100M cosmic ray events recorded*
- Quick-turn industry fabrication at competitive cost – *O($0.10/channel) at large O(10 M) channel system*





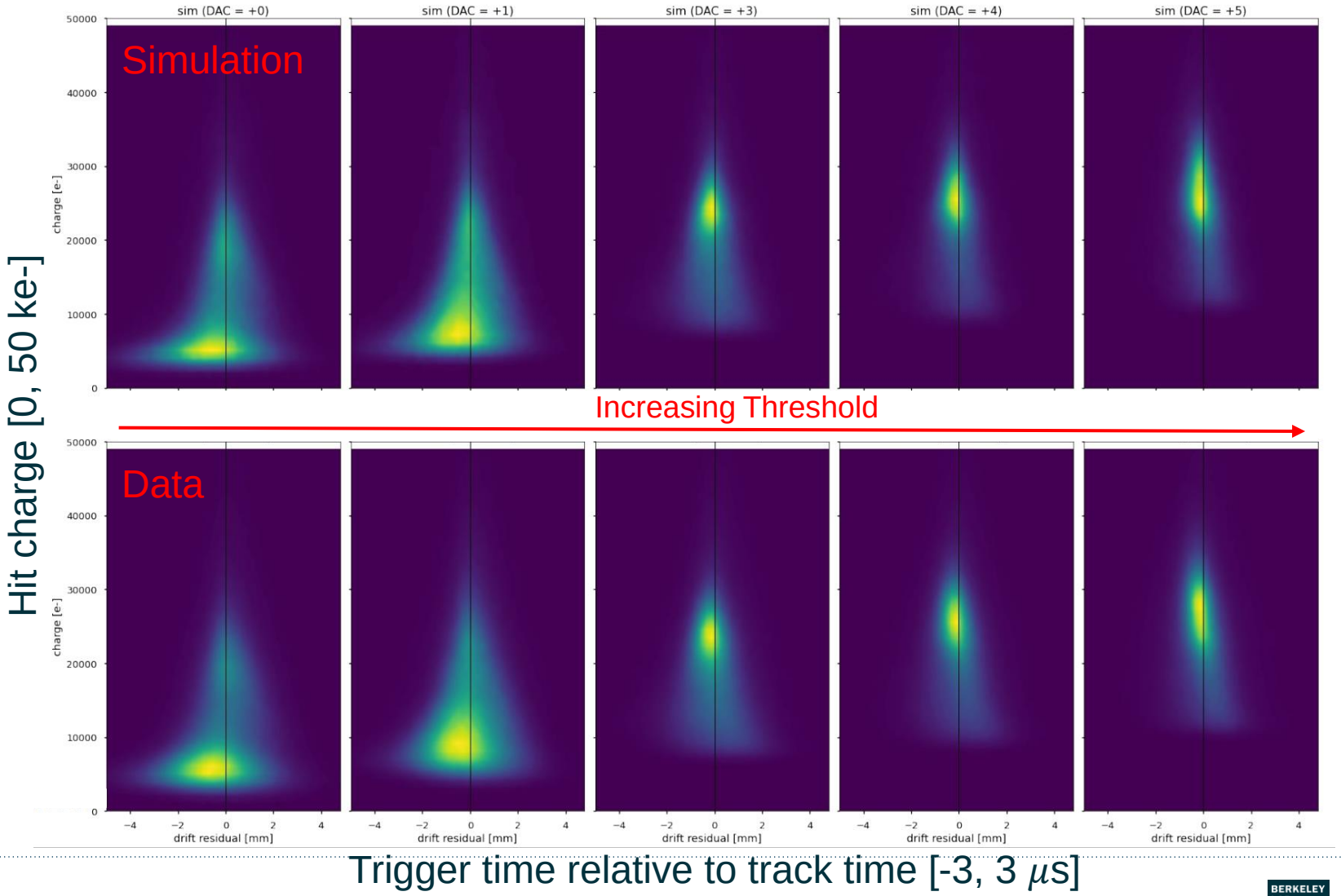


Pixel response validation

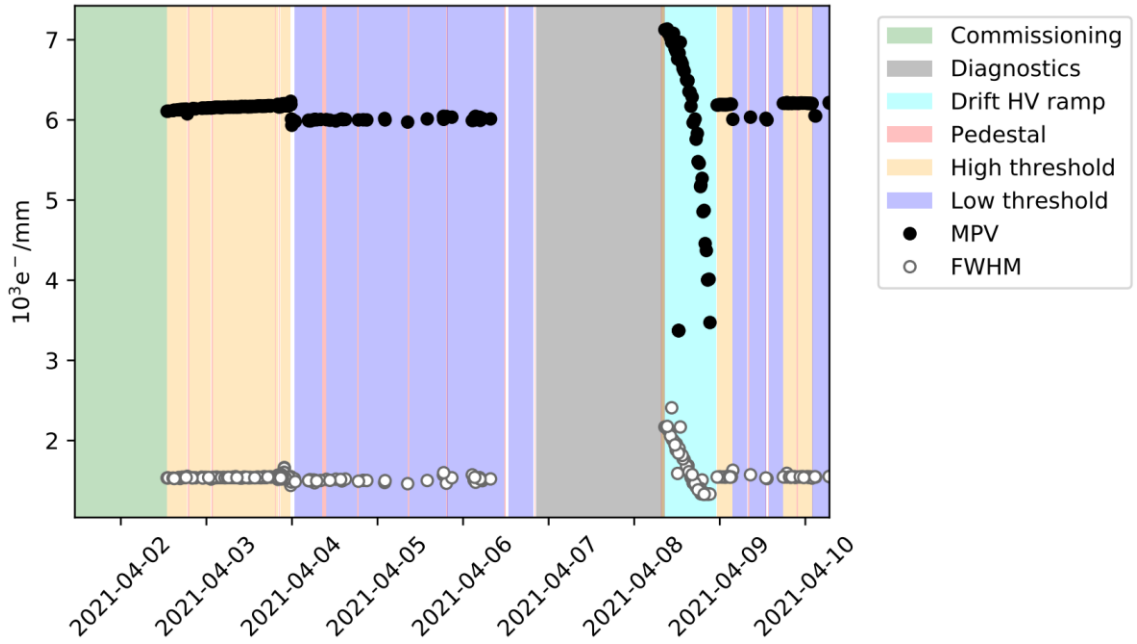
- Detailed ASIC front-end charge response simulation using GPU-optimized algorithms
- To first order, good data-simulation agreement in channel threshold crossing time and charge measurement

"Highly-parallelized simulation of a pixelated LArTPC on a GPU"
publication in preparation

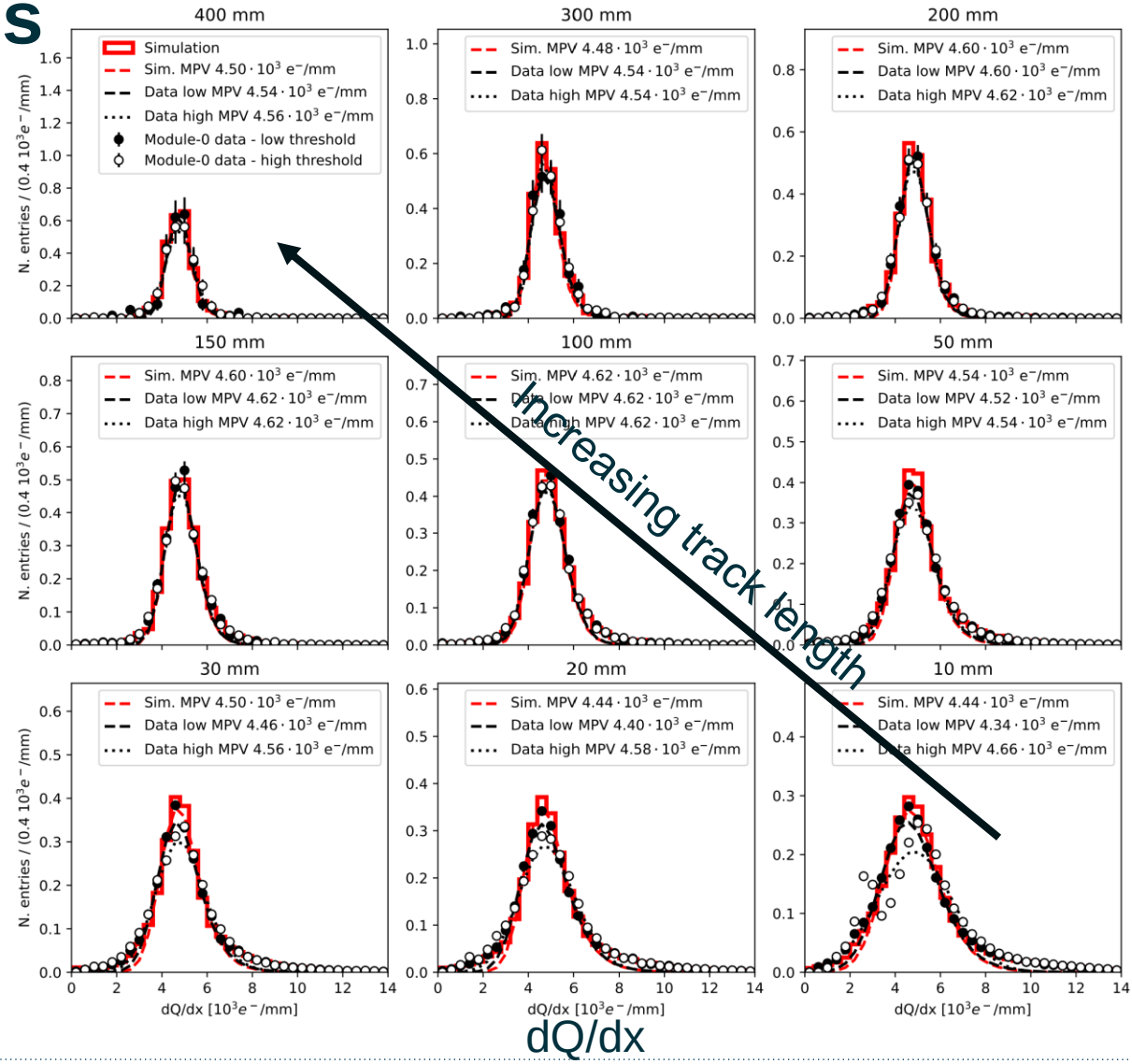
Pixel trigger response versus threshold (data versus MC)



Track-level Cosmic Ray Analysis



- Pixels are continuously active (>100M cosmic ray events recorded)
- Serial data packets stream out of system as channels self-trigger
- MIP response is consistent with expectation and stable throughout data taking

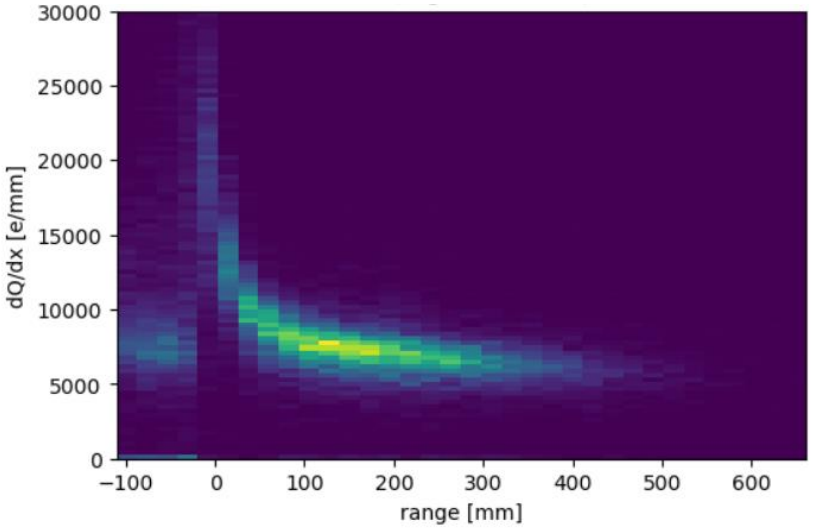


"Performance of a modular ton-scale pixel-readout liquid argon Time Projection Chamber"
publication in preparation

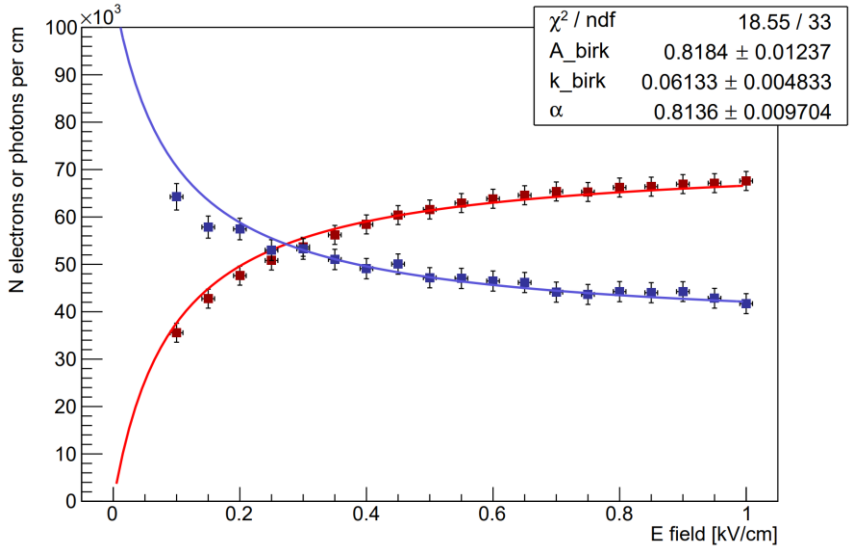
Detector Physics Studies

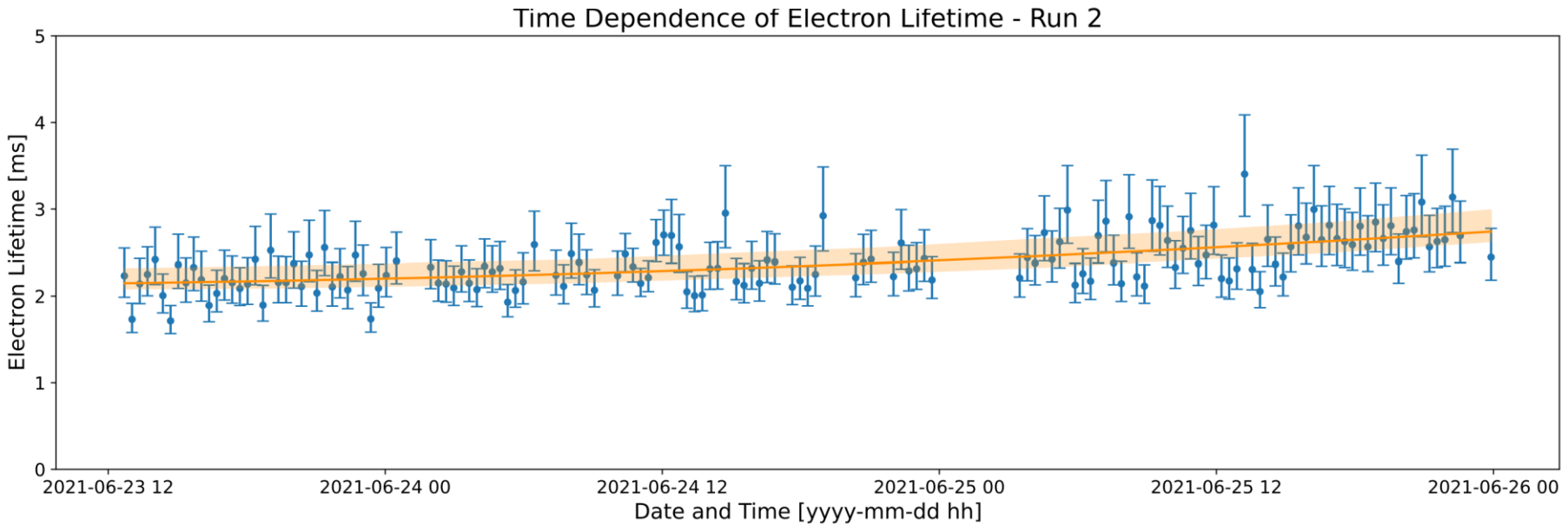
"Performance of a modular ton-scale pixel-readout liquid argon Time Projection Chamber"
publication in preparation

Stopping muon energy loss



Charge-light anticorrelation



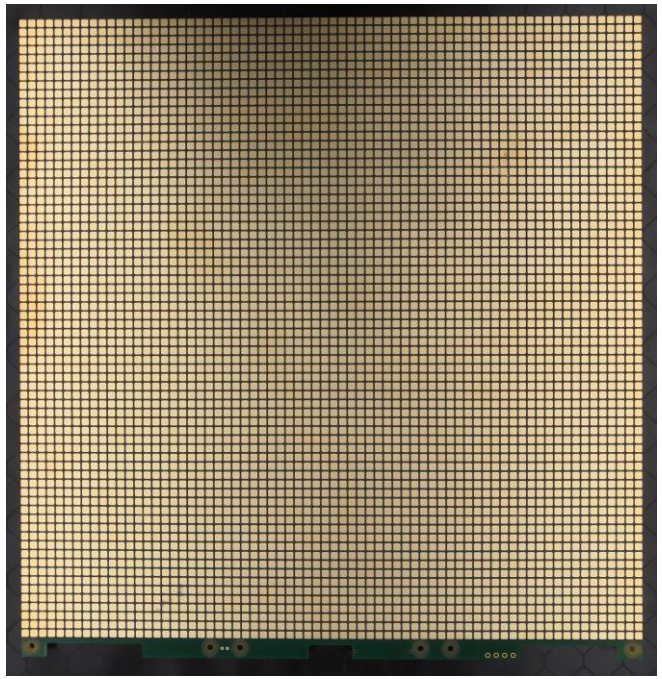


LAr purity electron lifetime

LightPix

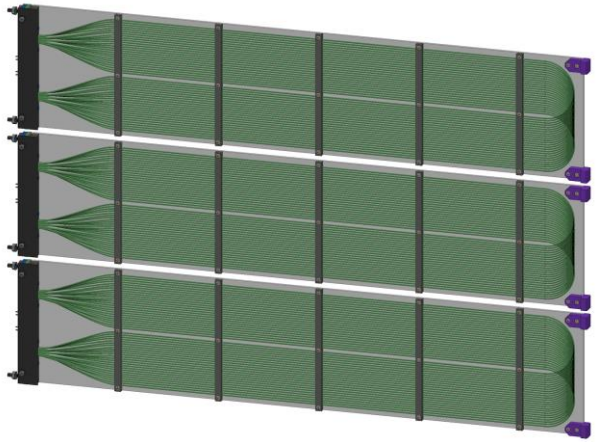
LightPix Concept

- Low-power cryogenic-compatible, scalable (>10^6) SiPM readout electronics at very low system cost
- Adapting existing LArPix system architecture
  - Shared cabling, feedthrough, warm electronics
  - LightPix ASIC re-uses majority of LArPix design, but replaces ADC with TDC
- Provide a path for highly-granular photodetection systems for very large detectors

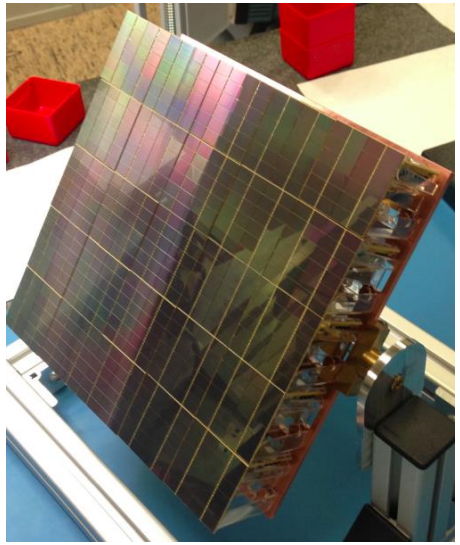


Replace pixel pads with SiPMs

Example of light trap SiPM detector format *LCM*

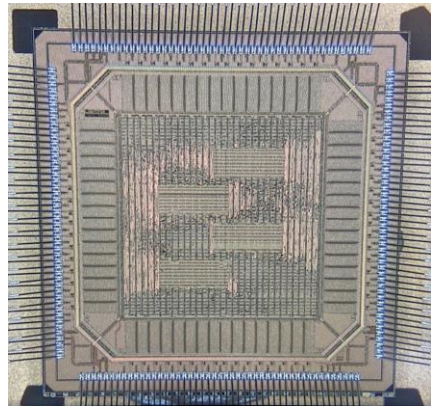


Example of direct SiPM detector format *DarkSide-20k*



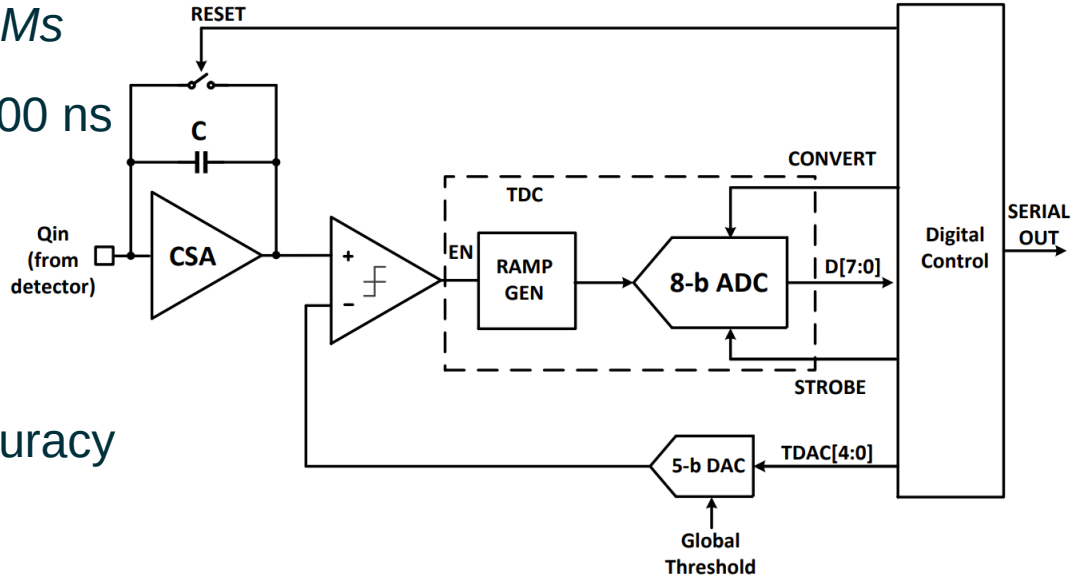
LightPix ASIC Implementation

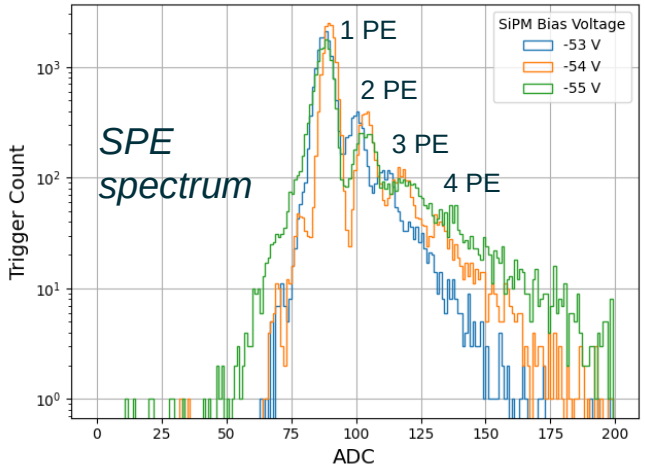
LightPix-v1b ASIC



LightPix-v1b TDC evaluation for SPE from commercial 3 mm x 3mm SiPMs

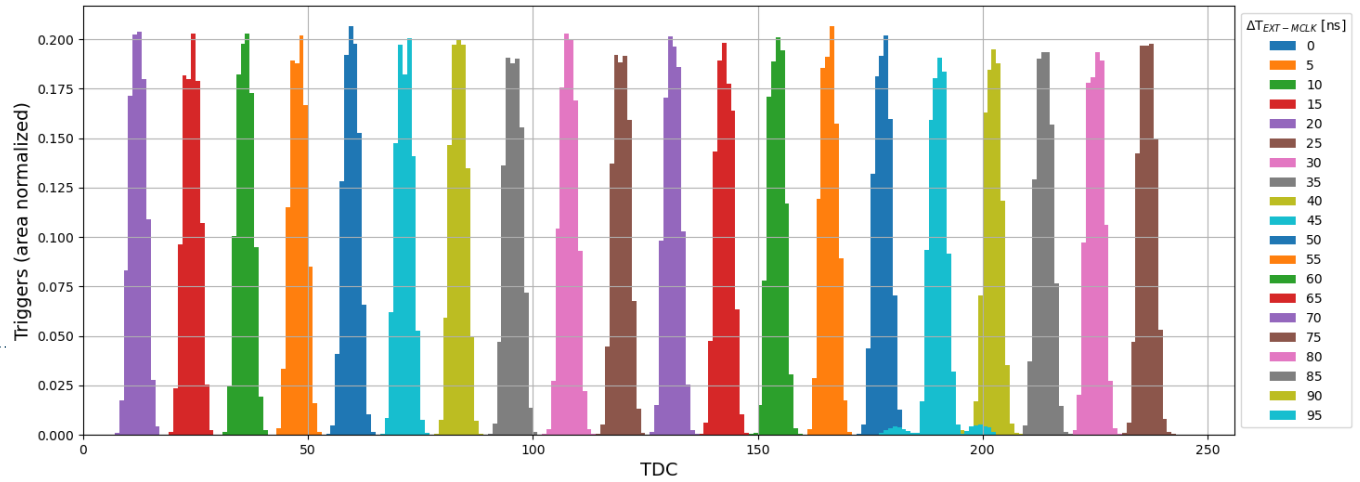
- Linear to <1 ns over the full 100 ns timing range
- < 1 ns jitter
- < 2 ns time-walk bias
- < 1 ns RMS global timing accuracy





LightPix-v2

- Dual TDC/ADC functionality in single ASIC – design complete, awaiting production



TDC output versus test pulse time offset

Summary

LArPix

- Status
  - Successfully produced, qualified, deployed multiple O(100k) channel systems
  - ~1/2 million pixel detector operation in NuMI GeV neutrino beam (2023)
- Near-term R&D focus
  - ASIC
    - Correlated double sampling to improve noise
    - Implement 10-bit ADC to improve charge resolution
  - Anode tile
    - Robustness to microphonics
    - Mitigate far-field induced charge with pixel pad geometry

LightPix

- Status
  - TDC meets design targets
  - Multi-SiPM performance demonstration in-progress
- Near-term R&D focus
  - TDC + ADC functionality in next ASIC version
  - Deployment and testing of light detector system in prototype LArTPC
  - Exploration/optimization of light detector formats