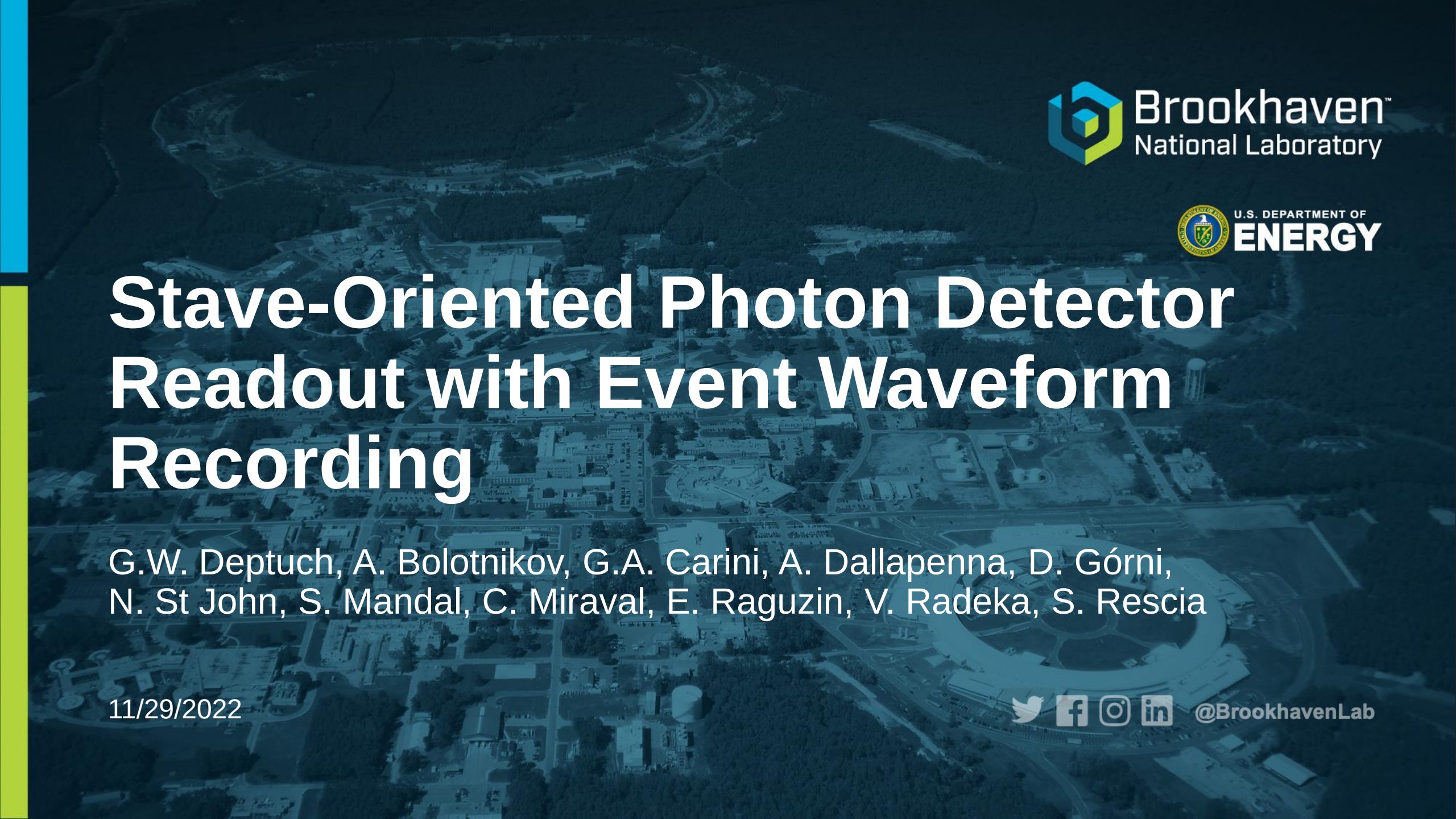

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U.S. DEPARTMENT OF ENERGY

Stave-Oriented Photon Detector Readout with Event Waveform Recording

G.W. Deptuch, A. Bolotnikov, G.A. Carini, A. Dallapenna, D. Górni, N. St John, S. Mandal, C. Miraval, E. Raguzin, V. Radeka, S. Rescia

11/29/2022

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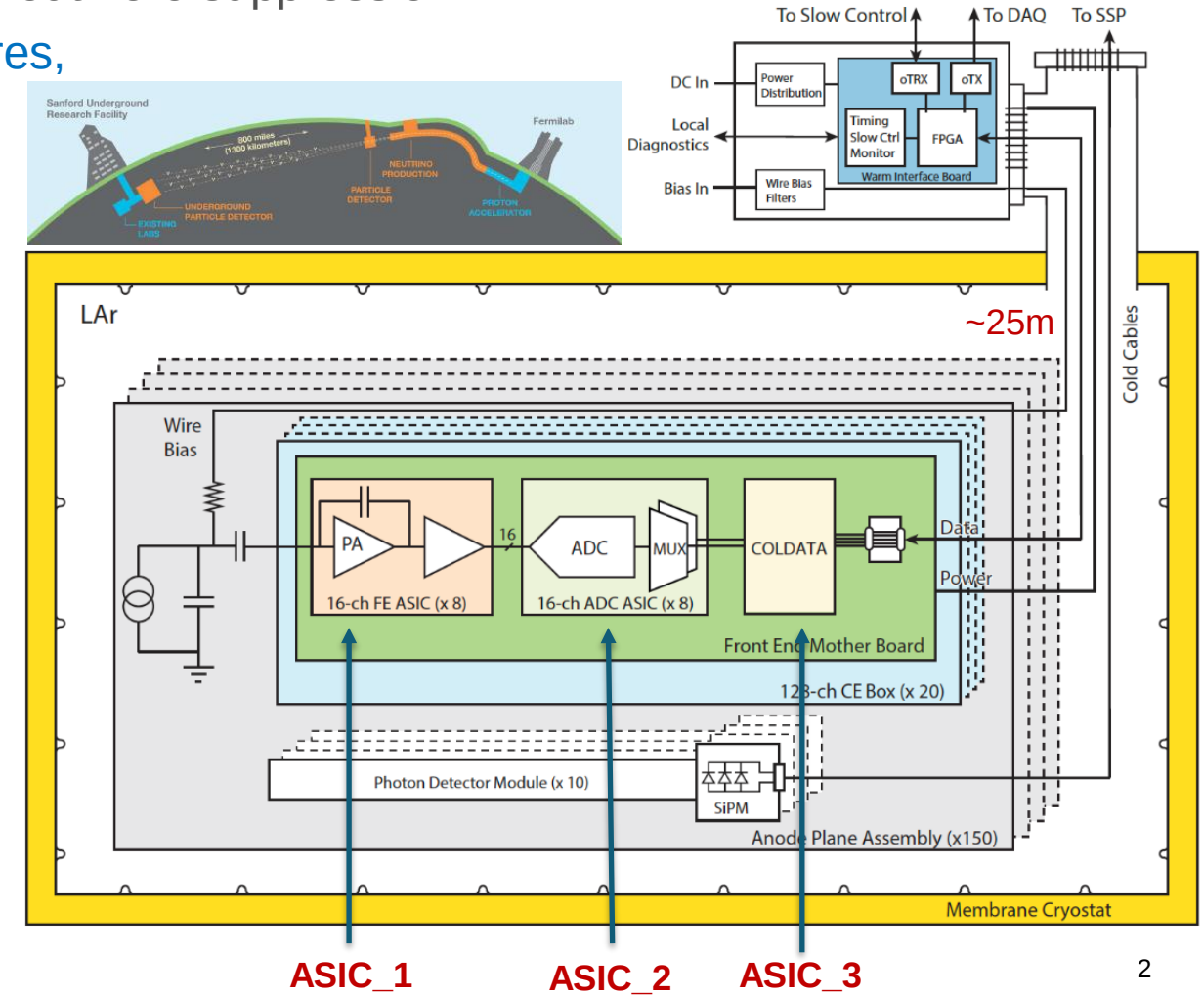
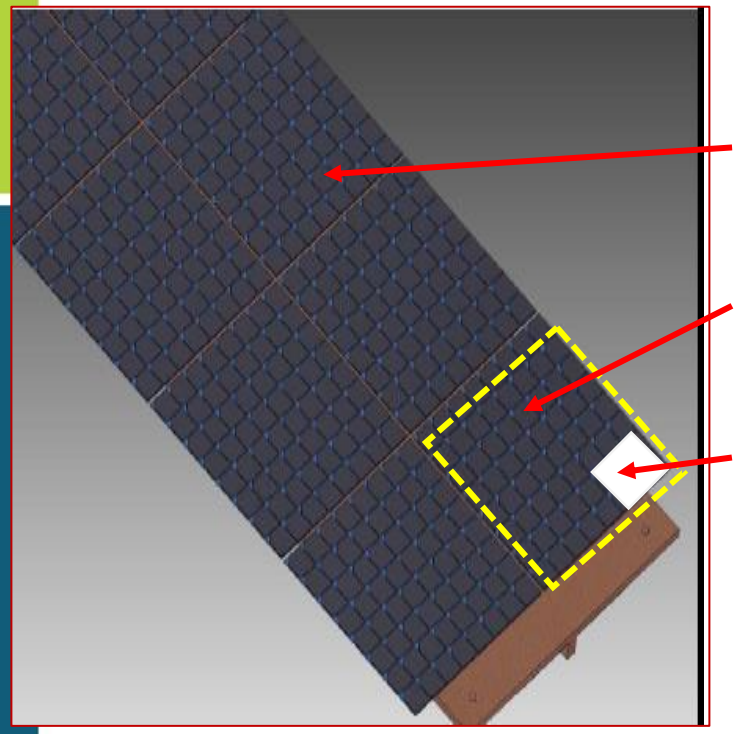
DUNE 3-ASIC lAr TPC Streaming Readout

- Integrated electronics in cryostat (giant TPC with ~5 m drift distance) in liquid Ar (80 K, not accessible for lifetime of DUNE experiment ➲ HCE reliability)
- Waveforms are digitized at 2 MHz and read out without zero suppression
- Electronics circuits are mounted near the sense wires,
  - Amplifier and Shaper 16 channels
  - ADC 16 channels
  - Data Merger and Serializer 2 × 1.25 Gbps
- 3-ASIC readout for DUNE far detector:
  - Front-End: LArASIC (180 nm) by BNL,
  - Time interleaved ADC: ColdADC (65 nm) by LBNL, FNAL, BNL)
  - Data concentrator/transceiver: ColdDATA by FNAL, BNL digital implementation and P&R
- One 10 kTon FD-1HD detector has:
  - 3000 x 128-channel Front End Mother Boards with 24000 x FE ASICs, 24000 x ADC ASICs, 6000 COLDATA ASICs

  Total 12000 1.28 Gbps links (9.2 Tbps of waveform data)



Staves, Tiles, Mini-tiles, SiPMs

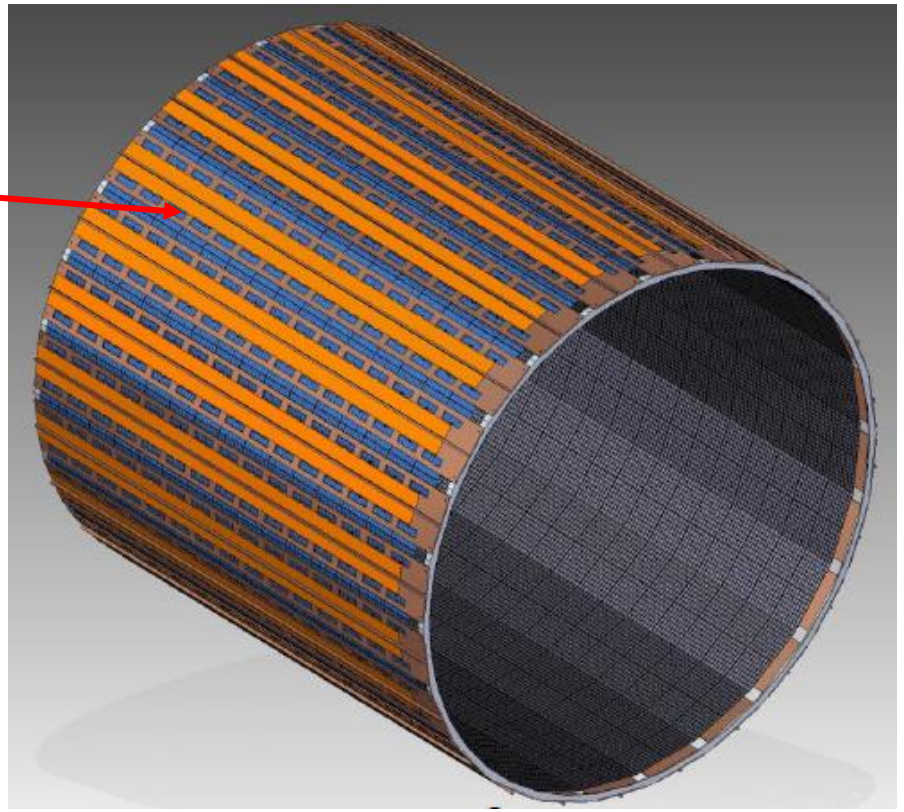


Staves: **24**

Tiles : **24** x 2 x 10 = **480**

Minitiles/subarrays 6 cm^2:
480 x 16 = **7680**

SiPM Area: 7680 x 6 cm^2 ≈4.6 m^2



Technology	"HPK"	"FBK"
C/A [nF/cm^2]	3.5	8.5
V_{op} [V]	60	30
C_{6cm^2} [nF]	**21**	**51**
C_{2s} [nF]	**5**	**12.5**
V_{2s} [V]	120	60

} in series connection

Readout challenge:
Fine segmentation of 7860 SiPM subarrays=electronic channels (<1 p.e./subarray), still results in a "giant" subarray capacitance/channel, **~5-12 nF** in the best case (series connections C_{2s}), and **~20-50 nF** in the worst case (SiPMs in parallel).

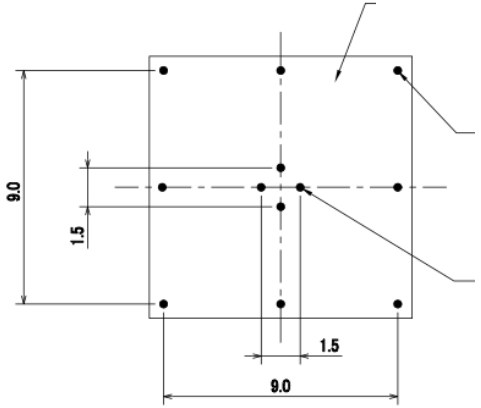
SNR>10 for 1 p.e. essential for nEXO!

Fused silica interposer optimized for HPK SiPM geometry

- Total 96 SiPMs (8×12)
- SiPMs arranged in 4×4 arrays, each consisting of 2×3 subarray (2s3p)
- 0.2 mm gaps between SiPMs
- 16 readout channels
- UV SiPM is “p-on-n” type device with anode at window side

Bonding pads on a new Hamamatsu S16483 ATS device

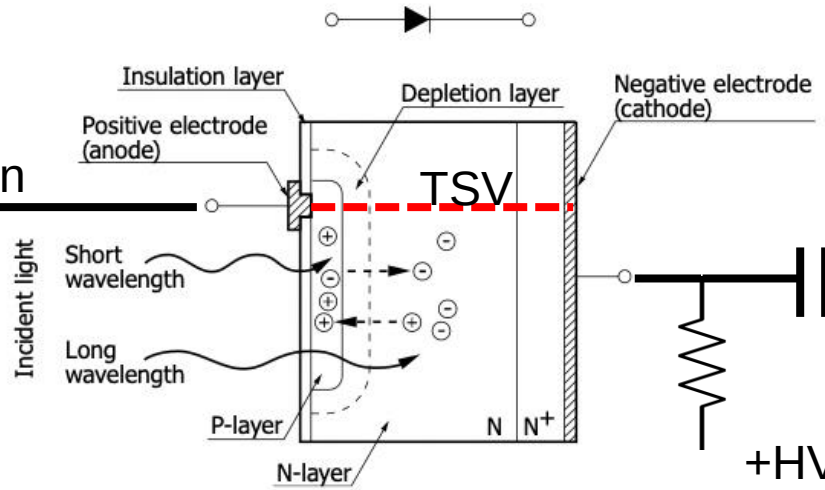
10.1x10.1 mm^2 chip



Cathode (bottom side) pads

Anode (window side) pads

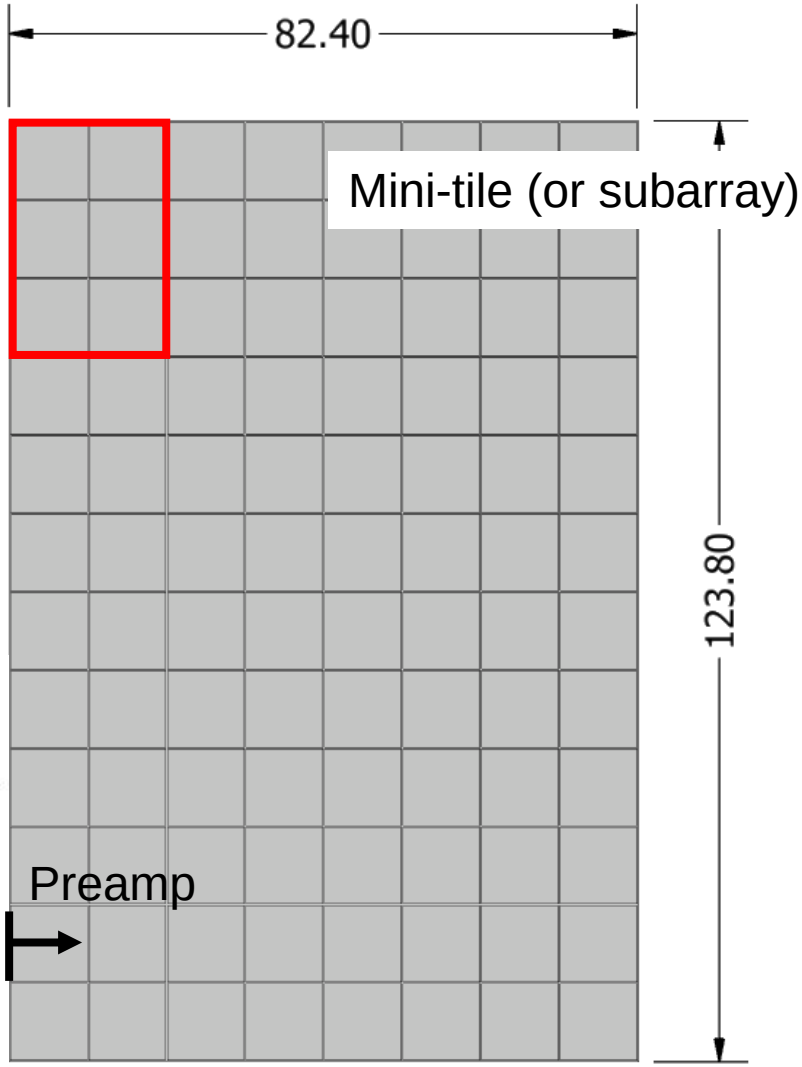
Common



Preamp

+HV

Tile (top view)



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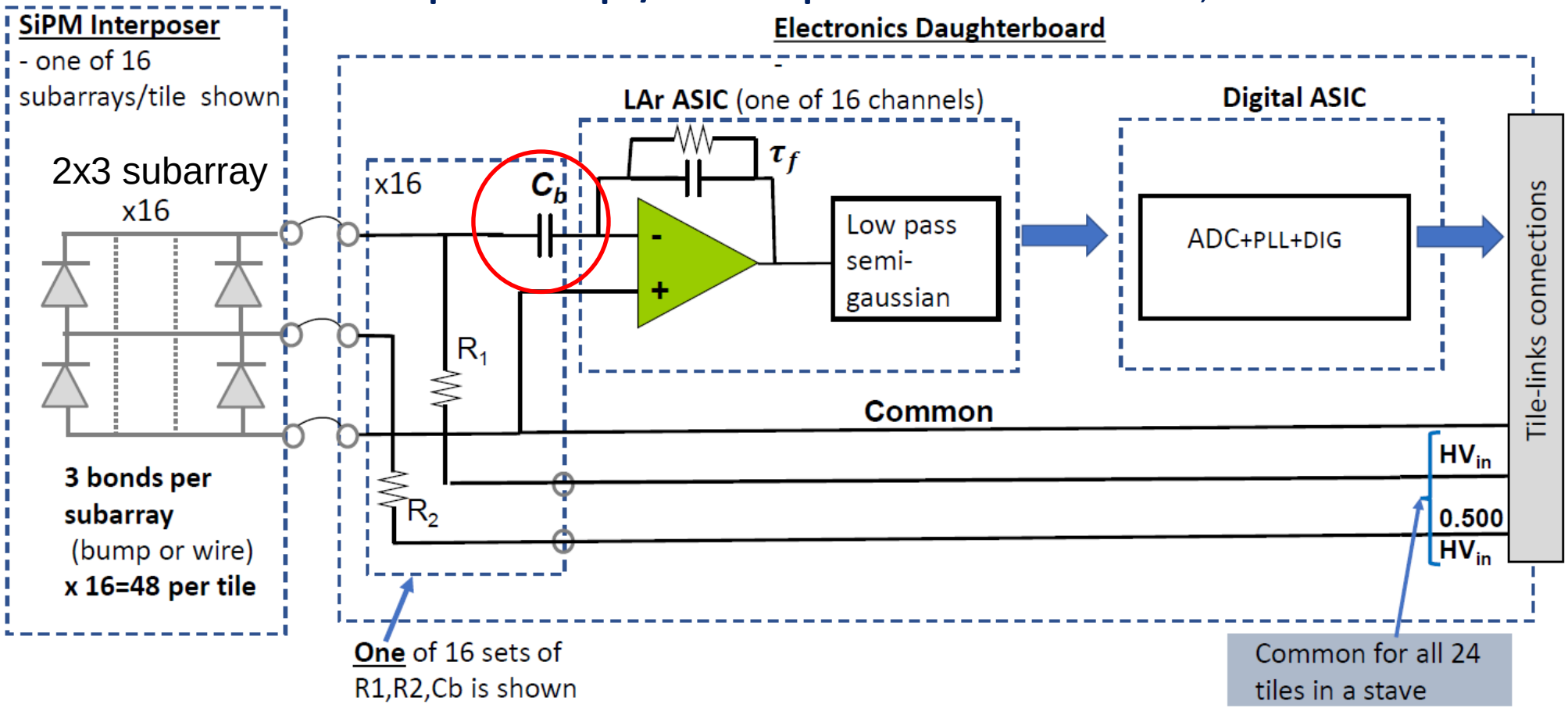
Readout architecture and extraction of signal from the large capacitance SiPMs

Integration of SiPMs and PRE: Weak Coupling of SiPM and electronic readout: $C_b << C_d$

Radiopure 500 pF/100 V capacitor easier to realize, and lower risk than 50 nF/100V;



Calibration and diagnostics of electronics independent of SiPM capacitance, bias and condition (open or short).

Small C_b allows higher inductance interconnections.

In situ SiPM array capacitance measurement

PRE TDR: Fig. 10.4.2. Tile readout with all active electronics on daughter board

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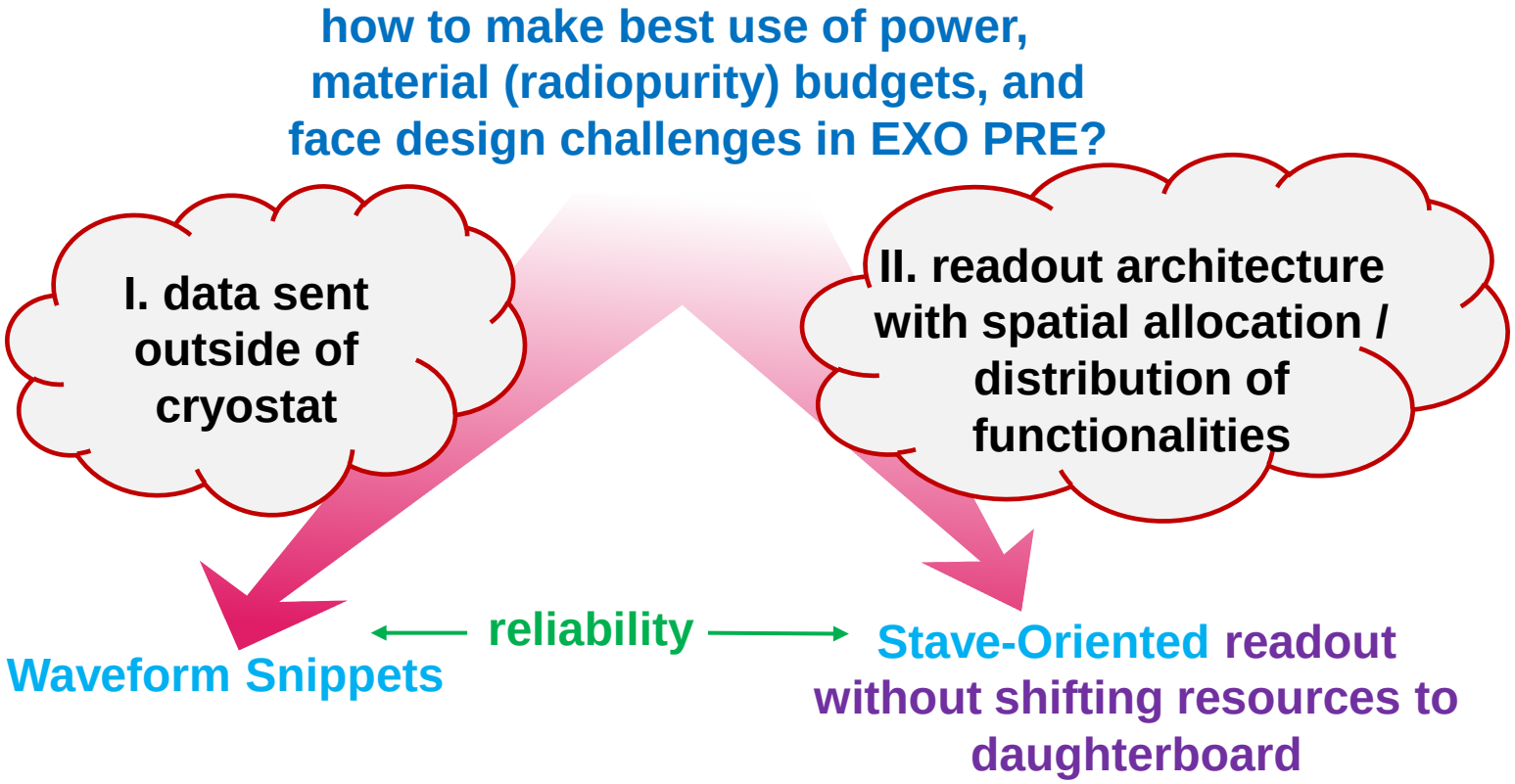
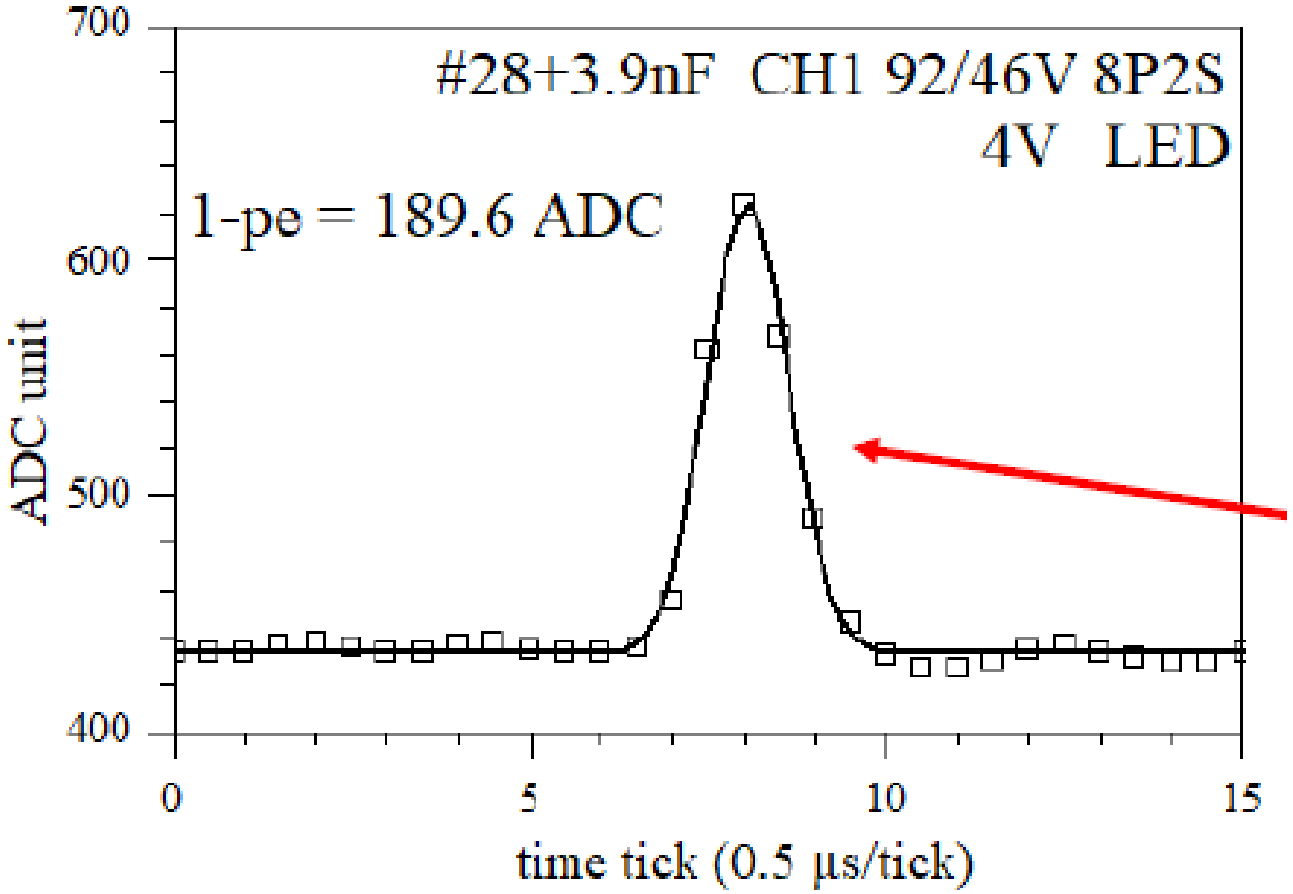
Introduction of WSSO



Waveform Snippet and Stave-Oriented = WSSO scheme

WSSO - illustration



Waveform acquired with the SiPM + FE(LArASIC) to show system proof-of-concept.

Information about single p.e. is fully captured by a '*snippet*' of samples (30 samples shown):

- avalanche = 0.4 pC at OV = 4 V
- 1-p.e. *S/N* ~60;
- 1-p.e. *coincidence resolution* between two subarrays < 20 ns

Recipe of WSSO

elimination of sending
continuous stream

Waveform Snippets

parts of digitized time sequences containing
pre-signal÷signal÷post-signal
samples

- the filtered FE signal is continuously sampled and digitized, exactly as for data-streaming (τ_p=1 μs and 2 MSps).
- the data are examined for events (signals larger than ½ *p.e.*), and then a ***snippet of samples*** (waveform snippet WS) is retained.
- WSs contain a small number of samples of each signal and the baseline before and after the event (*20 - 32 samples, equivalent to 10 -16 μs, may be sufficient*).
- each WS is identified through time stamp and channel number for identification.

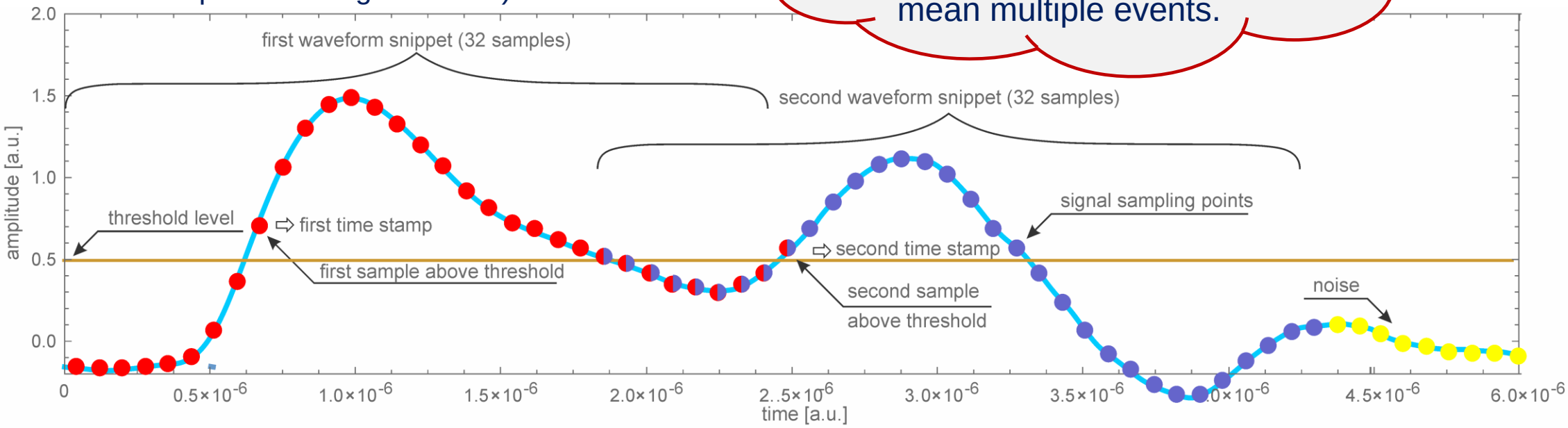
WSSO - protocol

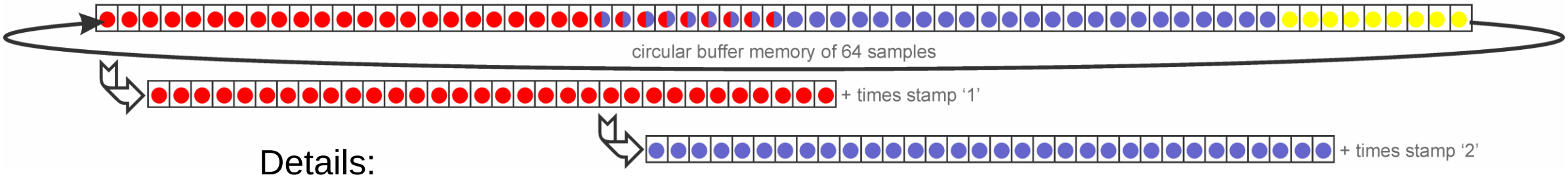
Example of WS extraction

(assuming WS length = 32 samples and single samples crossing threshold)

Are data lost if multiple threshold crossings? **NO**

more than one threshold crossing in one length of WS may mean multiple events.





Details:

- how many samples need to go above/below threshold to register WS and new WS,
- definition to time stamp, length of WS, etc.

can be decided and programmed in an-on-ASIC WS registration protocol

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WSSO v.s. streaming data rates

assumption of max DCR and calibration rate = **4×10^3 events/s (per channel)**

Per Tile:

WS: snippet size [32 samples] × event rate [4×10^3 events/s] × ADC resolution [12 b] × # channels/minitiles [16] ≈ **24.6 Mbps/tile**

v.s.

Streaming: [ADC conv. rate] 2 MSps × ADC resolution [12 b] × # channels/minitiles [16] = **384 Mbps/tile**

Per Stave:

WS: tile data rate [24.6 Mbps] × # tiles [20 tiles/stave] ≈ **491.6 Mbps/stave**

v.s.

Streaming: tile data rate [384 Mbps] × # tiles [20 tiles/stave] ≈ **7.68 Gbps/stave**

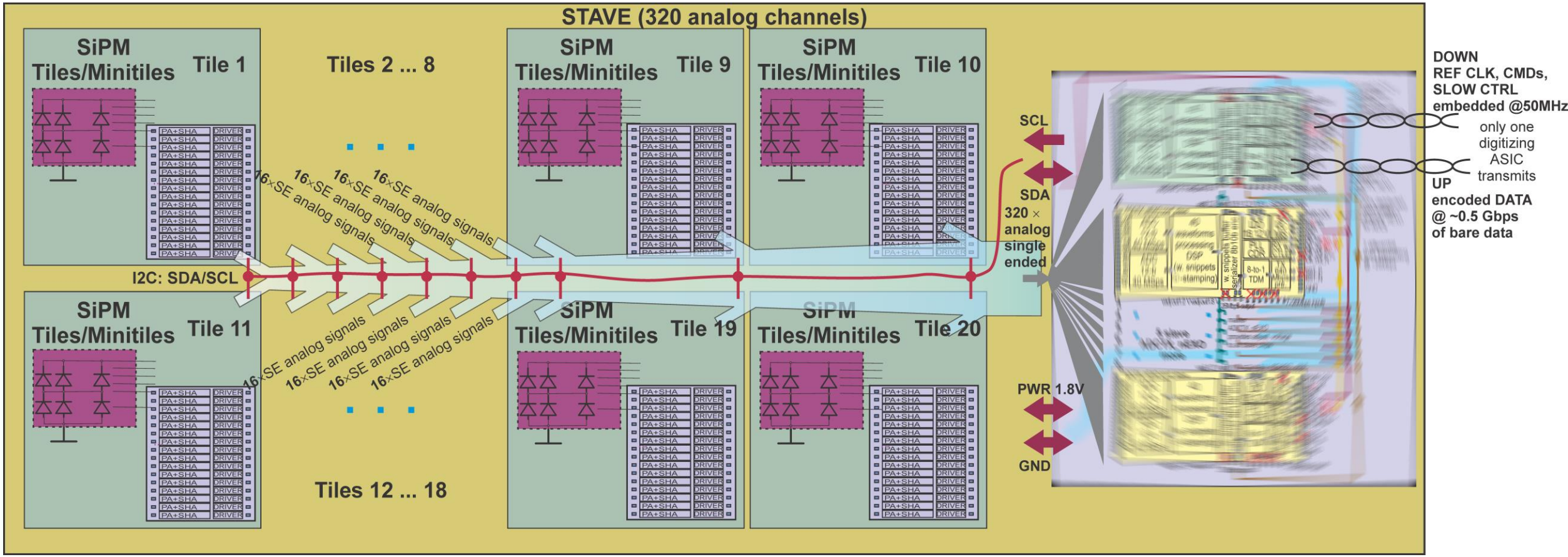
Total:

WS: stave data rate [491.6 Mbps] × # tiles [24 stave] ≈ **11.8 Gbps**

v.s.

Streaming: stave data rate [7.68 Gbps] × # tiles [24 staves] ≈ **184.3 Gbps**

Concept of WSSO



power regulation on tops of staves: two power for ADCTX_nEXO ASIC one power distributed down to FE_nEXO ASIC,

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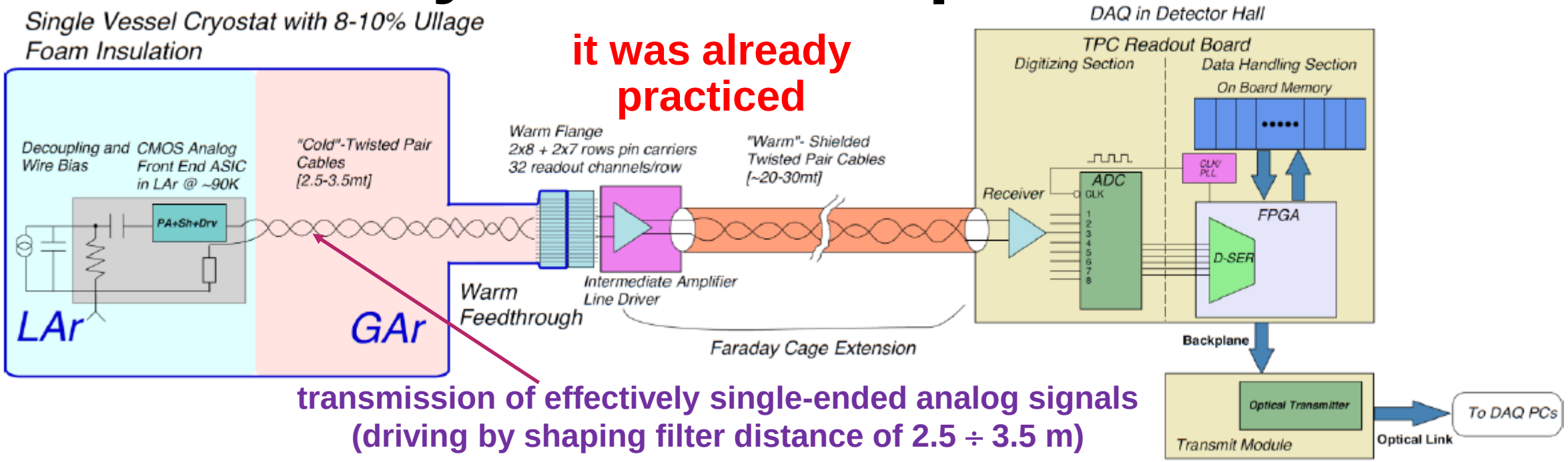
Is SO entirely new and unproven?



it was already practiced

transmission of effectively single-ended analog signals (driving by shaping filter distance of 2.5 ÷ 3.5 m)

Could all analog lines be driven outside to external ADCs in nEXO?

it is not a good idea, as among other troubles, it would require 7680 analog lines be driven through feedthrough

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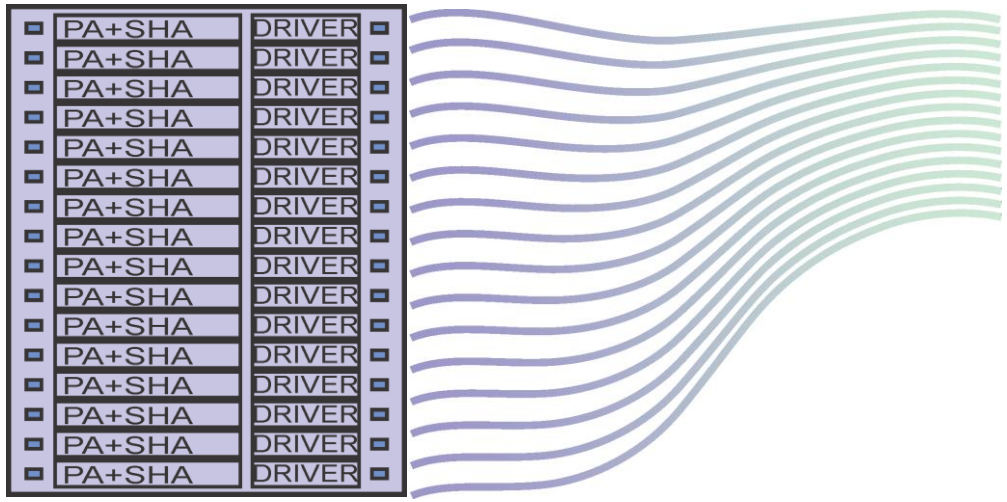
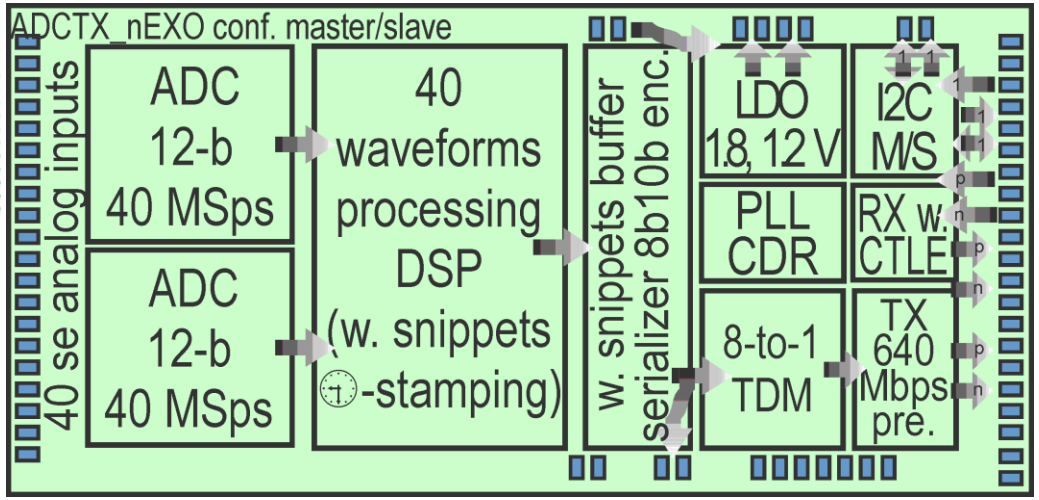
The MicroBooNE TDR (2/24/2012-DocDB 1821-v12): Electronics/Data Acquisition (WBS 1.5/1.9)

ASICs in WSSO

ASICs: FE_nEXO



ADCTX_nEXO



Location: Daughter Board

Location: Top of Stave instead of Daughter Board

Single-ended (SE) analog waveforms

Recipe of WSSO

provide interface to stave with reduction of **20** data cables from stave to transition box to **1** cable

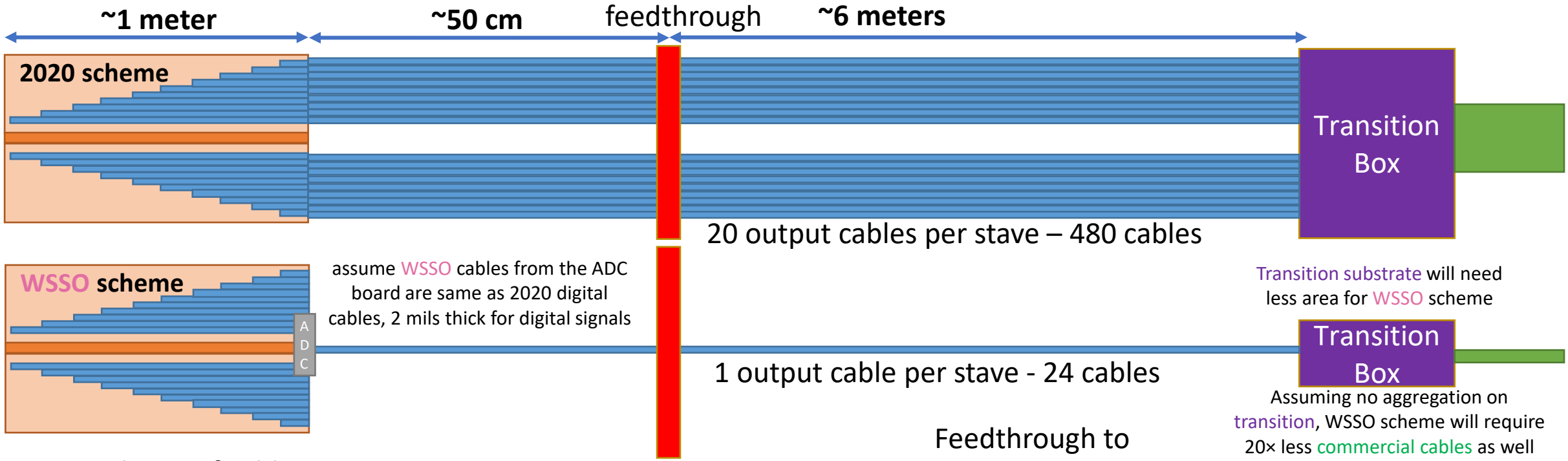
Stave-Oriented readout

optimal allocation of electronics functionalities, cabling and mechanics

- optimal placement of ASICs in 2-ASIC readout solution,
- more than 10 × reduction of data cables = easier and more reliable mechanics of feedthroughs,
- improving radiopurity through reduction of polyimide volume,
- no distribution of digital signals across staves, and easy handling of slow-control,
- less components (decoupling capacitors on daughter boards) and lighter power distribution,
- achieving modularity, reconfigurability and suitability for testing as stave is one self-contained subsystem block,
- makes stave possible for testing in laboratory and includes test modes :
  - taking empty (not containing thresholded data) waveform snippets (tacking baseline/low freq. noise),
  - allowing streaming one selected channel without applying any threshold.

Questions for SO (1)

material budget and radiopurity comparing 2020 with WSSO



Scheme	Funnel part of cable Volume (cm^3)	Funnel part of cable Mass (g)		Top of stave to feedthrough Volume (cm^3)	Top of stave to feedthrough Mass (g)		Feedthrough to Transition Box Volume (cm^3)	Feedthrough to Transition Box Mass (g)		Total Taiflex Cable Volume (cm^3)	Total Taiflex Cable Mass (g)
2020	106.02	150.54	+	64.25	91.24	+	771.02	1094.85	=	877.04	1245.39
WSSO	89.86	127.59		3.21	4.56		38.55	54.74		128.41	182.33
	15% less			95% less			95% less			85% less	

Questions about SO (2)

cross-talks between single-ended analog lines

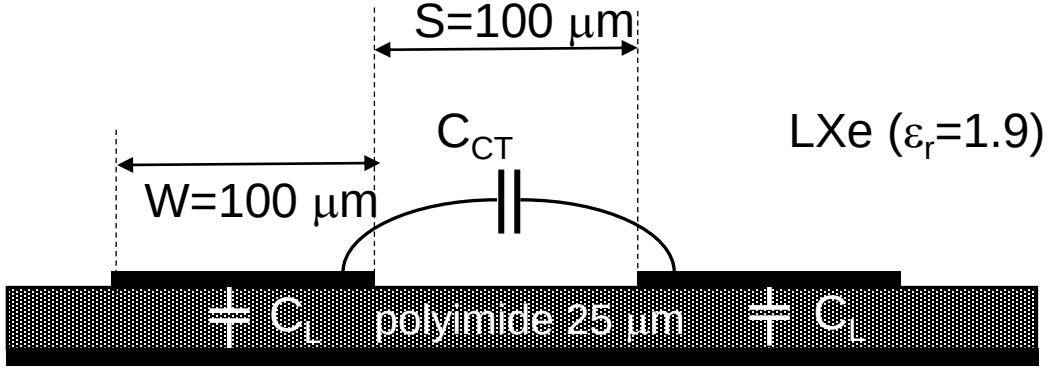
signal lines: 100 μm (4 mil) width / 100 μm (4 mil) spacing

conductor: 0.5 oz Copper, thickness = 17 μm (0.67 mil)

dielectric: Kapton, thickness = 25 μm (1 mil)

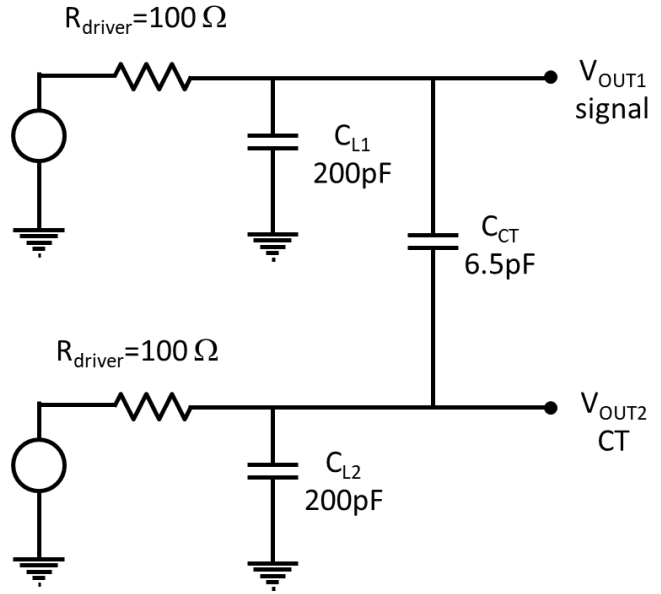
ground plane: 0.5 oz Copper under signal traces

bandwidth of transmitted signals is limited < 300 kHz

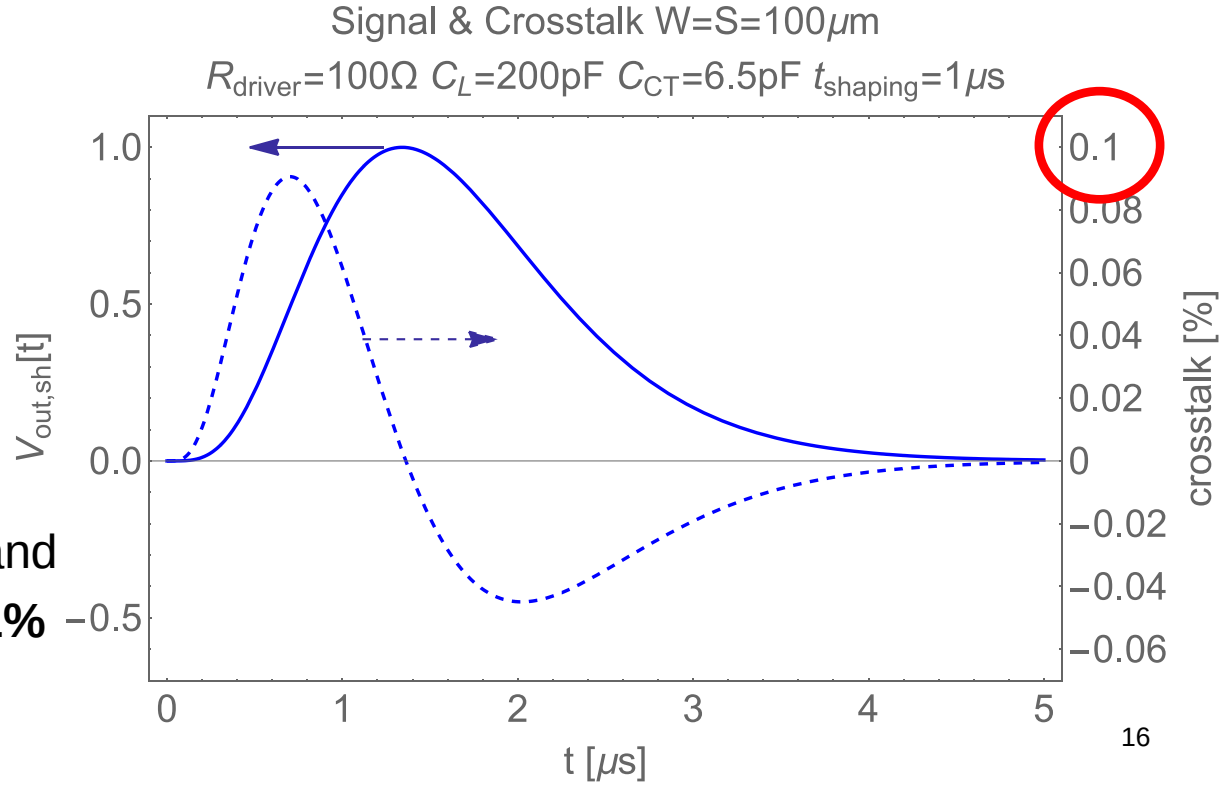


LXe (ε_r=1.9)

capacitive coupling (dependent on the driver's output- and receiver's input resistance) can be maintained **below 1%**



lumped elements equivalent circuit



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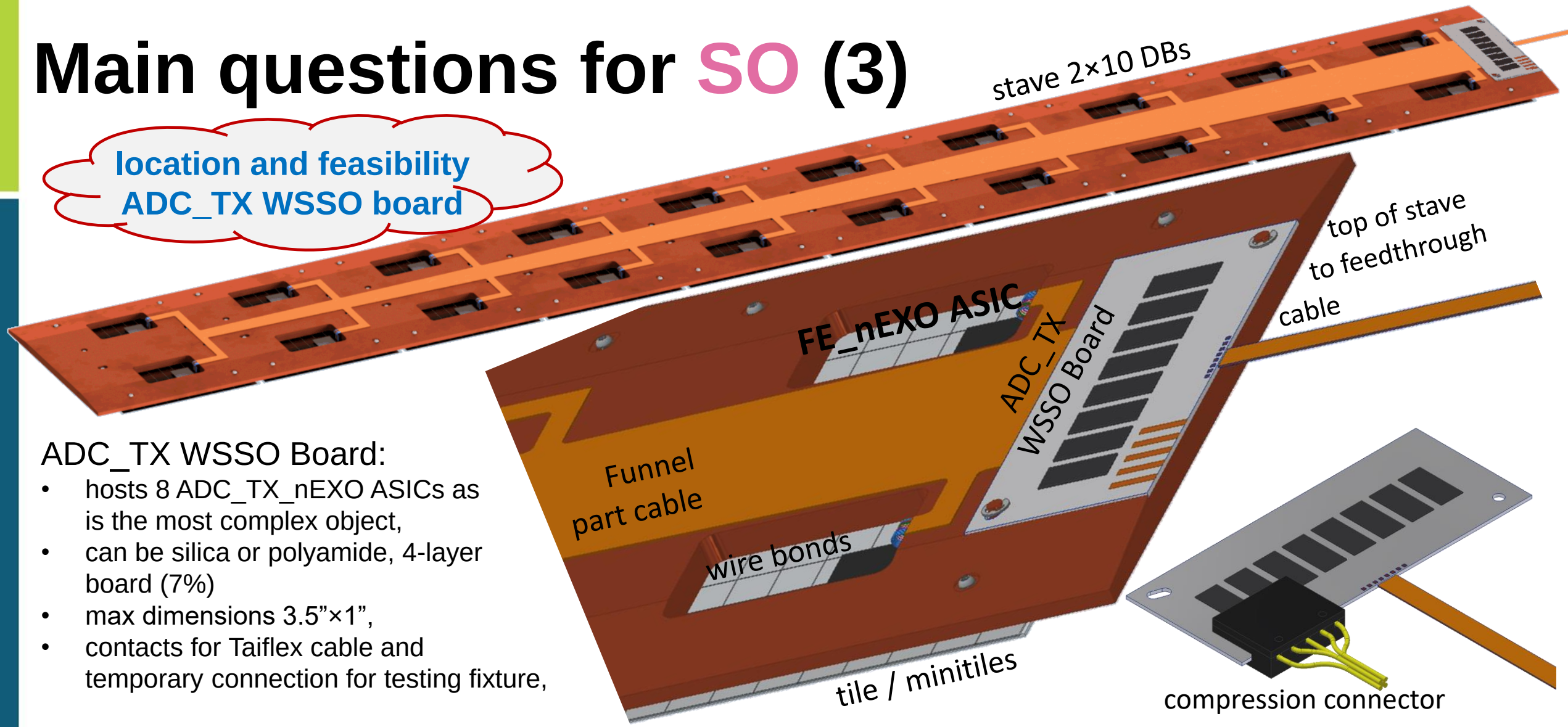
Main questions for SO (3)

location and feasibility
ADC_TX WSSO board

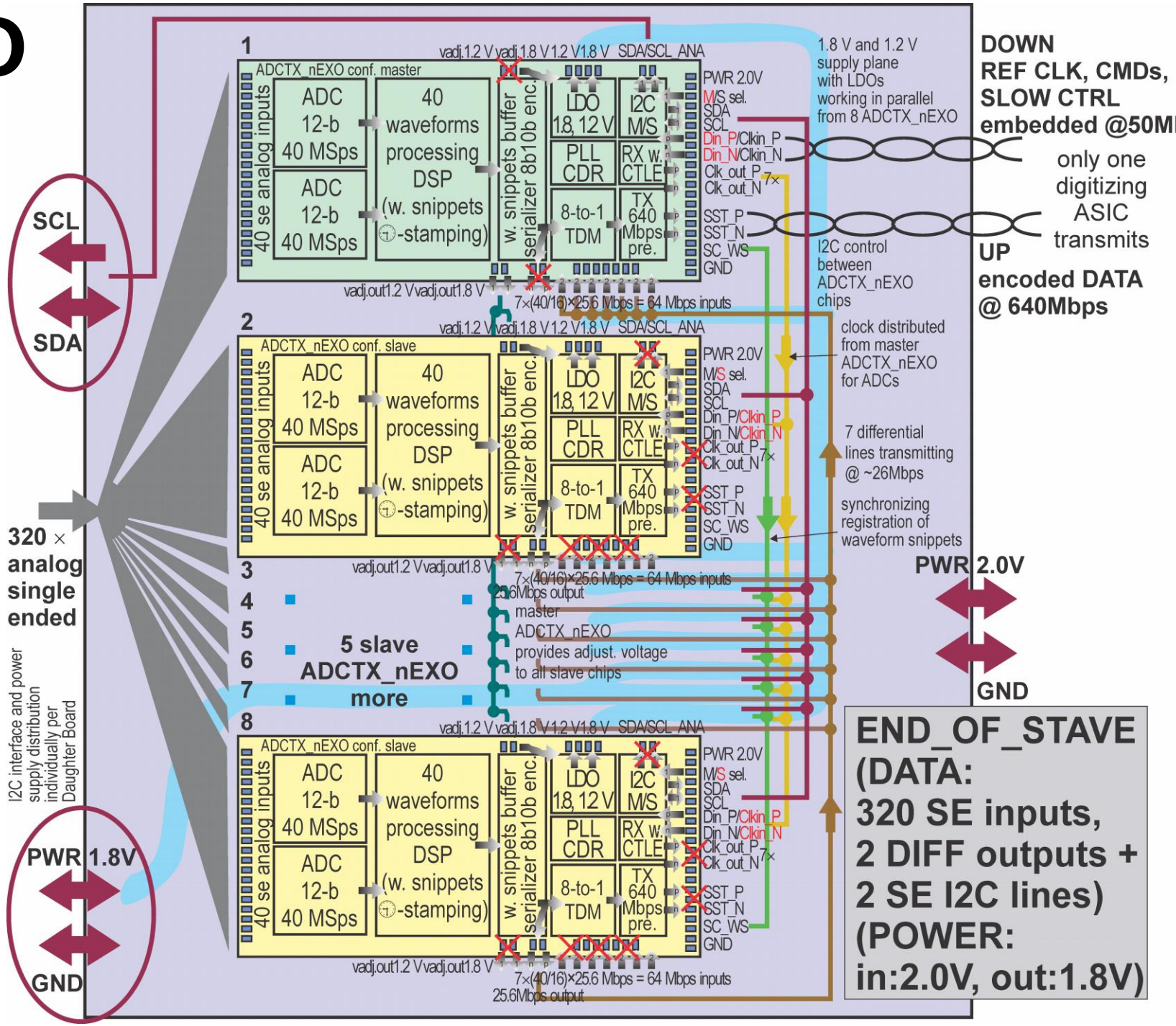


ADC_TX WSSO Board:

- hosts 8 ADC_TX_nEXO ASICs as is the most complex object,
- can be silica or polyamide, 4-layer board (7%)
- max dimensions 3.5”×1”,
- contacts for Taiflex cable and temporary connection for testing fixture,

ADC_TX_nEXO ASIC Board

- 320 analog input channels split into 8 ADC_TX_nEXO ASICs,
- each ADC_TX_nEXO ASIC is identical,
- only one *master* is required per stave,
- *master* ADCTX_nEXO ASIC recovers clock,
- *master* synchronizes all ADC_TX_nEXO ASICs,
- two loops of slow control,
- voltage regulation for 1.2 V (digital) and 1.8 V (all analog)



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Principal points of WSSO

- The Waveform Snippet and Stave-Oriented (WSSO) scheme will provide all the signal generated by SiPMs with a record for all events, at a significantly lower data rate, caontrasting to the original concept, where:
  - *the baseline samples contain information about nothing but noise,*
  - *480 data cables transfer 24 cables-worth signals.*
- WSSO provides a reduction in the number of low dispersion cables and their connections by an order of magnitude or more, a reduction in the amount of potentially background contributing material, a simplification of the feedthrough design and lower cost, etc.
- WSSO improves reliability, making feedthroughs less prone to disconnect or get damaged.
- WSSO scheme makes the staves into self-contained objects simplifying testing of the staves and assembly into the cryostat.

Reserve Slides

Comparison of readout schemes

Readout Scheme	1) Continuous sampling with waveform recording -- "data streaming"	2) Continuous sampling with "WS data recording"	Comments on 1)	Comments on 2)
Data rate / tile @ 2MSps 12-bit ADC	384 Mbps	24.6 Mbps (32 samples per WS)	-	-
Number of low dispersion data links	**480 cables**	**24 or 48 cables**	Critical connections on each tile	Critical connections on each stave
Daughter board design	entire analog and ADC + digital + data transfer circuits and LDOs	FE ASIC on the board; ADC + digital + data transfer and LDOs are integral for each stave	Location: daughter board	Location: top of stave
Power dissipation location	100% on daughter boards	1/3 on daughter boards; 2/3 on top of stave	2 powers on DB	1 power on DB
Location of ASICs	on daughter boards	FE ASIC on daughter board; ADC-digital ASIC on top of stave		
Location of V_{DD} capacitors	100% on daughter boards	1/3 on daughter boards; 2/3 on top of stave		

nEXO ADC

SysADC_P1

Low-power, 12-bit, hybrid ADC design in 65 nm CMOS:

Overall: 8-bit SAR (MSB) + 5-bit digital slope (LSB),
SAR/digital slope boundary uses 1 redundant bit for robustness, thus resulting in 12-bit resolution.

Asynchronous successive approximation (SAR) converter:

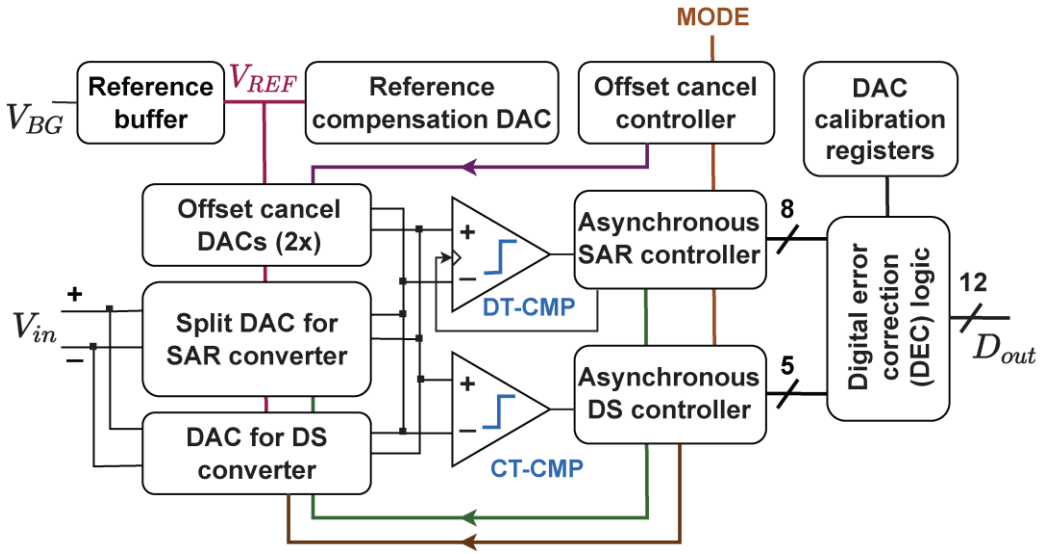
Fully-differential charge redistribution architecture,
Split capacitor DAC using low-power merge-and-split switching,
Uses one redundant conversion cycle for robustness.

Asynchronous digital slope (DS) converter:

Asynchronous low-power delay line-based architecture,
DS capacitors are laid out within the SAR DAC to minimize gain mismatch and simplify calibration.

- Additional features:

On-chip reference buffer w/ cancellation of switching transients,
On-chip digital calibration of comparator offset; supports off-chip calibration of DAC capacitor mismatch.



Preliminary performance specifications

Parameter	Value
Sampling rate	Up to 50 MS/s
Output resolution	12-bit
Full-scale voltage	1.7 V_{pp}
Effective no. of bits (ENOB)	11.0
Core power (at 50 MS/sec)	820 µW
Reference buffer power	1.15 mW
Walden FOM (including buffer)	19.5 fJ/bit

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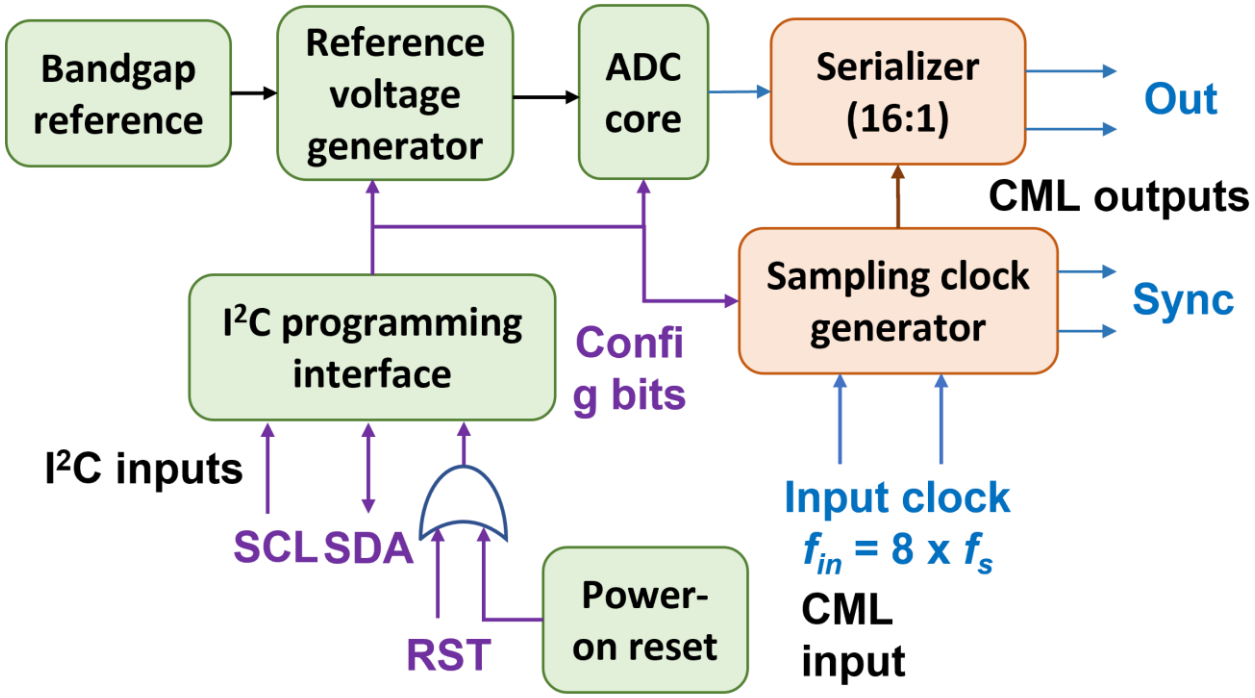
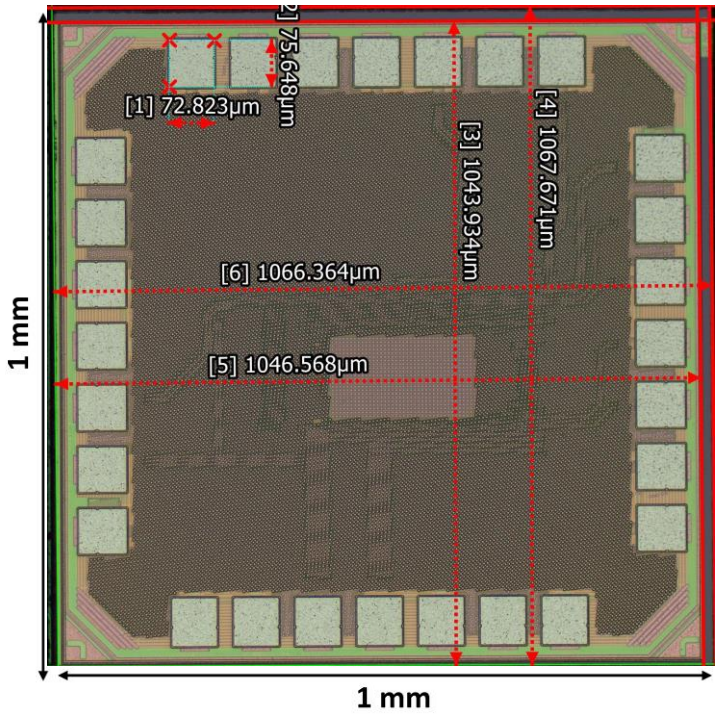
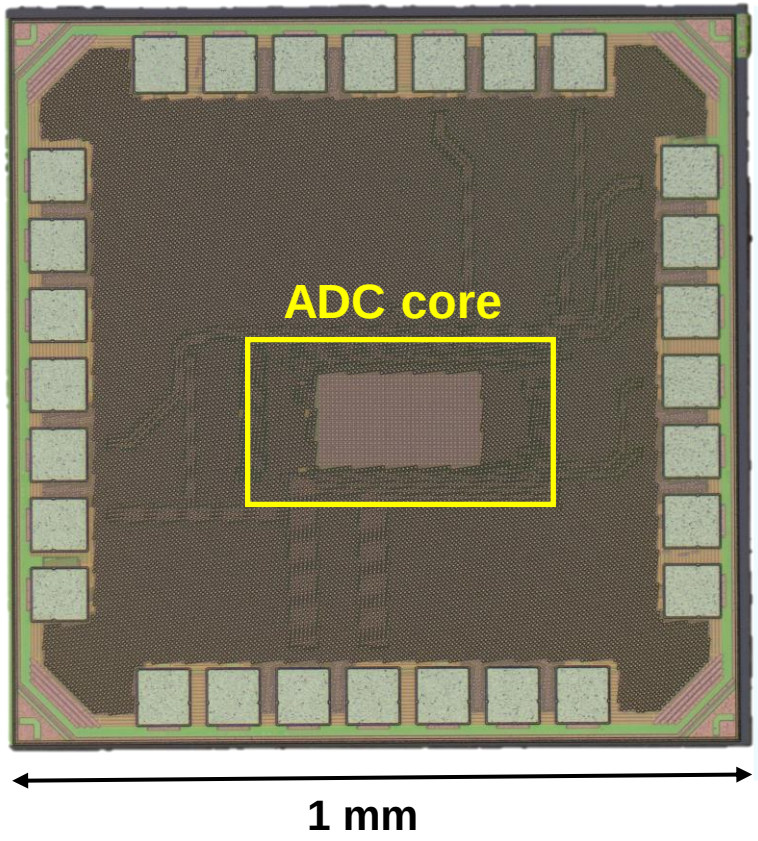
nEXO ADC

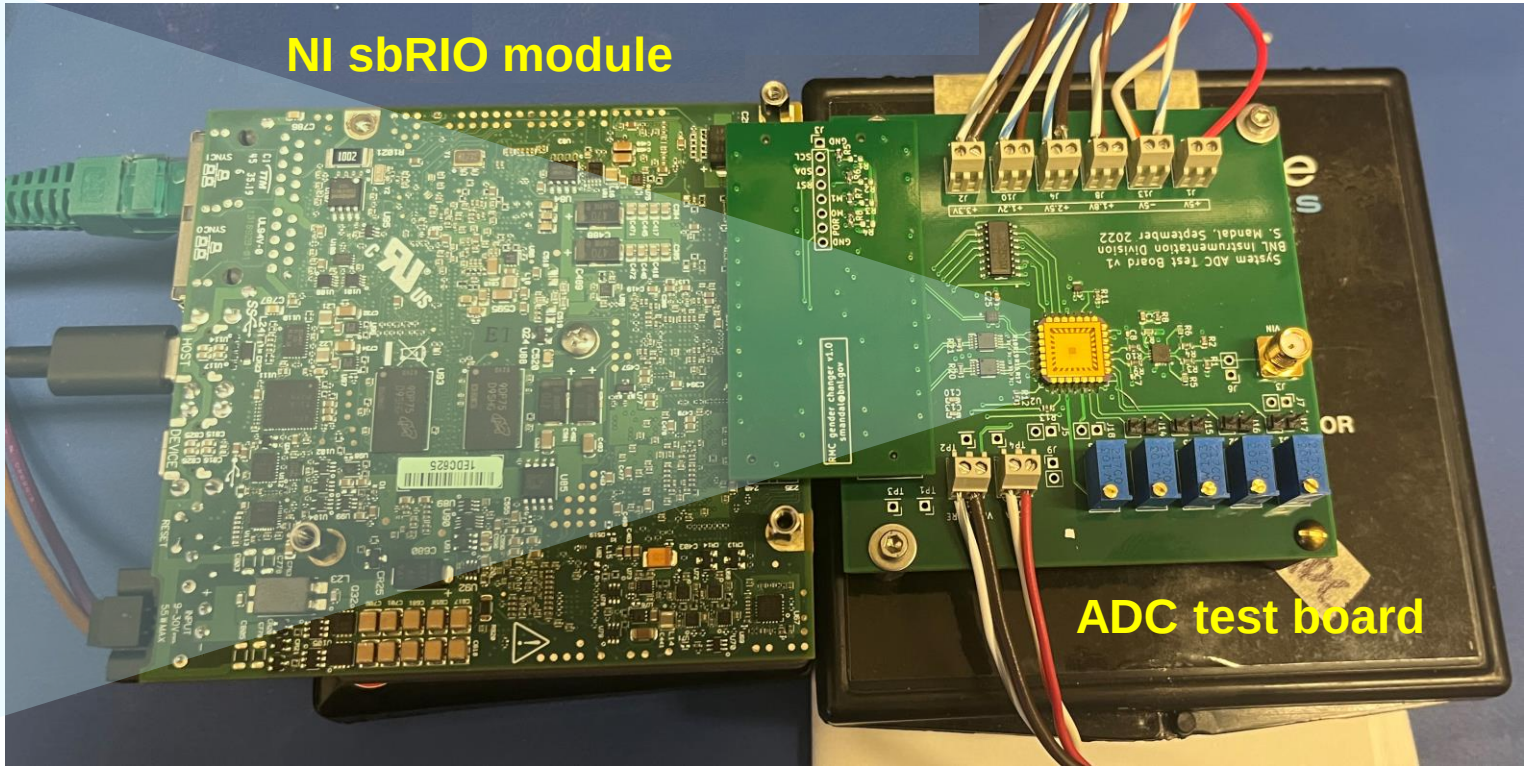




- The 1 mm^2 test chip integrates the ADC with accessory circuits (band-gap voltage reference, clock receiver, sampling clock generator, output serializer, serial programming interface, and power-on reset),
- Layout area of the ADC core (not including reference buffer) = 320 µm x 160 µm,
- Chip was submitted for fabrication in the TSMC 65nm CMOS LP 1P9M process in June (testing is underway).

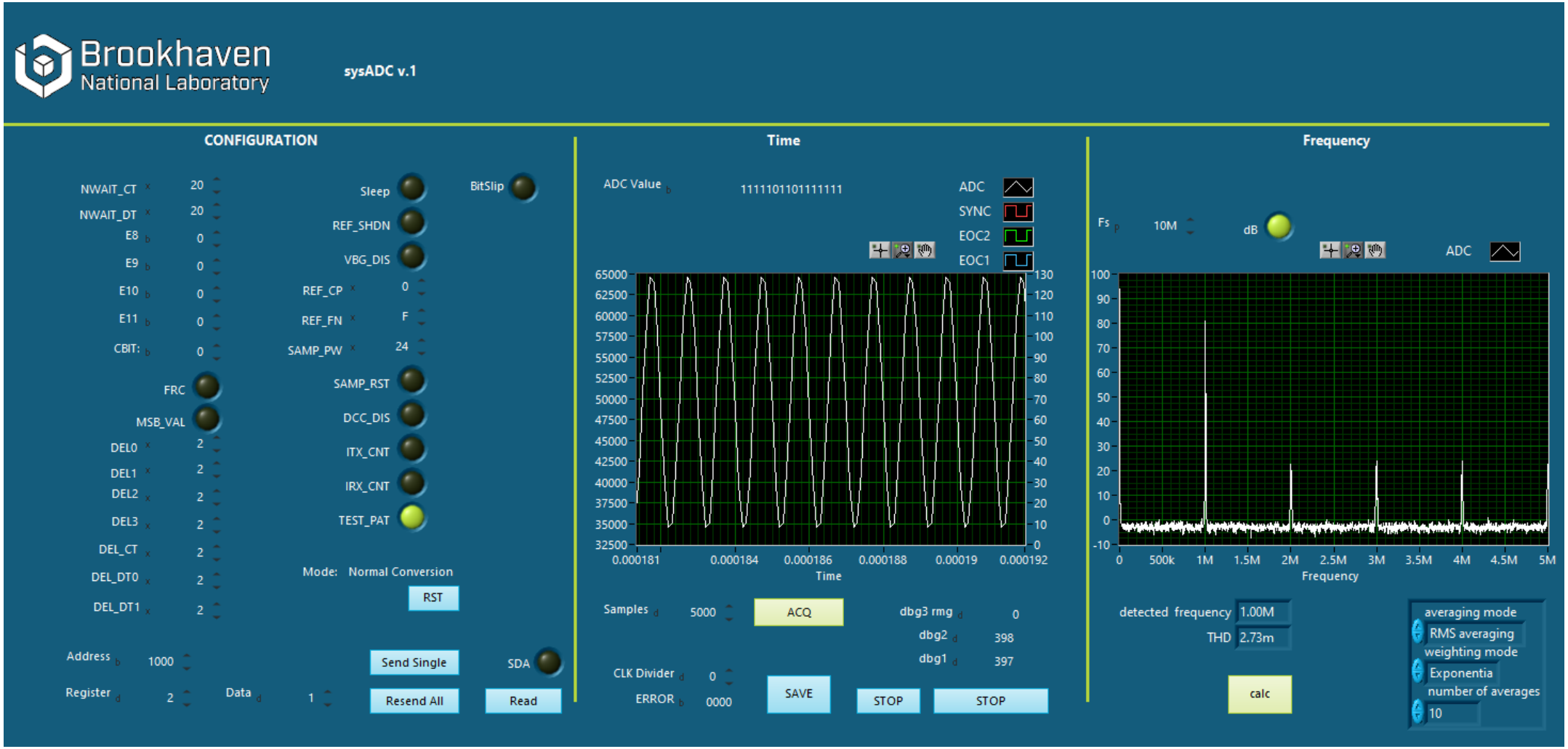
ADC test setup





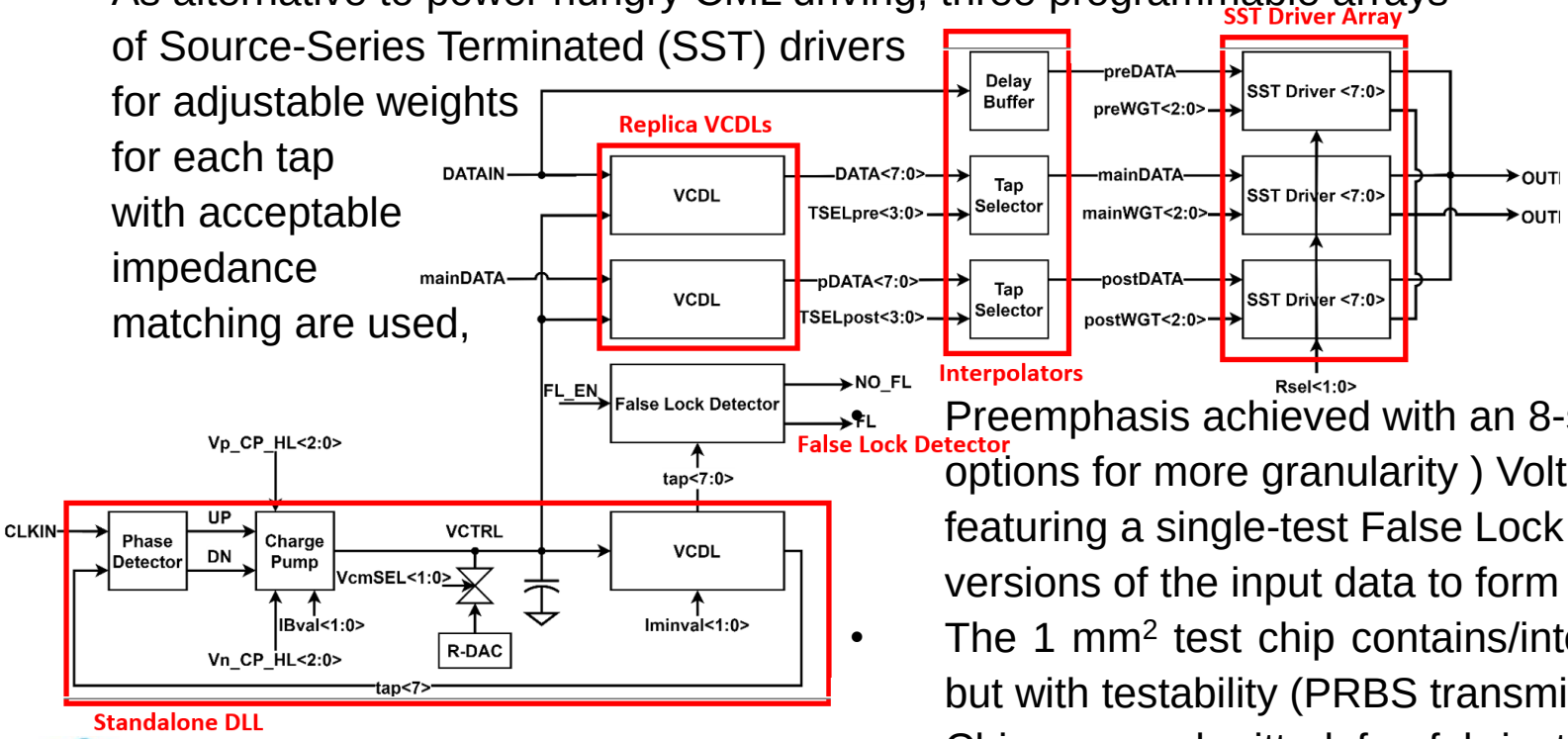
- The ADC test board includes a low-noise, low-distortion, high-slew-rate ADC driver (ADA4927) that also performs single-ended to differential conversion.
- The board also contains digital level translators (1.2V / 2.5V) for the ADC outputs and I^2C signals.

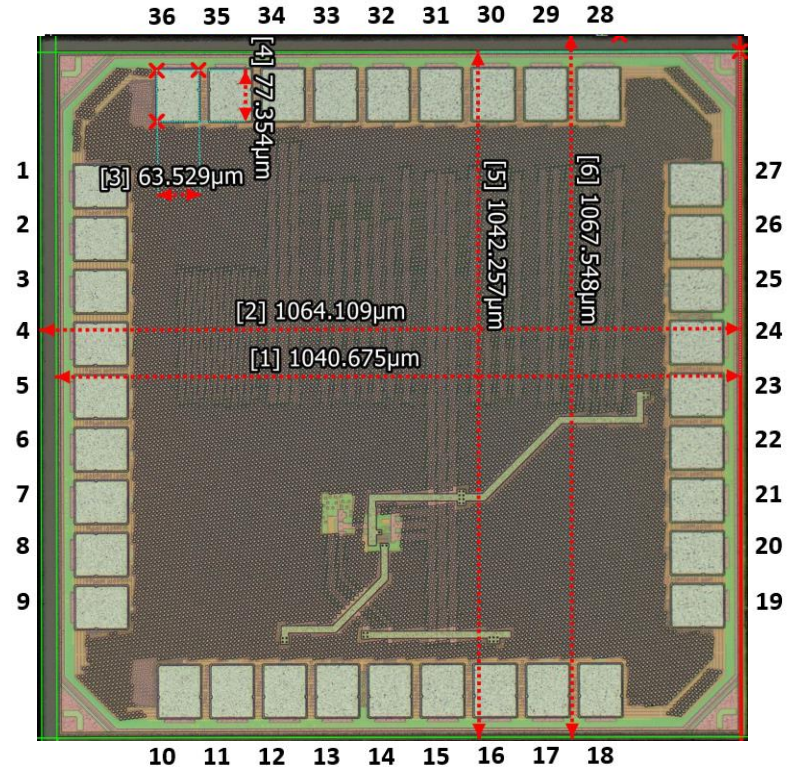
Test GUI (developed in LabVIEW)



nEXO Line Driver

- **PELnDrv_P1**
  - Low-power line drivers tailored to the application to effectively drive the desired cable in a power-efficient manner,
  - Non-conventional method of generating pre-emphasis (*patent pending*) developed for lossy transmission cables such as the one radiopure cable used for the nEXO experiment,
  - As alternative to power hungry CML driving, three programmable arrays of Source-Series Terminated (SST) drivers for adjustable weights for each tap with acceptable impedance matching are used,





Preemphasis achieved with an 8-stage (digital Interpolators allow 16 delay options for more granularity) Voltage-Controlled Delay-Locked Loop (DLL), featuring a single-test False Lock Detector, where replicas create delayed versions of the input data to form pre-emphasised stream,

- The 1 mm^2 test chip contains/integrates the full line driver without serializer but with testability (PRBS transmission data generator),
- Chip was submitted for fabrication in the TSMC 65nm CMOS LP 1P9M process in June (expected in August), efforts started to handle testing.

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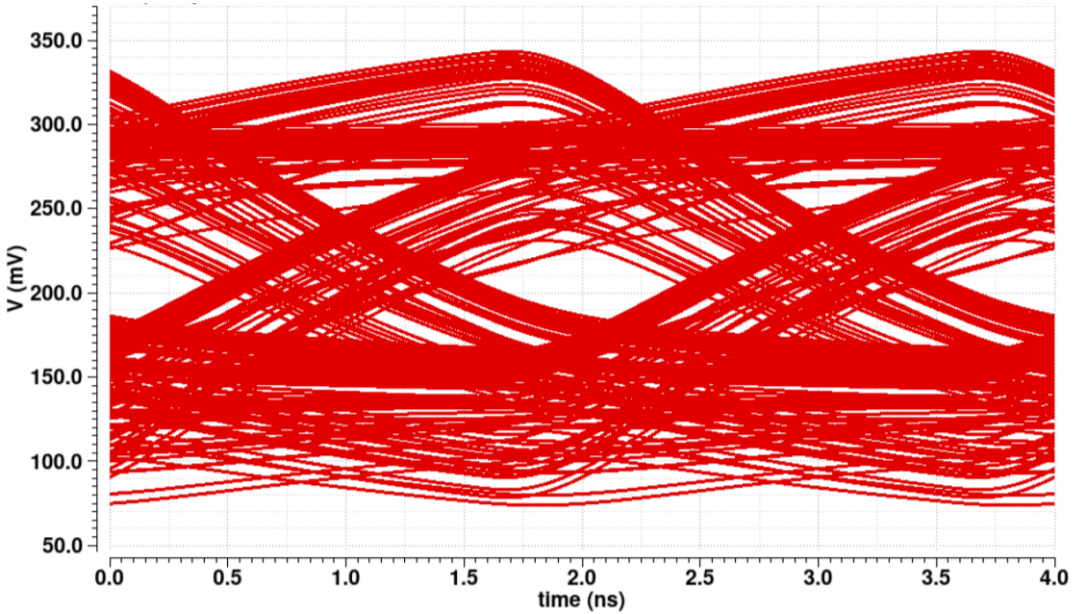
nEXO Line Driver

Regular Line Driver (no Pre-Emphasis):

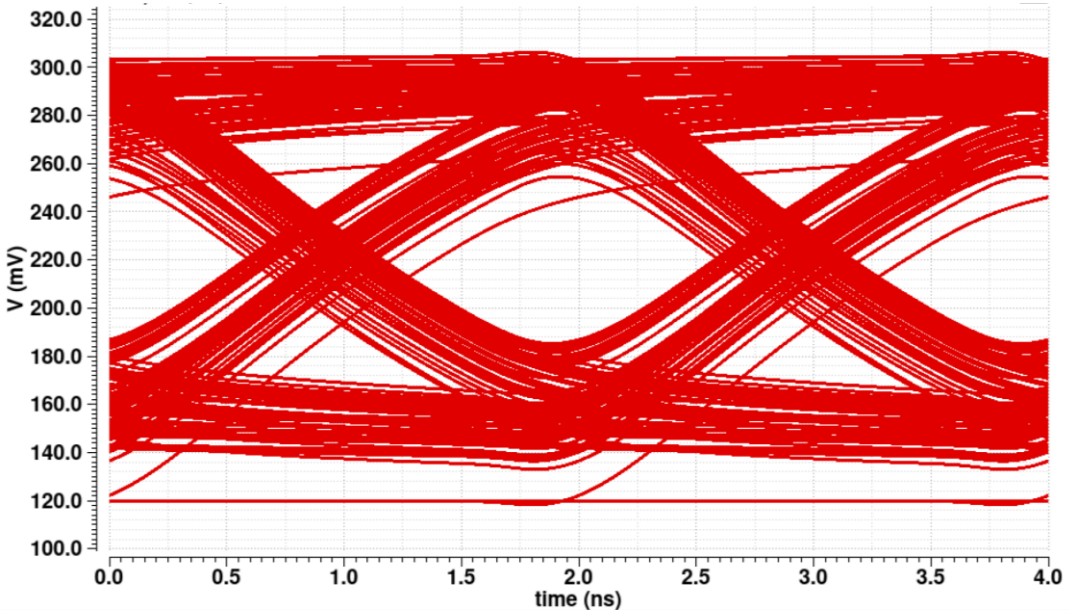
Settings: Pre-Tap Duration: 100% of UI | Post-Tap Duration: 100% of IO



Eye Opening: 37.6mV and 0.879ns

Optimal Line Driver Pre-Emphasis Settings:

Pre-Tap Duration: 10% of UI | Post-Tap Duration: 90% of IO



Eye Opening: 74.4mV and 1.183ns

Input: 7b PRBS signal running at bit period of 2ns (500MHz)

Tap Weights: 600mV each

Cable length: 6m

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