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Fast MAPS for Timing Capabilities at Future Colliders

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Why FAST MAPS?

At future e+e- machines, we will aim to unprecedented precision on Higgs and Standard Model measurements.

- These ambitious physics goals translate into very challenging detector requirements on tracking and calorimetry.
- High precision and low mass trackers, as well as highly granular calorimeters, will be critical
  - O(ns) timing capabilities are key to suppress beam induced backgrounds

Monolithic Active Pixel Sensors (MAPS), which combine the sensing element and readout electronics on the same device offer many advantages to achieve our objective

Our objective:

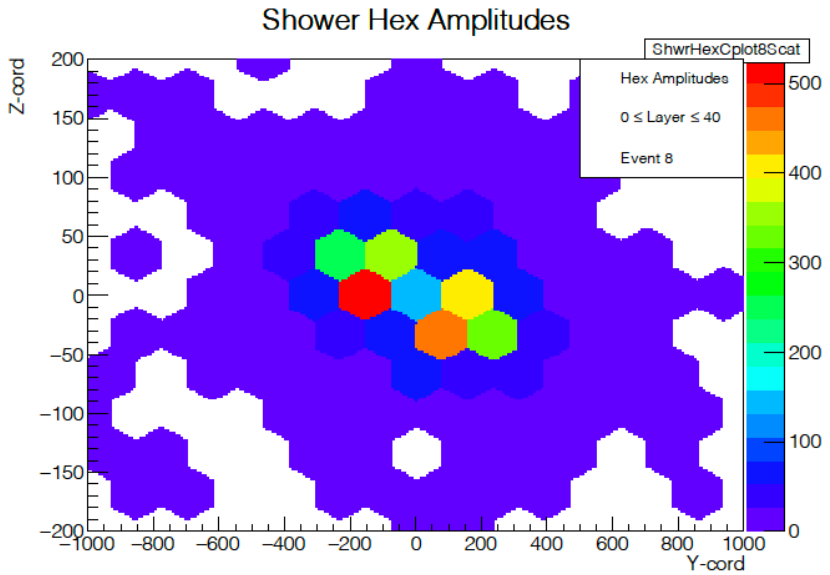
- **improved timing resolution by an order of magnitude beyond the state-of-the art for MAPS**
  - **→ O(ns) timing resolution**
- **low power consumption compatible with large area and low material budget constraints**
  - **→ 100 mW/cm^2 compatible with gas cooling and large area constraints**
  - **Power pulsing can reduce average power consumption for machines with a low duty cycle**

Example of a Possible Application

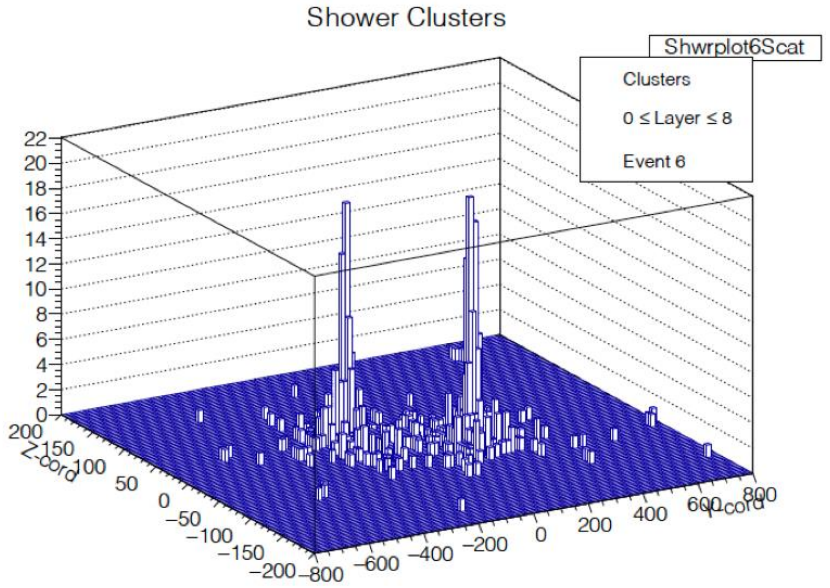
Digital E-Calorimeter for the International Linear Collider (ILC) [1]

Transverse distribution of two 10 GeV showers separated by one cm

Pixel amplitudes (analog) in the ILC 13 mm^2 TDR pixel design



Clusters in the first 5.4 radiation lengths in the new SiD digital MAPS design based on a GEANT4 simulation

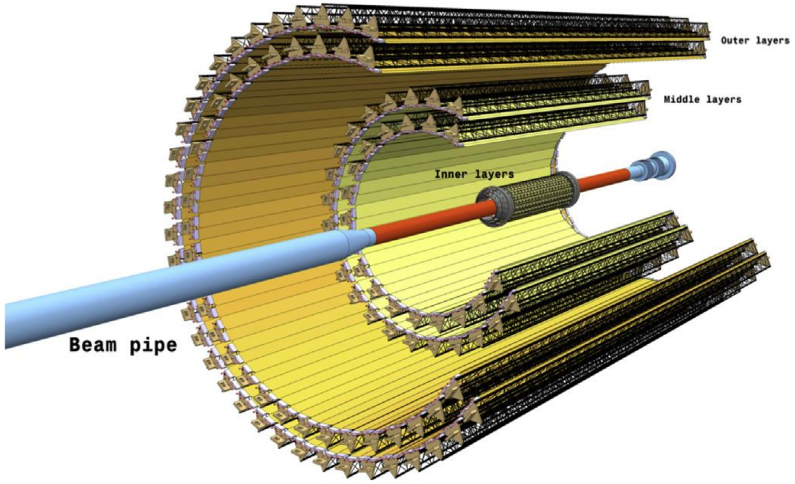


It is shown with simulations that the design of the digital MAPS applied to the ECal exceeds the physics performance required for the linear collider as specified in the ILC TDR

[1] Brau JE, Breidenbach M, Habib A, Rota L, Vernieri C. The SiD Digital ECal Based on Monolithic Active Pixel Sensors. *Instruments*. 2022; 6(4):51. https://doi.org/10.3390/instruments6040051

MAPS advantages

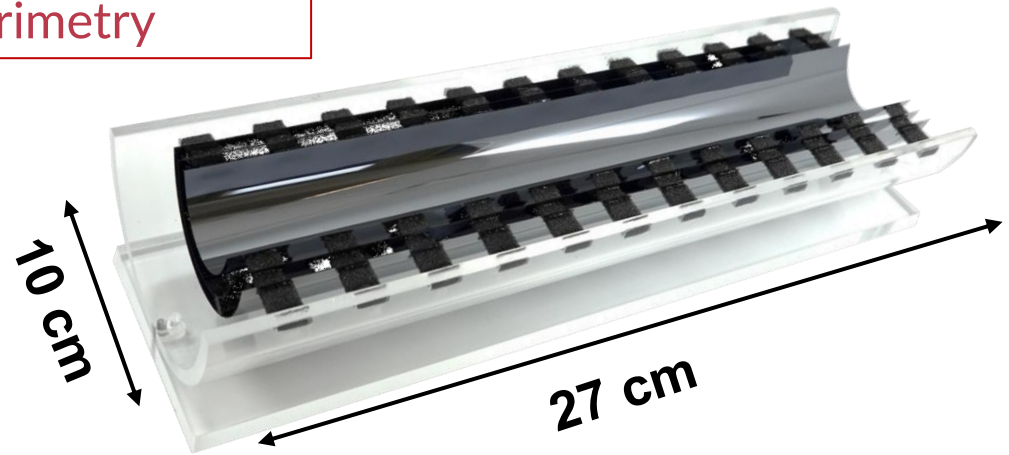
- Monolithic technologies have the potential for providing
  - Small sensor capacitance → High Signal to Noise Ratio with low power consumption
  - Small pixels not limited by bump size → High granularity
  - Thin compact detectors (< 100 µm thickness) → Low material budget
  - Lower costs : implemented in standard commercial CMOS processes
  - The possibility to go to wafer scale detectors with stitching



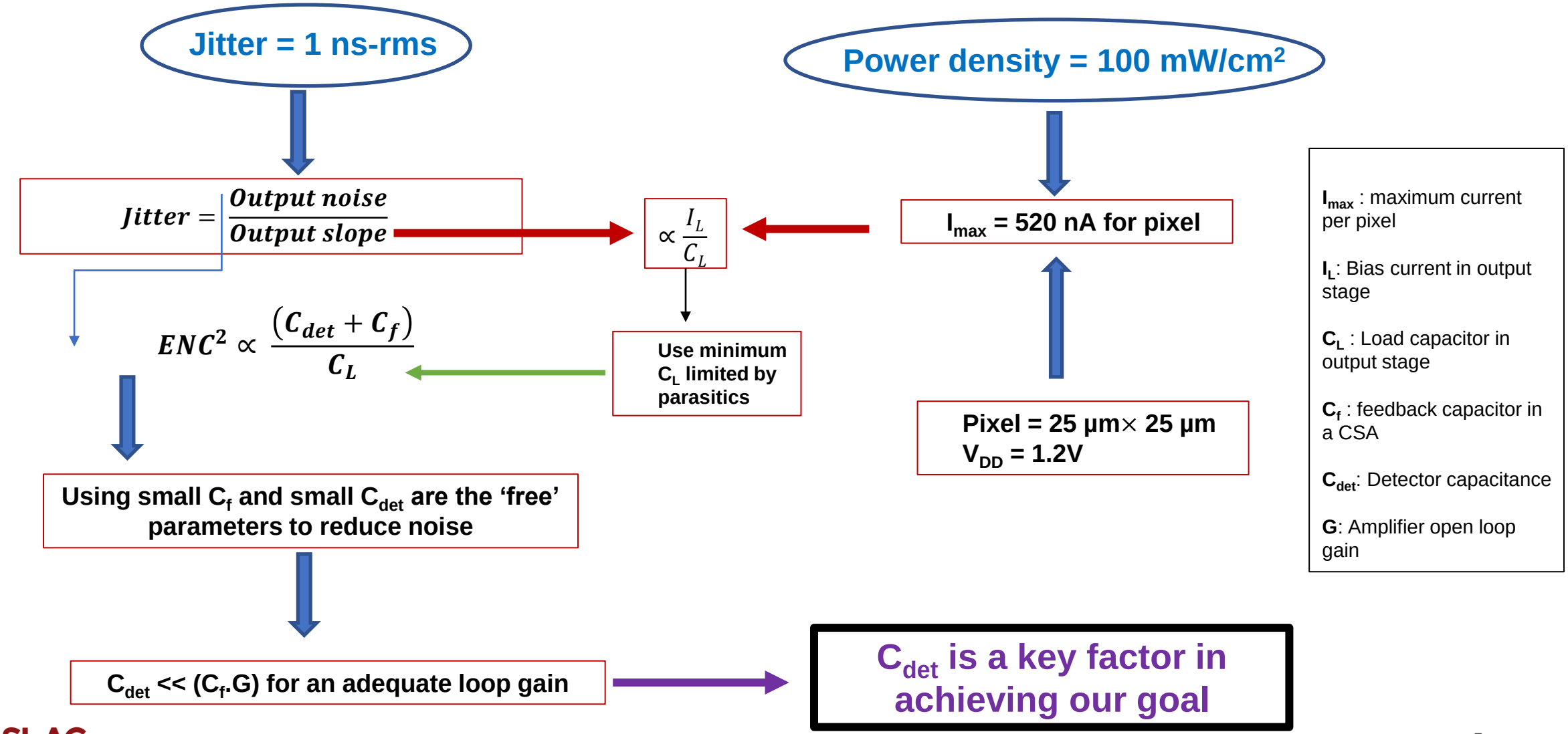
ALICE Inner Tracker System using the ALPIDE Chip
From ALICE Collaboration, Journal of Physics G 41 (2014) 087002

MAPS are very good candidates for high precision tracking and high granularity calorimetry

Ongoing efforts at CERN for achieving a wafer-scale bent MAPS



How can we achieve O(ns) timing resolution with 100 mW/cm^2?



I_{max} : maximum current per pixel

I_L: Bias current in output stage

C_L : Load capacitor in output stage

C_f : feedback capacitor in a CSA

C_{det}: Detector capacitance

G: Amplifier open loop gain

How can we achieve O(ns) timing resolution with 100 mW/cm^2?

C_{det} is a key factor in achieving our goal

A quick simplified hand calculation indicates a C_{det} in the order of a **few fF**

Hybrid Detectors

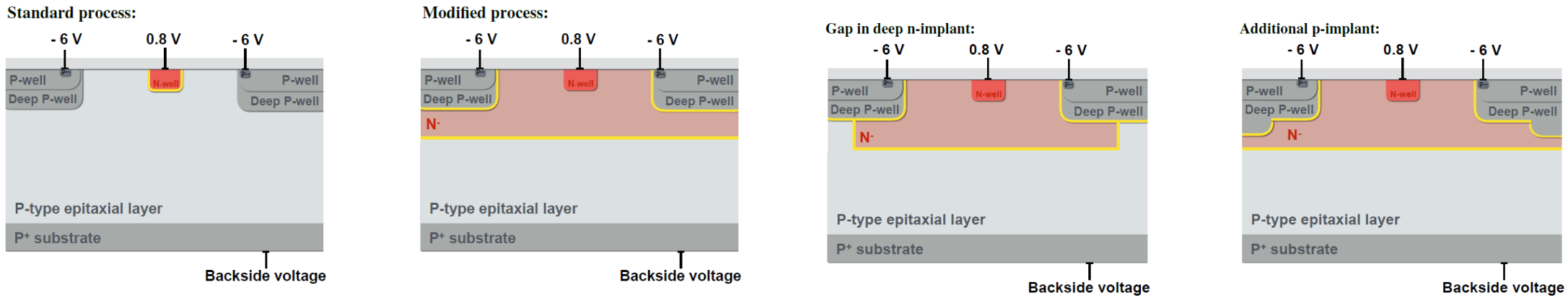
- Minimum C_{det} is limited by bonding parasitics
- Bump bonding limit min pixel size
- Cdet > 100 fF typically

MAPS

- Used historically for visible imaging sensors
- Have been introduced in HEP for about a decade
- It has been demonstrated that we could achieve **Cdet ≈ (1 – 10) fF**

MAPS on TowerSemi 180nm and 65nm

- New technology for MAPS has recently become available through CERN: TowerSemi 65 nm CMOS imaging process with modified implants
  - Deep sub-micron CMOS process: enables new architectures with more functionality and unprecedented performance
  - Sensor optimization in the TowerSemi180 process shows radiation hardness up to 10^{15} n_{eq}/cm^2, time resolution < 2ns with uniform charge collection efficiency across the pixel of size 36.4 µm x 36.4 µm with a small sensor capacitance **(few fF)** [1][2].
  - The know-how developed for the 180nm process is used and adapted to the 65 nm process.
  - Supports stitching: enable wafer-scale MAPS



Sensor optimization in TowerSemi 180 nm process

[1] M. van Rijnbach et al., *Radiation hardness and timing performance in MALTA monolithic pixel sensors in TowerJazz 180 nm*, 2022 *JINST* C04034

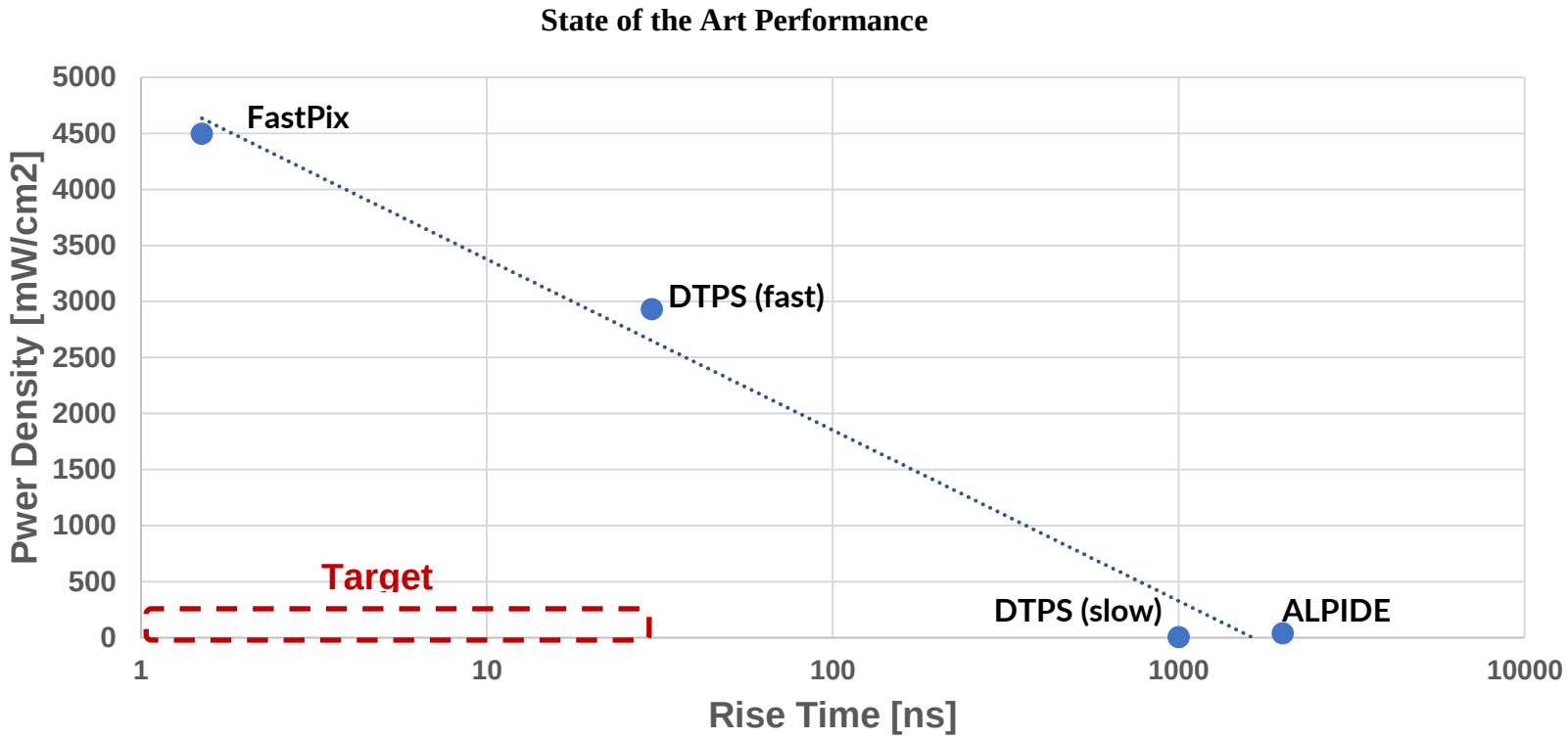
[2] M. Munker et al., *Simulations of CMOS pixel sensors with a small collection electrode, improved for a faster charge collection and increased radiation tolerance,*2019 *JINST* 14C05013

State-of-the-art & our target

Initial specifications for fast MAPS

Parameter	Value
Time resolution	1 ns-rms
Power density	100 mW/cm^2
Minimum Threshold	200 e-
Noise	< 30 e-
Maximum particle rate	100 hits/cm^2
Spatial Resolution	7 µm
Expected charge from a MIP	500 – 800 e/h

*Power density goes down if we use power pulsing in low duty cycle e+e- machines

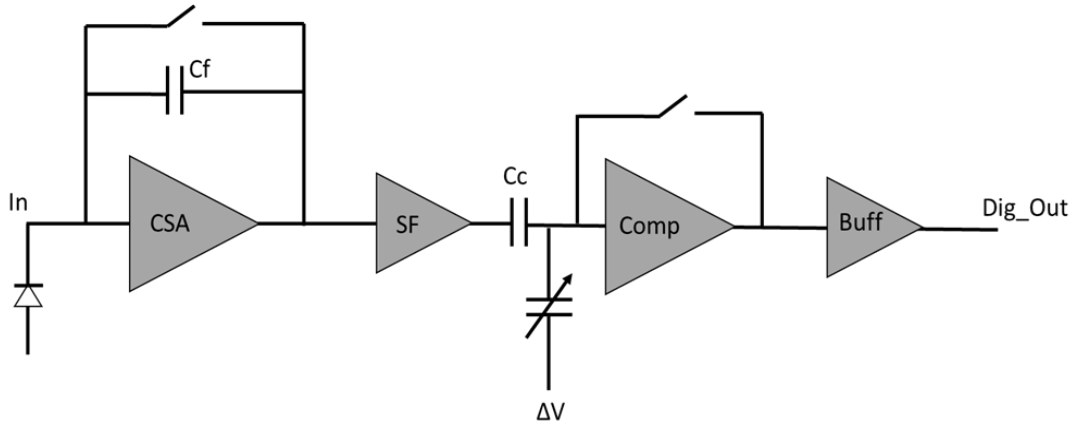


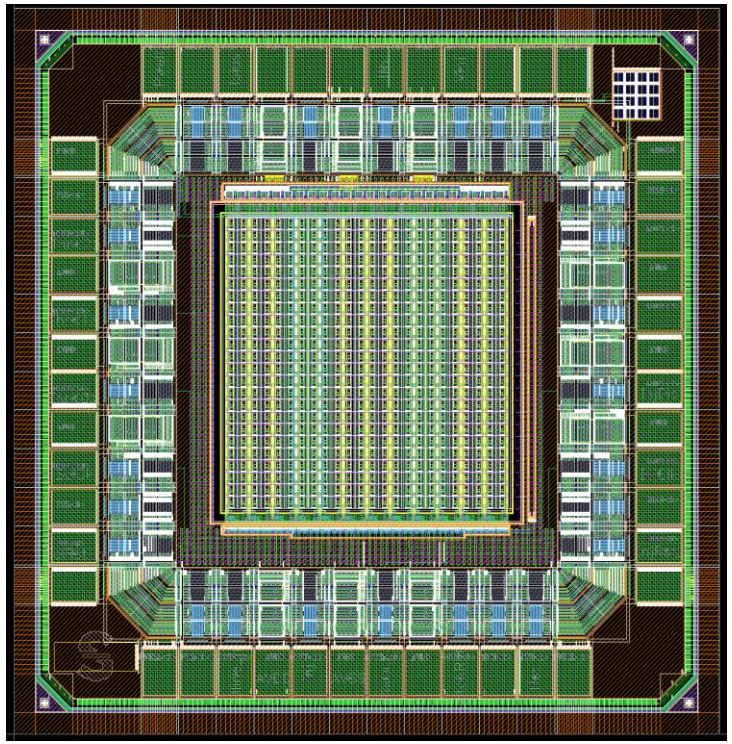
AISC	Technology	Rise time [ns]	Power density [mW/cm2]
FastPix[1]	TJ 180	1.5	4500
DTPS(Fast) [2]	TJ 65	30	2933
DTPS(Slow) [2]	TJ 65	1000	6.4
ALPIDE[3]	TJ 180	2000	40

[1]: T. Kugathsan *et al*. https://doi.org/10.1016/j.nima.2020.164461
[2] : F. Piro *et al.* 'A Compact Front-end Circuit for a monolithic sensor in a 65 nm CMOS Imaging Technology' NSS-MIC 2022
[3] : M. Mager https://doi.org/10.1016/j.nima.2015.09.057

MAPS Prototype Submission

- The CERN WP1.2 has been working and optimizing MAPS TowerSemi technology for many years.
- SLAC is collaborating with CERN WP 1.2 on a shared submission.
- The prototype design submitted with a total area 5 mm x 5 mm and a pixel of 25 µm × 25 µm



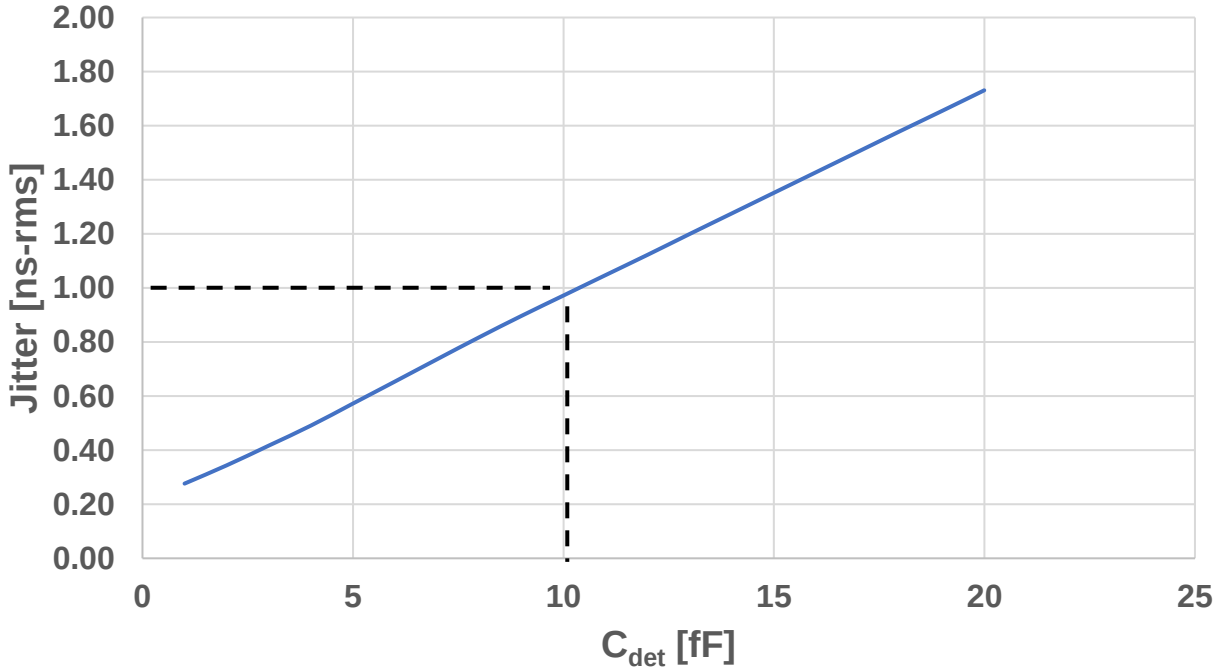


Layout of MAPS SLAC prototype for WP1.2 shared submission

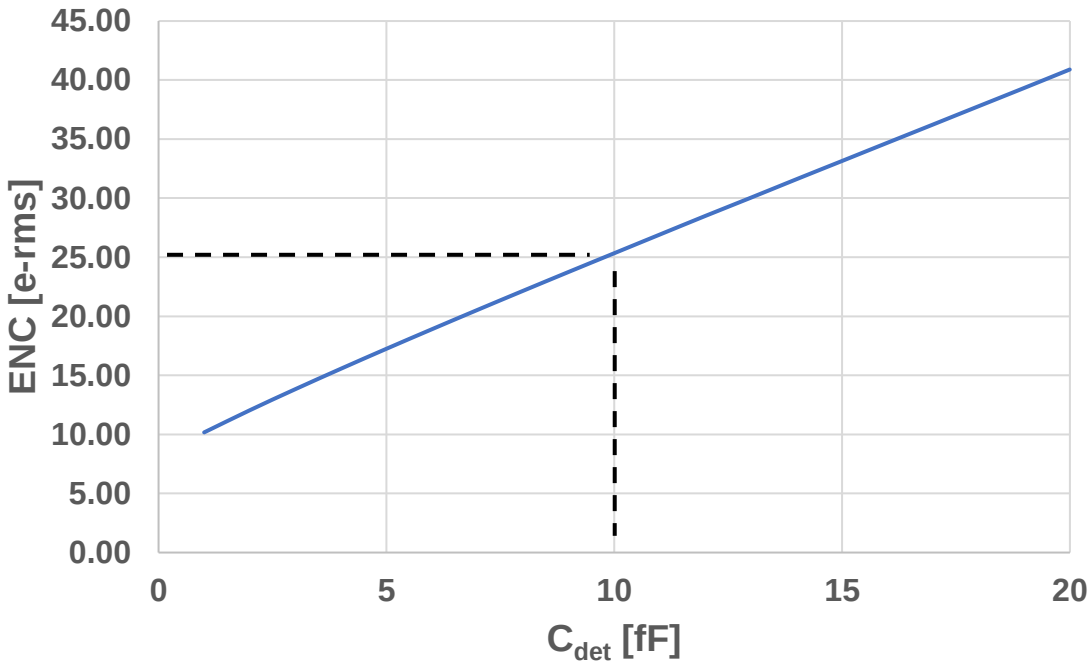
Pixel key elements

- Charge Sensitive Amplifier (CSA) with a synchronous reset, which can be powered down during inactive time
- A comparator with auto-zero technique, removing the need for per-pixel threshold calibration

Simulation of Jitter and ENC as a Function of C_{det}



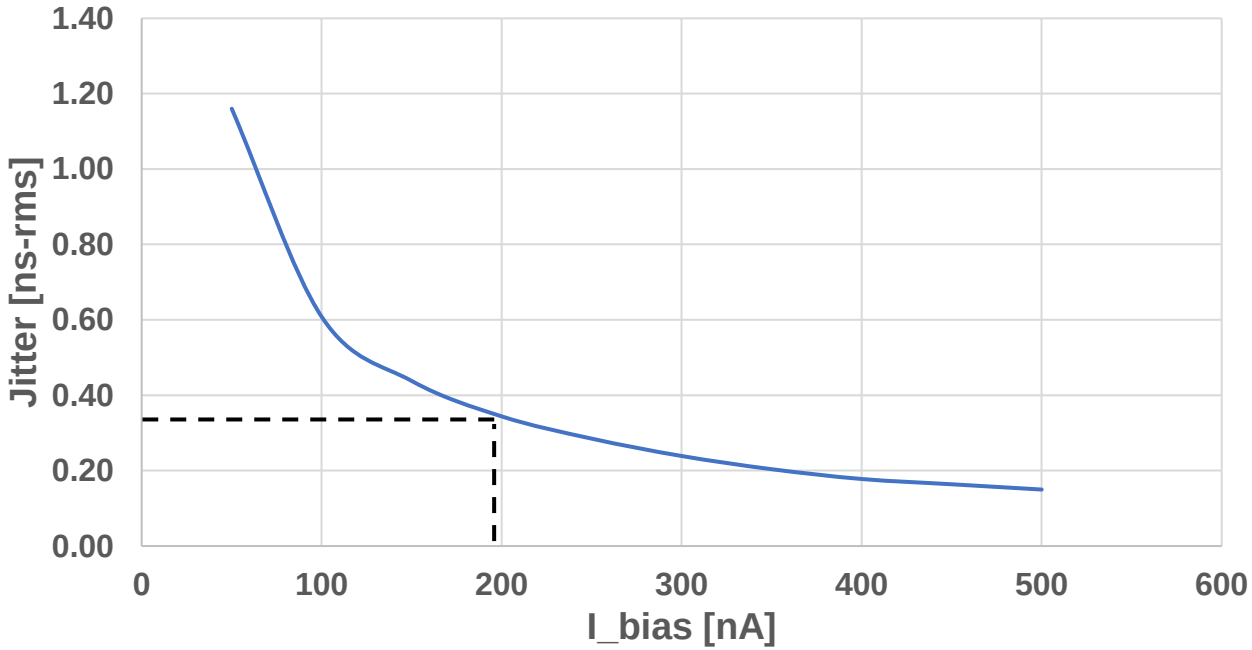
jitter < 1 ns-rms for C_{det} < 10 fF

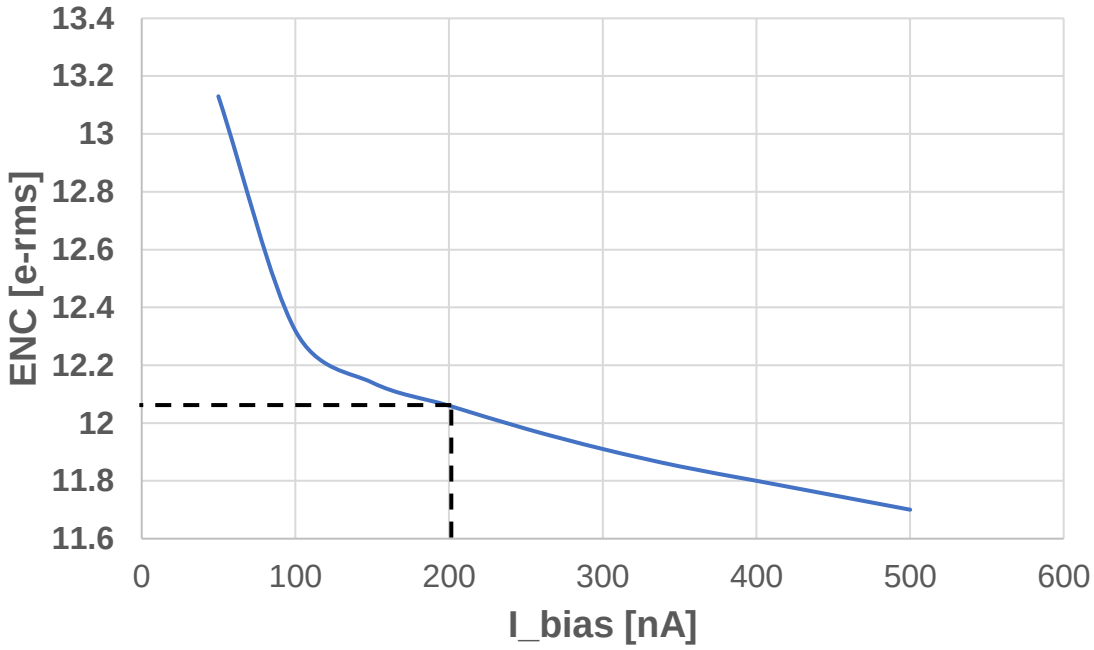


ENC < 25 e-rms

Jitter and ENC as a Function of power

Nomial I_bias = 200 nA
C_{det} = 2 fF in this simulation

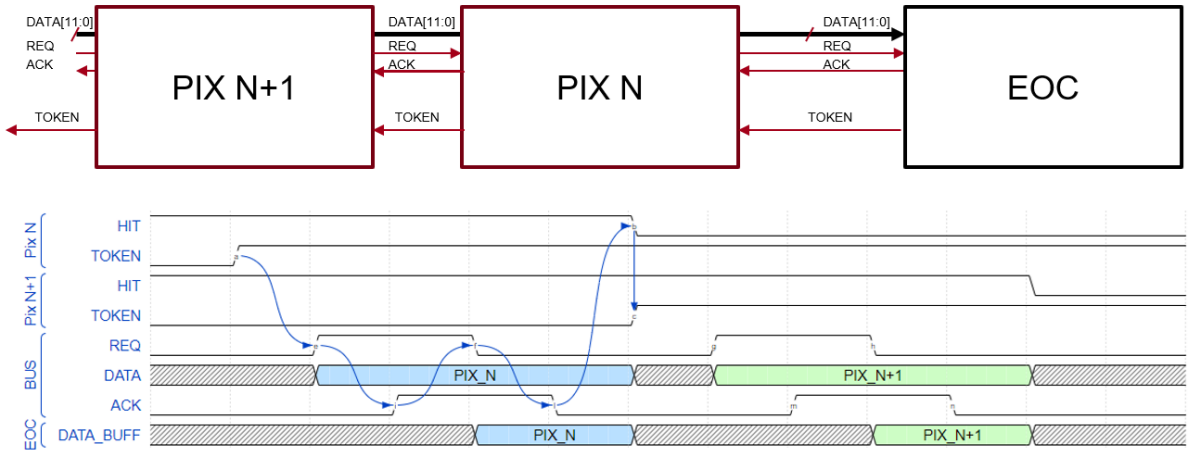




- **ENC does not really depend on power**
- **Jitter gets better with power, due to faster signal slope**
- **Nominal I_bias = 200nA seems a good compromise for ENC, jitter and power density and is compatible with the power budget.**

Next Steps

- Characterization of submitted prototype (in 2023)
- Design of a time encoding block (TDC) while respecting the power constraints
  - No clock distribution across the matrix
- Study/implement a sparse asynchronous readout architecture



A possible readout architecture that has been successfully implemented for the SparkPix-T (Tixel) ASIC developed at SLAC

Conclusion

- With optimized commercial MAPS process, it has been demonstrated the possibility to achieve very low sensing node capacitance (< 10 fF)
- This allows very low noise (< 20 e-rms) and a timing capabilities of O(ns) with a very low power consumption <100 mW/cm^2
- The average power can go lower with power pulsing for applications in e+e- machines having low duty cycles, allowing the implementation of large area detectors with gas cooling
- Simulations proved the concept feasibility, and a prototype chip was design in a shared submission with CERN WP1.2 in TowerSemi 65 nm technology
- Considering the technical advantages, in addition to the low material budget, and the relatively low cost, Fast MAPS are excellent candidates for high precision tracking and high granularity calorimetry for future e+e- colliders

Thank you for your attention!