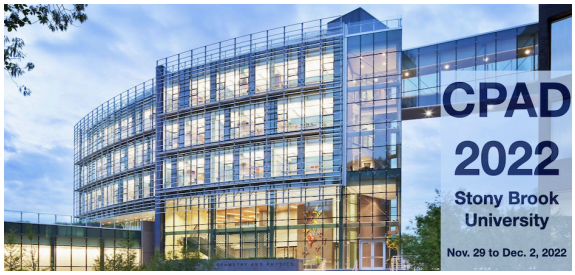

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Fast MAPS for Timing Capabilities at Future Colliders

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The detectors at future e+e- linear colliders will need unprecedented precision on Higgs physics measurements. These ambitious physics goals translate into very challenging detector requirements on tracking and calorimetry. High precision and low mass trackers, as well as highly granular calorimeters, will be critical for the success of the physics program. To develop the next generation of ultralight trackers, a further reduction of dead material can be obtained by employing Monolithic Active Pixel Sensor (MAPS) technology. In MAPS, Si diode charged particle sensors and readout circuitry are combined in the same pixels, and can be fabricated with commercial CMOS processes. Currently MAPS are widely used in different applications in High Energy Physics (HEP), and also in astronomy and X-ray imaging.

Recently, CERN has developed a process modification for the TowerSemi 180 nm CMOS imaging sensor process with extremely low capacitance (in the order of a few fF). This results in a reduced readout noise and power consumption of the front-end electronics, resulting in a reduced need for cooling and enabling light interconnection circuits and mechanical support structures. This technology has been utilized for the Inner Tracking System Upgrade (ITS2) of the ALICE experiment at the LHC.

The CERN WP1.2 collaboration is investigating the possibility of realizing wafer-scale MAPS devices on the novel TowerSemi 65 nm CMOS imaging process. This novel technology offers four-times higher density for circuits, higher spatial resolution, better timing performance and lower power consumption. All these features make the TowerSemi 65 nm process the current state-of-the-art technology for the development of new generation MAPS.

The present work focuses on the development of fast MAPS with improved timing resolution, from the current ~1μs state of the art to ~1 ns, leveraging the collaboration with the CERN's WP1.2. The improved timing resolution must be achieved with a low power consumption to allow for gas cooling, and to offer the possibility of realizing wafer-scale sensors. Therefore, the pixel design will rely on an efficient power-pulsing technique where the sensor's electronics are turned on only during a small window of time, taking advantage of the low duty cycle of e+e- linear colliders. Moreover, the pixel's sampling and noise cancelation techniques will be synchronized with the bunch crossing, to achieve a high signal to noise ratio while maintaining a low power consumption.

A first MAPS prototype was submitted this year in TowerSemi 65 nm technology. The prototype has a dimension of 1.5 ⊠ × 1.5 ⊠ with a pixel pitch of 25 ⊠ ×100 ⊠. This prototype serves to set the baseline for the sensor and the electronics performance. Following the characterization of this prototype, a second prototype will be designed with more emphasis towards meeting the required specifications.

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