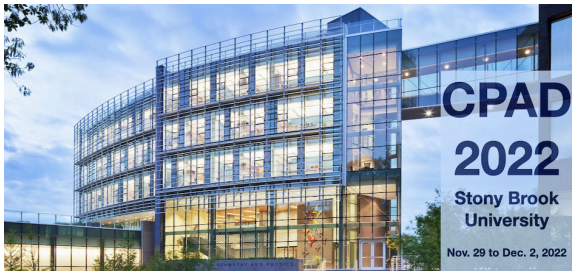

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Proposal to Develop an Economical Low-Power Sub-psec Resolution ASIC

Thursday, 1 December 2022 11:55 (20 minutes)

We propose to develop a pathfinder multichannel chip using a modern CMOS process to demonstrate large channel count and scalable multi-buffered readout with sub-psec timing resolution. The development will address the important challenges of calibration, stability and power density that will need to be overcome to create a robust detector system for particle physics experiments in HEP and NP using precise timing for identification of particle flavor and family.

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