MIDNA: Sub-electron skipper-CCD readout with multi-channel cryogenic low-noise readout ASICs

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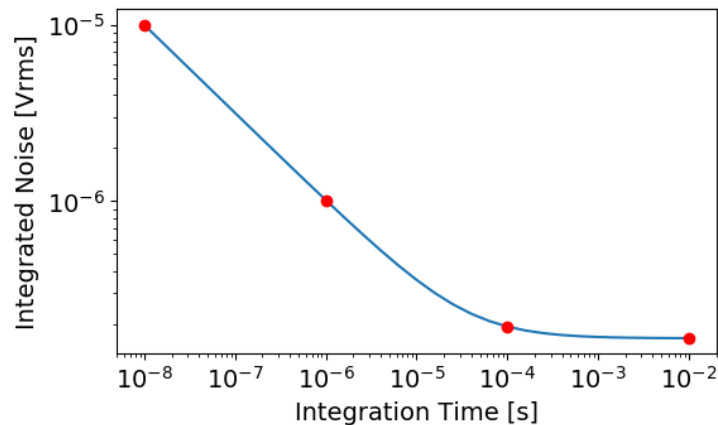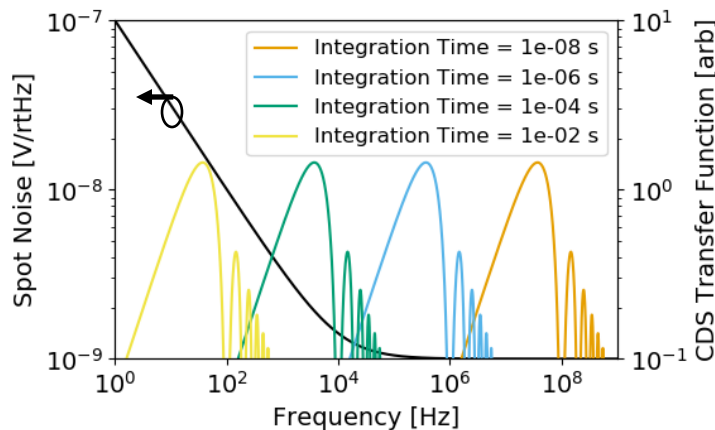[1]Fermi National Accelerator Laboratory

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Outline

- Skipper CCDs used for Dark Matter

- Midna ASIC for Skipper CCD Readout

- Midna 2 Architecture and Results

- Conclusions and Future Development

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CCDs for Low Noise Imaging

- CCDs have long been the main choice for low noise scientific imaging
- The low noise has been enabled by a combination of integrating the readout for long periods and using correlated double sampling (CDS) [1]
  - Unfortunately, 1/f noise means that there was a limit to the effectiveness of this approach
  - Long integration moved the content of interest to lower and lower frequencies
  - The spreading out of the CDS sampling points reduced the filtering of flicker noise

[1] White et al., "Characterization of Surface Channel CCD Image Arrays at Low Light Levels."

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Skipper CCDs for Exceptional Low Noise for Dark Matter Search

- Skipper CCDs and similar technologies enabled the non-destructive readout of the same pixel many times [2]
  - The noise can be lowered by averaging many shorter reads rather than one long read
  - It continues the decreasing noise trend with longer measurement times
- There are still limits to this approach
  - Leakage in the charge transport in the CCD (low)
  - Speed of the various readout stages and clocking
- A skipper CCD has demonstrated the lowest ever, 0.068 e$^-_{rms}$, noise floor in CCDs [3]
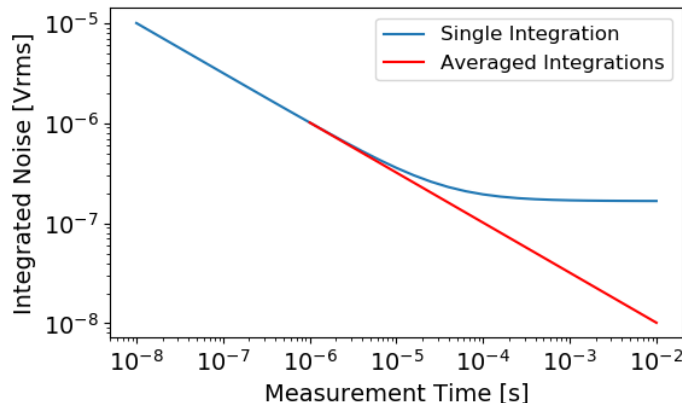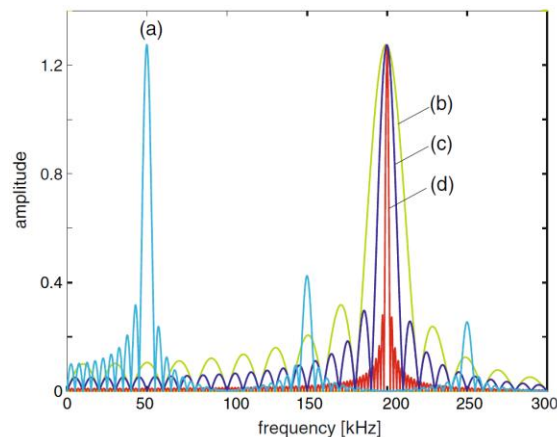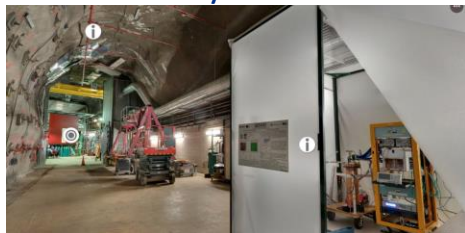 - Required 4000 read averages at 10 µs/read

Fig. 8 Frequency response of the Skipper readout system for $T_S = 10\ \mu s$ and $N = 10$ (**a**) and for $T_S = 2.5\ \mu s$ and $N = 10$ (**b**), $N = 20$ (**c**) and $N = 100$ (**d**)

From [3]

[2] Janesick, J.R., et al. "New advancements in charge-coupled device technology: sub-electron noise and 4096×4096 pixel CCDs."
[3] Fernández Moroni et al., "Sub-Electron Readout Noise in a Skipper CCD Fabricated on High Resistivity Silicon."

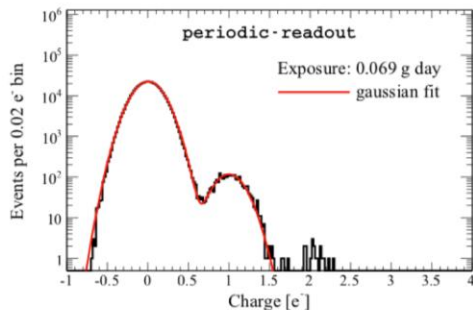🎇 Fermilab

Skipper-CCD for Dark Matter Search

FNAL / MINOS

Phys. Rev. Lett. 122, 161801 (2019)

SNOLAB

During December 2019 we installed the first skipper-CCD at SNOLAB. (2.5 g active mass)

SENSEI 100

Design for the 100g experiment is done, and orders for parts have been placed.

Multi skipper-CCD modules for SENSEI-100 currently being tested with great success.

Next: 28 Gigapixel digital camera for dark matter!
Cooling, readout, packaging and testing of the required **24000 skipper-CCD sensors require engineering solutions that are not available yet for scientific CCDs.**

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OSCURA: 4 year Research and Development Effort

"DOE Dark matter New Initiatives" FNAL, LBNL, PNNL, U. Chicago, U. Washington, Stony Brook University.

Fermilab is leading the effort to develop the a skipper-CCD dark matter detector with active mass of 10 kg of Silicon.


28 Gigapixel digital camera for dark matter!

Cooling, readout, packaging and testing of the required **24000 skipper-CCD sensors require engineering solutions that are not available yet for scientific CCDs.**

Radiation background required is ~10 lower than state of the art experiments.
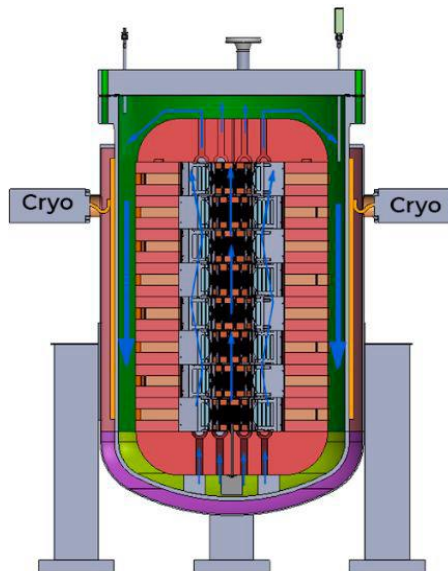
Fabrication of **skipper-CCDs needs to be adapted to the changes in the semiconductor industry. We have identified new industrial** partners for this, and will be testing them over the next year.
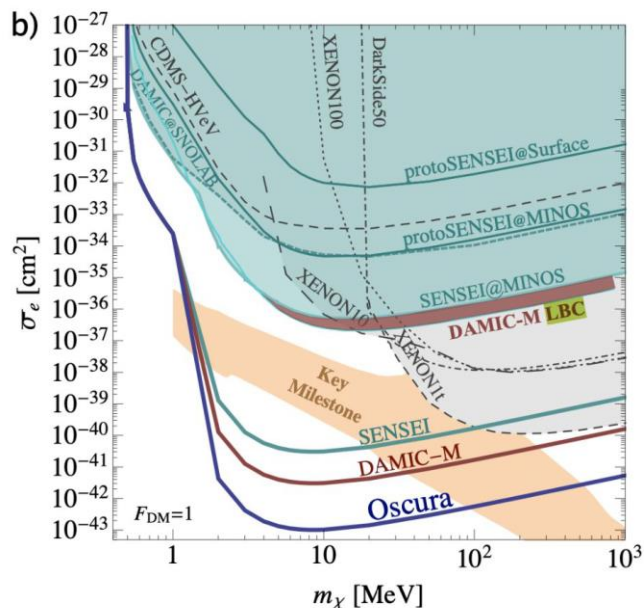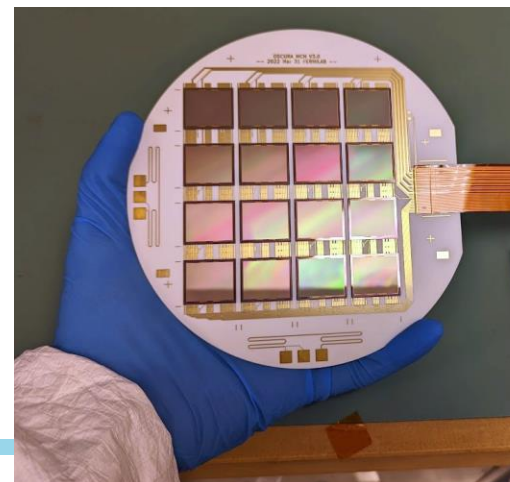
Taking the skipper-CCDs to their full potential as dark matter detectors.

An ASIC to Support Scaling to 28 Gigapixels, MIDNA

- MIDNA is a prototype cryogenic low-noise skipper-CCD readout ASIC

- It is an enabling technology for the OSCURA dark matter detection project

- Integrates multiple readout channels onto a single chip, replacing numerous costly PCB components and saving valuable physical space

- Operates at 120 Kelvin where COTS devices are not guaranteed to specification

4 channels discrete electronics
(C. Chavez, Fermilab)

4 channels
MIDNA

21mm

45 mm

2 mm

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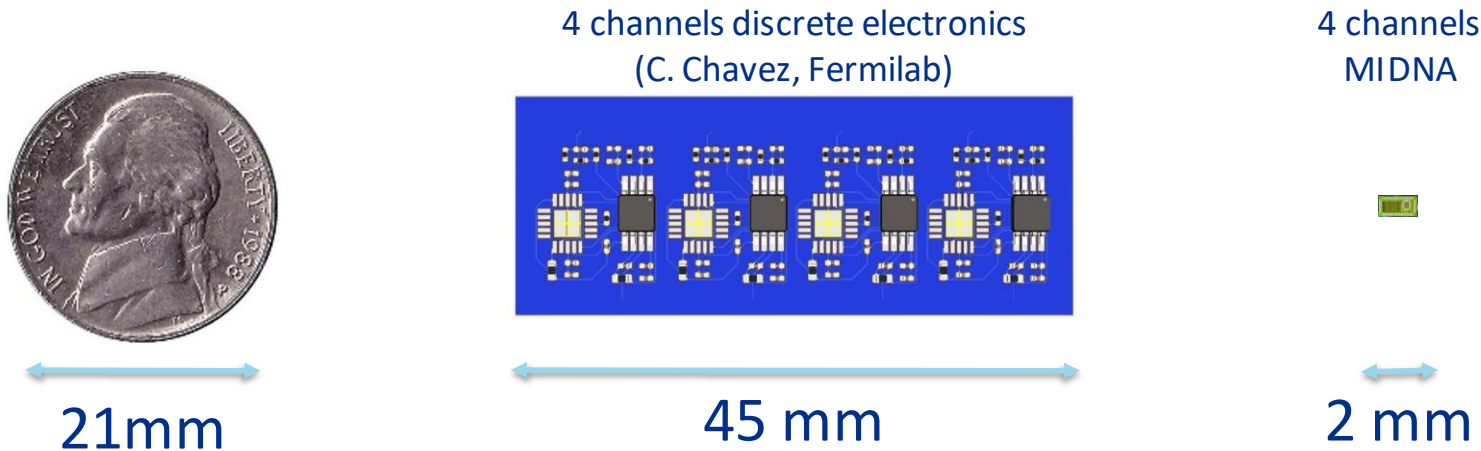
MIDNA Specifications and Roadmap of the Chips

- Less than one third of typical CCD readout noise
- 3000 electron maximum input
- Pile up to achieve sub-electron readout noise with CCD (for signals up to 5e$^-$)
- Capable of cryogenic operation between 100 and 130 Kelvin

MIDNA v1

- Prototype proof of concept
- Noise is top priority
- Little priority on integration
- Auxiliary test structures

MIDNA v2

- Refined performance
- Support circuitry integration
- Keep minor scaling

MIDNA Future

- Scale to need, 100s channels practical
- On chip digitization

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MIDNA Channel

- The foundation of the MIDNA channel is a dual-slope integrator
- The integrator is used to implement CDS and filtering
- Chopping included in the integrator is key to sub-electron performance
- See T.England's CPAD 2021 presentation
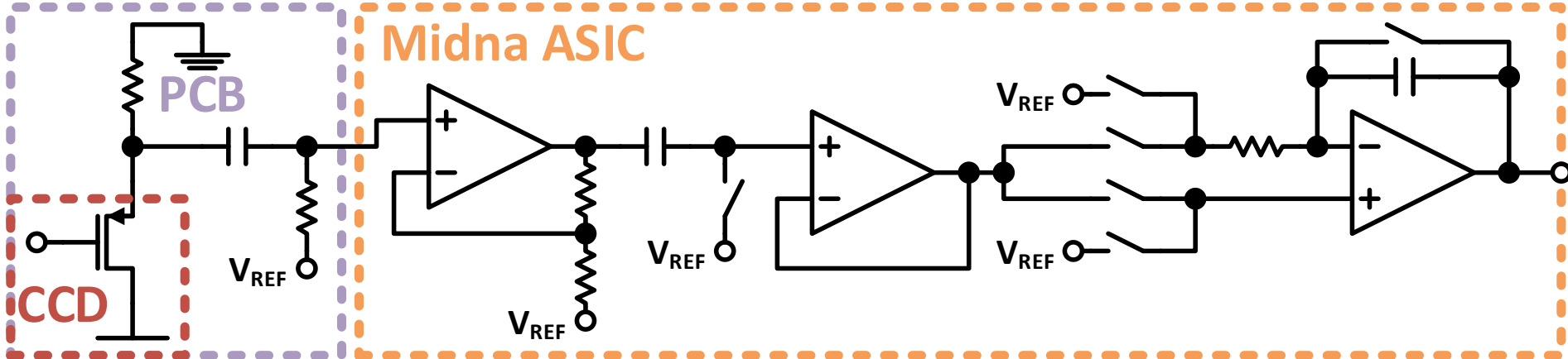
MIDNA 2 incremental improvements

- Internal BGR reference and independent voltage buffering
- Reduced integrator offset for improved analog pile-up
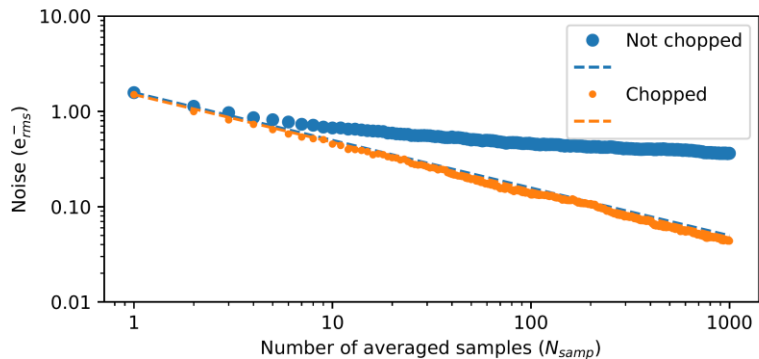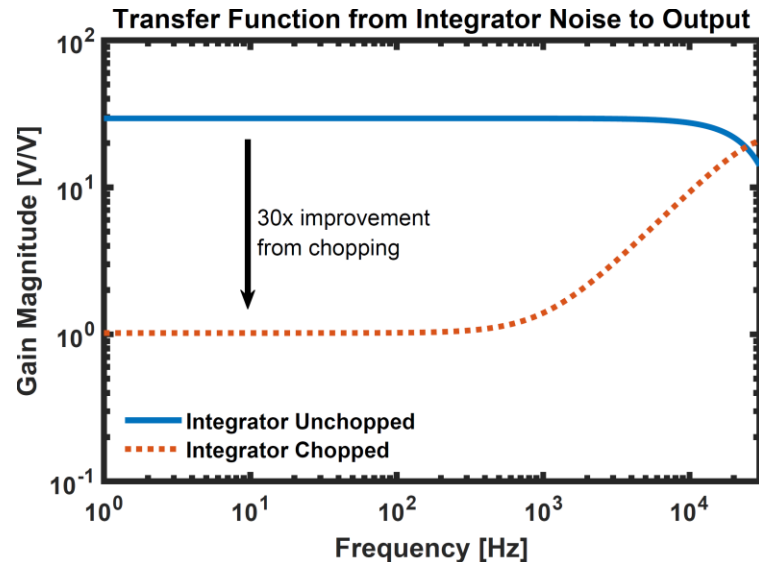- Chopping now default
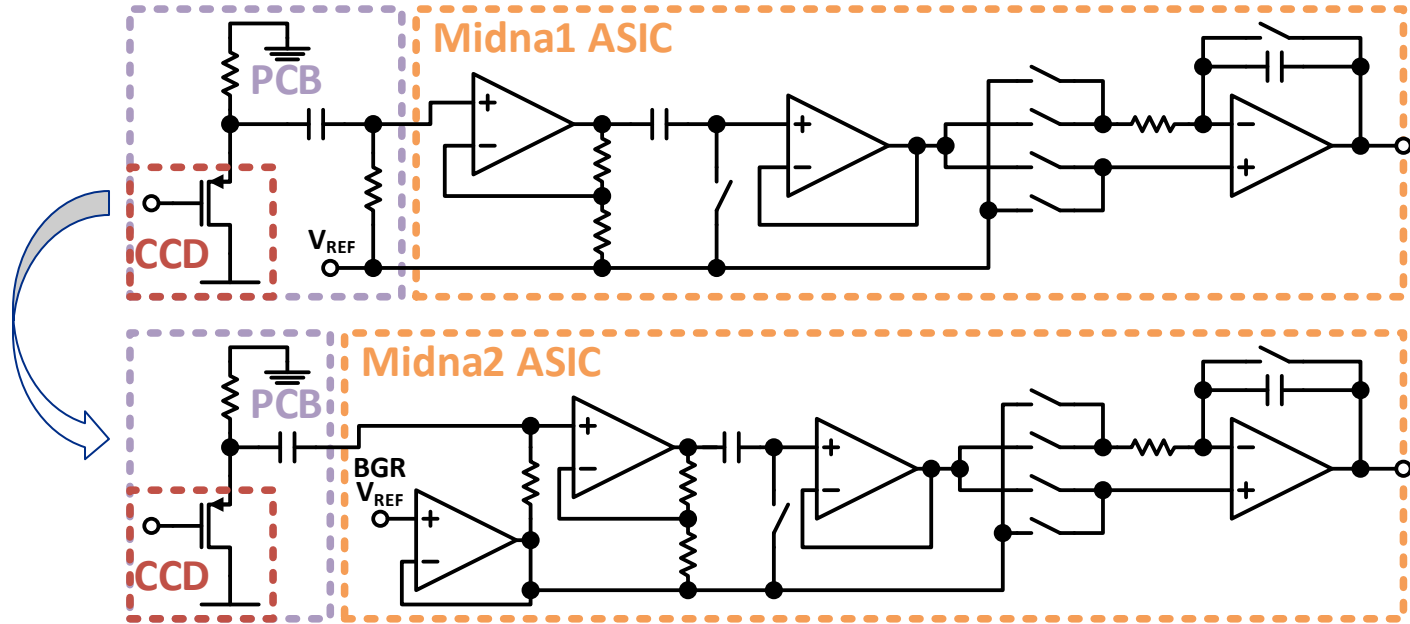
Integrator Chopping

Chopping allows the integration of the feedback amplifier's internal offset and low frequency noise in opposing directions during readout, greatly lowering the magnitude of the transfer function from the effective noise source to the output of the channel

Test results for a standard-sequence measurement of an AC-grounded channel with and without chopping of the integrator.
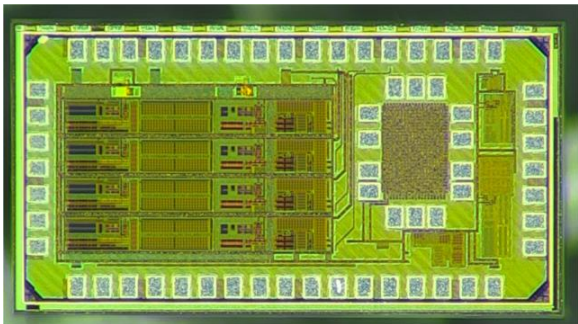
- Without mitigation of the 1/f noise contributed by the integrator feedback amplifier, the noise magnitude saturates
- With chopping, noise reduction continues as $N^{-1/2}$, indicative of white noise
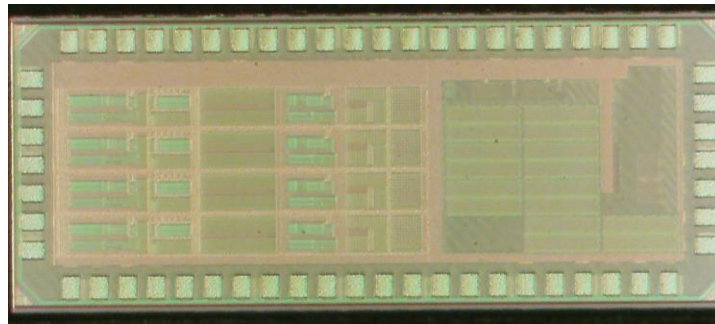- → Chopping critical for low noise results

Transfer Function from Integrator Noise to Output

30x improvement from chopping

Integrator Unchopped
Integrator Chopped

Frequency [Hz]
Gain Magnitude [V/V]

Not chopped
Chopped

Noise (e_{rms}^-)
Number of averaged samples (N_{samp})

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MIDNA 2 adds Support Circuitry on chip for OSCURA Scaling

MIDNA v1

MIDNA v2

- Size: 2mm x 1mm
- Four parallel readout channels
- Digital controller
- External biasing
- Test structures

- Size: 2.5mm x 1mm
- Four parallel readout channels
- On-chip voltage bandgap reference and biasing
- Reduced Integrator offset and chopping by default.
- Reference voltage buffered on each channel.

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Block Diagram

- Each channel is about 150 μm x 1.3 mm
- Chip is 2.5 mm x 1 mm
- Taped out in March 2022
- Four analog channels
- 4.5mW/channel
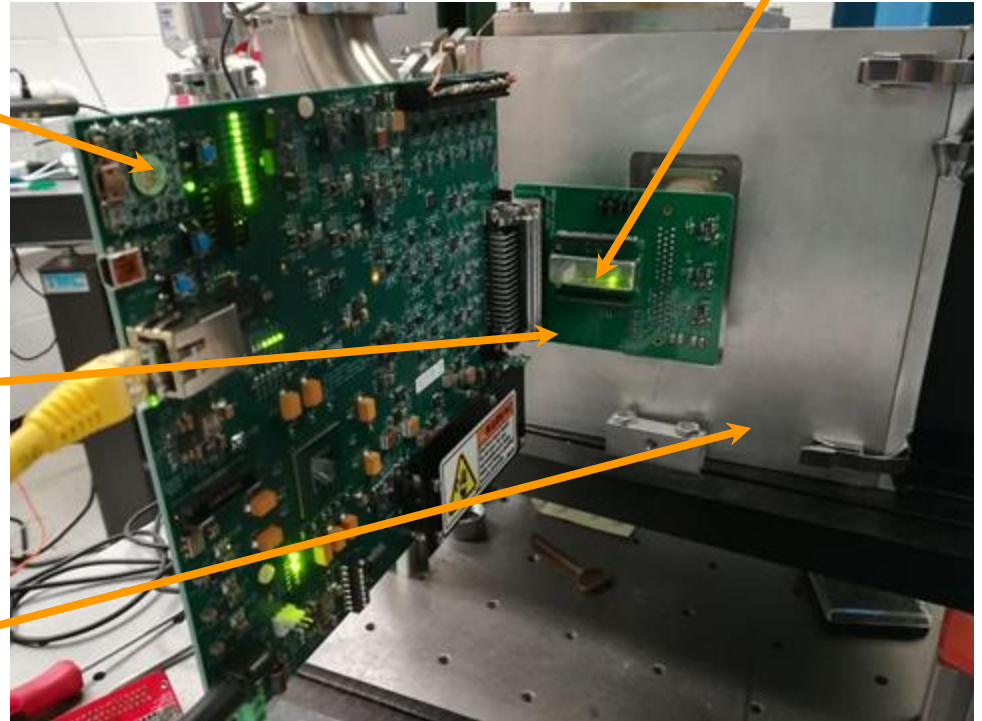- On chip low-noise bandgap reference
- On chip biasing

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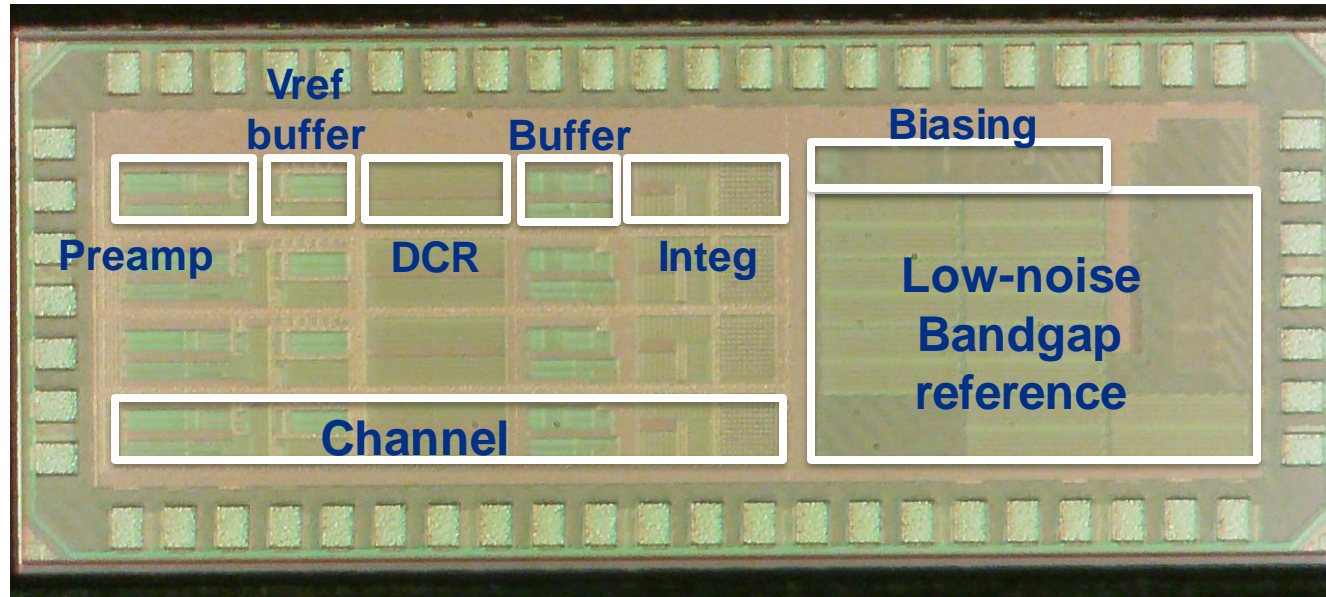
MIDNA 1 Measurement Setup

PC

FPGA

DACs, Clks | ADCs | Power supply

Vreg

CCD
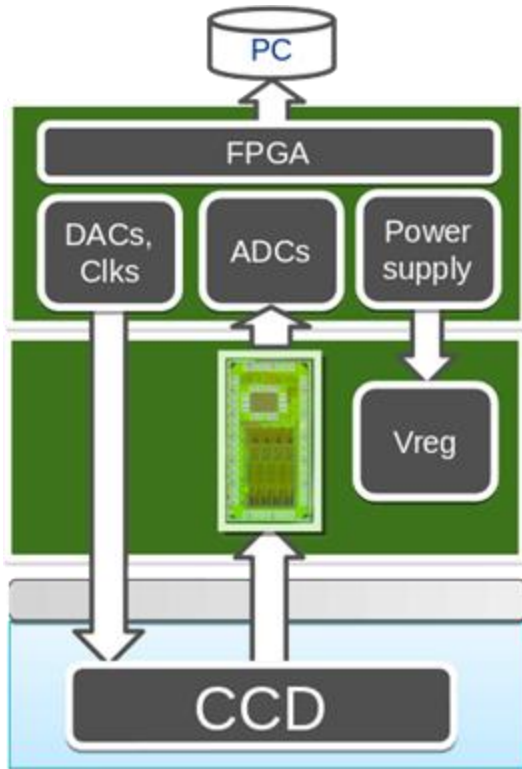
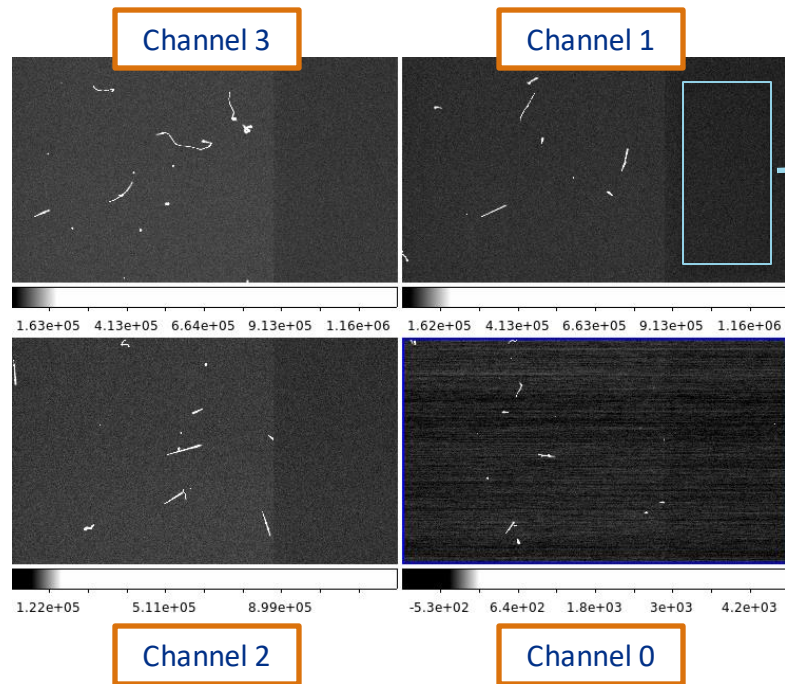Low-Threshold Acquisition (LTA) board
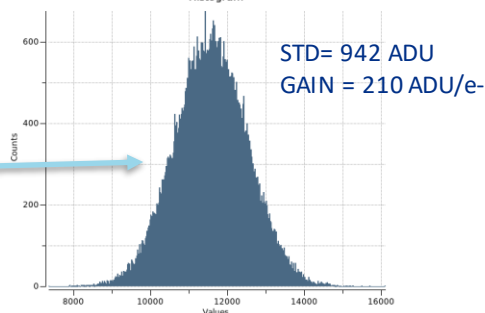
Outside Dewar board

Cooled down CCD

MIDNA (shielded)

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MIDNA 1 CCD Image Readout

- Channel working. We see particle interactions.
- Single sample acquisition.

Pixel histogram
(overscan region)

Channel 3

Channel 1

STD= 942 ADU
GAIN = 210 ADU/e-

1.63e+05   4.13e+05   6.64e+05   9.13e+05   1.16e+06

1.62e+05   4.13e+05   6.63e+05   9.13e+05   1.16e+06

1.22e+05   5.11e+05   8.99e+05

-5.3e+02   6.4e+02   1.8e+03   3e+03   4.2e+03

Channel 2

Channel 0

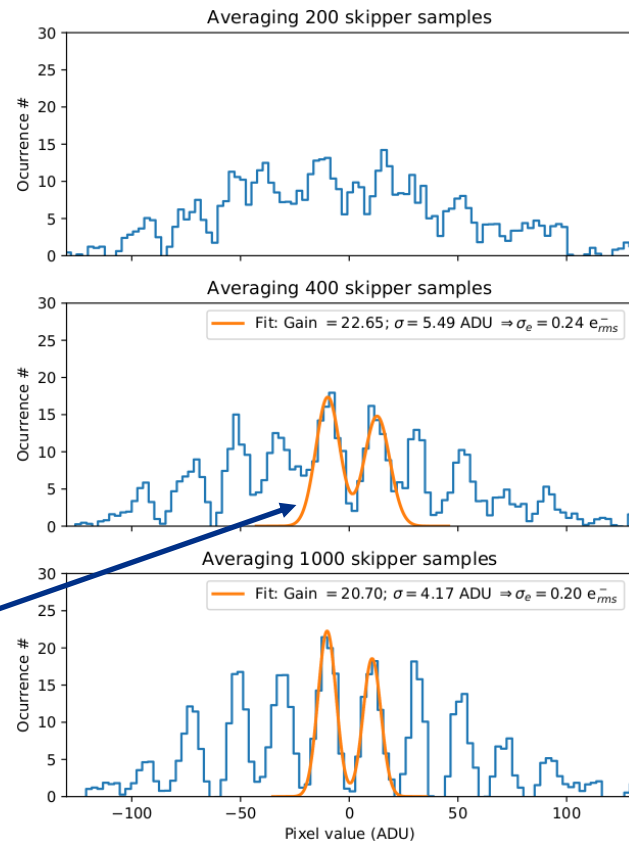Single sample
readout noise: 4.5 e⁻$_{rms}$

Microchip CCD @ 140K
Integration time: 13μs

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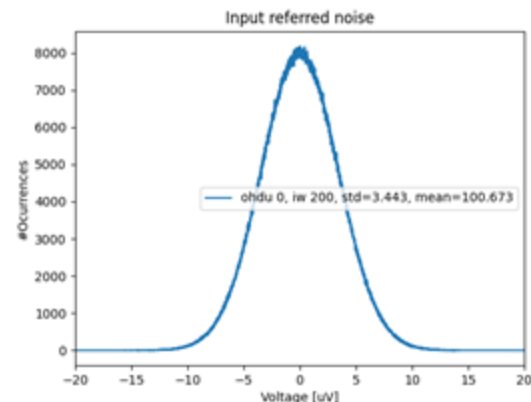
MIDNA 1 Achieves Sub-electron CCD Readout Noise

- Even with MIDNA at room temperature, sub-electron readout noise was achieved
- Noise is dominated by the CCD
- 0.2 e-rms achieved with 1000 piled up reads
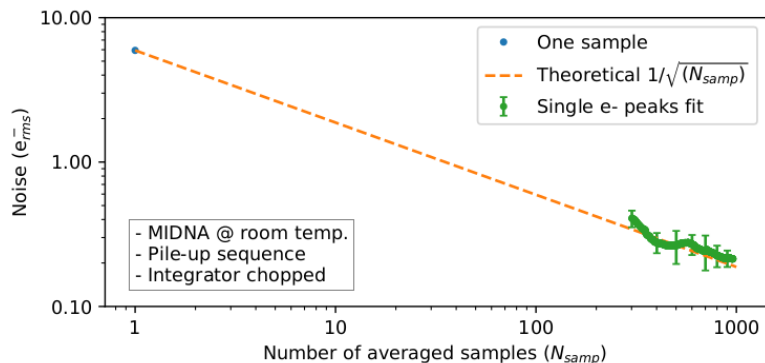
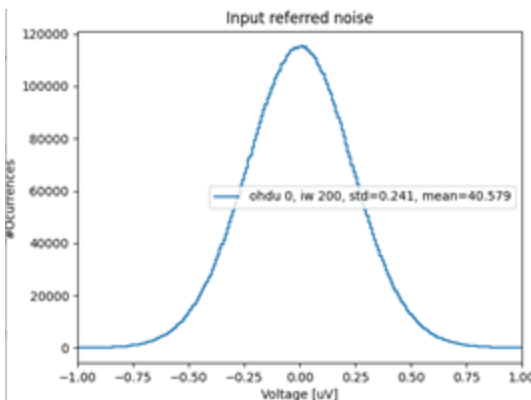Separation of single electron peaks visible even at 400 reads

MIDNA2 Results: Input Referred Noise

ASIC readout noise (no CCD)

- Inputs AC grounded
- Standard sequence. No polarity. IW=13.3µs. SamplePeriod=826µs.
- On average, **3.5 µV$_{RMS}$** input referred noise.
- Equivalent to **2 e$^-_{RMS}$** (CCD gain of 1.8µV/e-)

Reference voltage noise

- Inputs AC grounded - Always RESET
- Standard sequence. Polarity neg/pos. IW=13.3µs. SamplePeriod=826µs.
- Less than **0.3 µV$_{RMS}$** input referred noise
- Equivalent to **0.166 e$^-_{RMS}$** (CCD gain of 1.8µV/e-)
- → Negligible contribution from additional circuitry

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Analog Pile-Up Feature

https://arxiv.org/abs/2108.09389

**Standard sequence** for reading out one sample:

- one negative integration phase
- one positive integration phase
- one sampling phase (black dots).
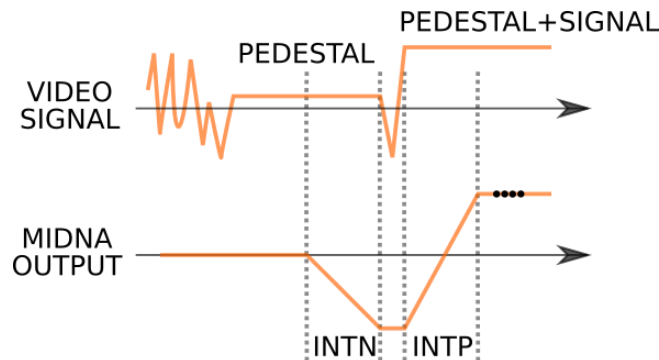
Analog pile-up sequence (e.g. for 3 skipper samples):

- many pairs of integration phases
- only one final sampling phase.
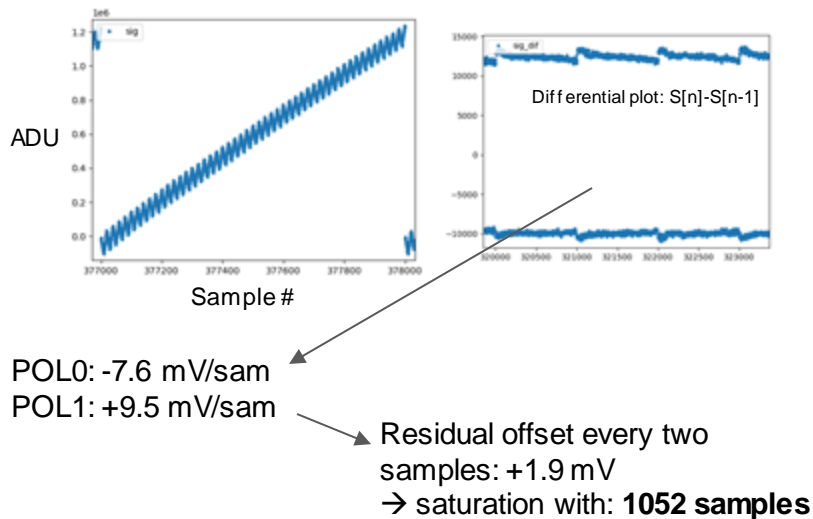- No reset between skipper samples

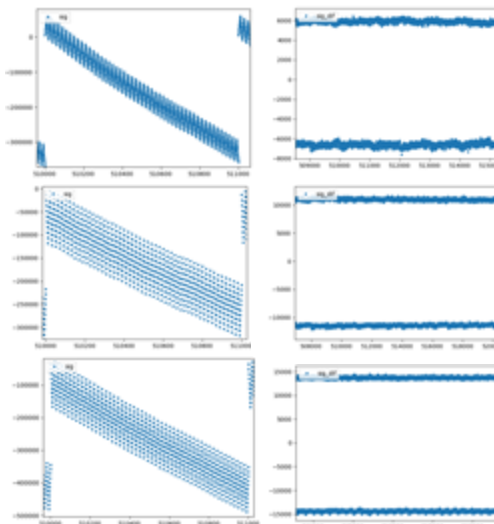→ Analog averaging reduces the number of ADC conversion and data transfer, at the cost of DR

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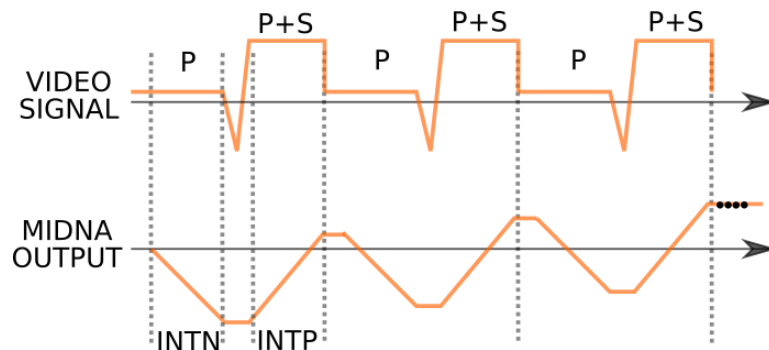
Offset with polarity switching: MIDNA 1 vs. MIDNA 2

DCR always ON. Polarity switch every 10 CDS. IW=13.3µs. Pile-up N=1000.

MIDNA 1

ADU

Sample #

POL0: -7.6 mV/sam
POL1: +9.5 mV/sam

Differential plot: S[n]-S[n-1]

Residual offset every two samples: +1.9 mV
→ saturation with: **1052 samples**

MIDNA 2

Residual offset every two samples:

Channel	Res offset [mV]	# samples for satur.
3	-0.4	**5000**
1	-0.23	**8695**
2	-0.28	**7288**

- Improved in offset symmetry
- Less residual offset
- More room for signal pile-up

5-10x improvement in the residual offset from the integrator with chopping, and this improvement comes from a better symmetry in pos and neg polarities.

Conclusions and Future Work

- MIDNA 1 successfully demonstrated CCD readout with sub-electron noise
  - At a variety of temperatures: room temperature down to ~100K
  - With multiple pile up techniques: cancelation sequence, on chip pile up & off chip pile up

- MIDNA 2 brings more support circuitry on chip to scale OSCURA
  - Lowers complexity of OSCURA, with fewer external components and connections to room temperature
  - Eliminates sources of external interference
  - Testing ongoing, positive results so far
  - Upgrade CCD for lower system noise

- The future of MIDNA is multi-faceted, beyond OSCURA
  - MIDNA itself can be scaled practically to 100s of channels
  - Integrate on-chip ADCs, memory, and programmable digital control
  - Work has expanded to multiple other projects, see talks by A.Quinn and B.Parpillon and L.Rota

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