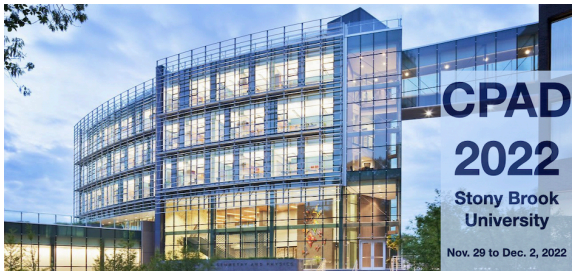

Contribution ID: **146** Type: **Contribution Talk**

Sub-electron skipper-CCD readout with multi-channel cryogenic low-noise readout ASICs

Thursday, 1 December 2022 09:30 (20 minutes)

The MIDNA series of application specific integrated circuits (ASICs) are cryogenic skipper-CCD readout chips fabricated in a 65 nm LP CMOS process and intended for the OSCURA dark matter detection project. Each MIDNA ASIC integrates four front-end channels designed to interface with four of the 4000 skipper-CCDs that make a 28 gigapixel dark matter detection camera. Each channel is less than 0.2 mm² and achieves an equivalent noise charge of 1 e⁻_{rms} at 20 µs integration time in simulation. Taking advantage of the non-destructive readout capabilities of skipper-CCDs, the first chip, MIDNA 1, has demonstrated a CCD image readout with 0.2 e⁻_{rms} noise by averaging samples of each pixel. The averaging can be performed digitally, by sampling the output of the chip, or it can be performed in the analog domain by using the analog pile-up readout scheme, thus reducing the number of analog-to-digital conversions required per pixel. Both chips enable the scaling required by OSCURA by integrating readout channels containing a pre-amplifier, a DC restorer, and a dual-slope integrator. The channel has four gain settings to maximize dynamic range for a variety of CCD charge gains. The minimum integration time is 1 µs. The power consumption is 6.5 mW per channel plus 5.5 mW for auxiliary circuitry. The linear dynamic range is 3000 e⁻ in nominal gain. The temperature range is 84-120 Kelvin as required by the skipper CCD, and the input referred noise is less than 6 nV/√Hz at 10 kHz. The second iteration of the chip, MIDNA 2, additionally integrates a voltage reference, bias generation, and reference buffering on chip, which reduces channel to channel crosstalk.

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Session Classification: WG1: Solid State Detectors and ASICs

Track Classification: WG1: Solid State Detectors and ASICs