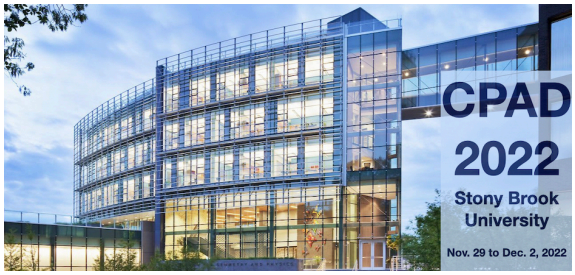

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Chip Development Toward 12 bit 10 GSPS Cryogenic ADC for Multiplexed Quantum Readout

Thursday, 1 December 2022 09:50 (20 minutes)

The ROADS (Readout of Analog Data Simultaneously) effort at Fermilab is a collaboration with Microsoft Quantum. The goal is to advance the state-of-the-art in cryogenic electronics for quantum computing applications, especially in highly scaled systems. The design objectives center around the development of a high-speed, high-linearity analog-to-digital converter (ADC) as part of a fully digital solution for frequency multiplexed readout. The ADC is targeted for 10 GSPS, 12 bit performance operating at 4 Kelvin based on an interleaved Successive Approximation Register (SAR) architecture. To date, the effort has taped out two chips using the GF 22 nm Fully Depleted Silicon-on-Insulator (FD-SOI) process. The first was the Mis-Match Test Chip which included test structures for a SAR ADC: a 6-bit capacitive digital-to-analog converter (DAC), bootstrapped switches, and source-follower readout. The chip has been tested and proven to be functional at cryogenic temperatures with good binary-scaled control, effective sampling from the bootstrapped switches, and acceptable readout performance. The second tape out was the Michigan chip, which is a development pathfinder prototype for the high-speed ADC and low-jitter PLL. Michigan included four SAR ADC channels with analog input buffering, a type II charge pump LC phase-locked loop (PLL), various clock generation circuits, and digital data handling with integrated memory. The fully programmable PLL runs at 10.24 GHz. The next chip, Glebe, will include further refinements of the designs. Full speed ADC slices will be interleaved to achieve 10 GSPS, and a double-sampling PLL that employs a cryo-VCO with common mode resonance technique is being developed. Specific performance metrics and figures of merit can be presented at the workshop.

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