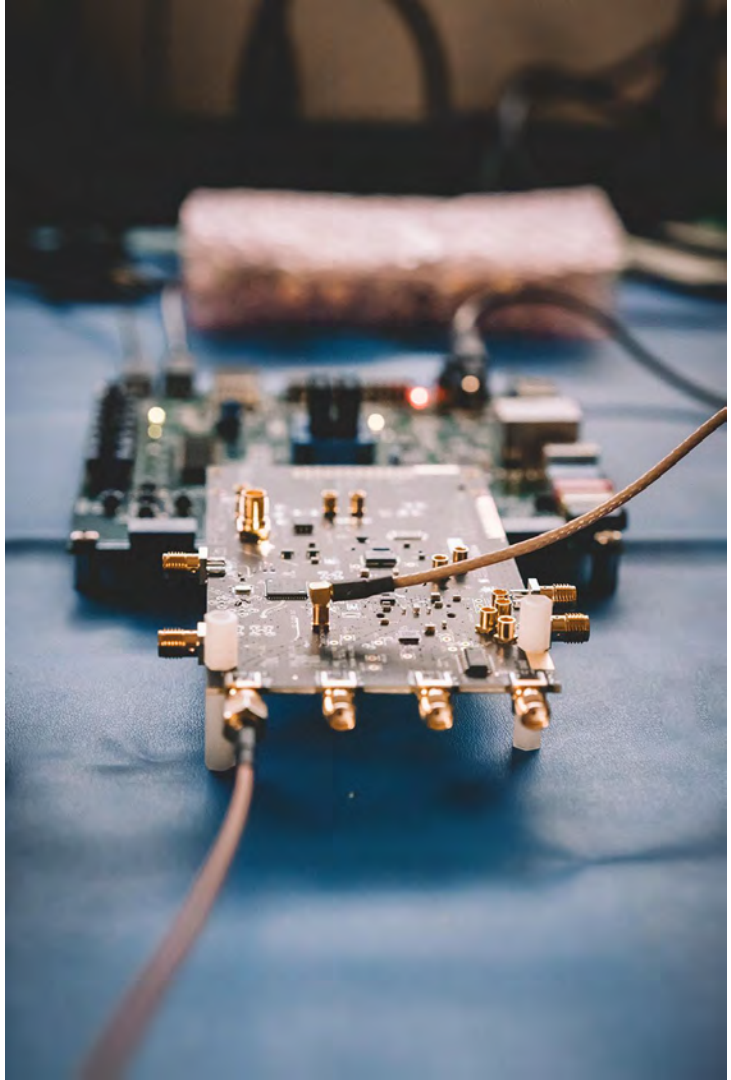


NALU SCIENTIFIC
ENABLING INNOVATION

Waveform Digitizing Electronics for Reading out Next Generation Detectors

Nov 29, 2022
Isar Mostafanezhad, Ph.D.
Founder and CEO at Nalu Scientific LLC

Work partially funded by US DOE SBIR Grants:

DE-SC0015231, DE-SC0017833, DE-SC0020457

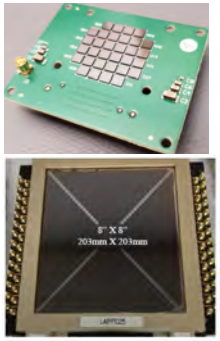
https://indico.bnl.gov/event/17072/contributions/70717/

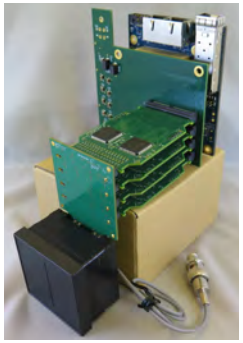
Outline

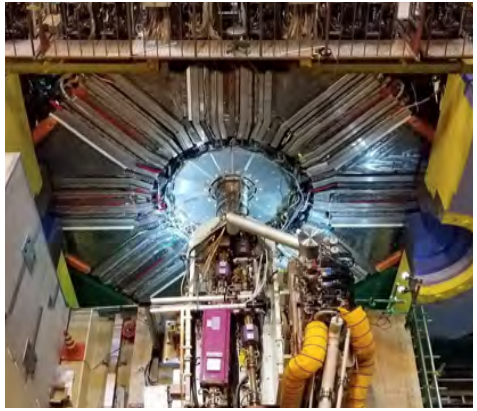
- **Introduction**
- **Digitizer Chip Development:**
  - HDSoC
  - HPSoC
- **Integration Efforts**
  - Benchtop digitizers
  - Sensor integration
- **Conclusions**

NALU SCIENTIFIC
ENABLING INNOVATION

WAVEFORM DIGITIZER SoCs
FOR PRECISE TIME OF FLIGHT ESTIMATION







1. Front-end Chips:

- Event based digitizer+DSP
- 4-32 channel scope on chip
- 1-15 Gsa/s, 12 bit res.
- Low SWaP-C
- User friendly: FW/SW tools

2. Integration:

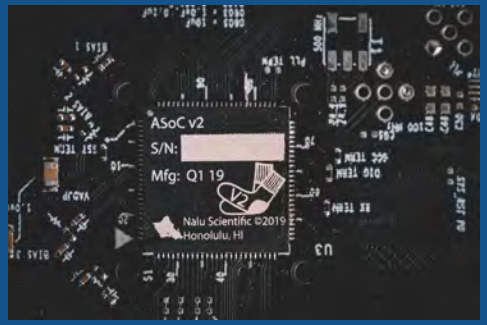
- SiPM
- PMT
- LAPPD
- Detector arrays

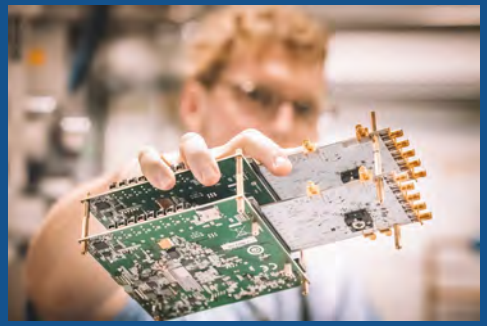
3a. Main application:

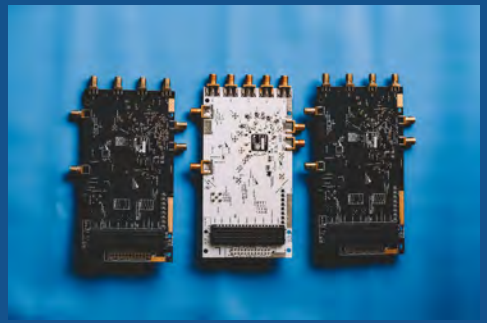
- NP/HEP experiments
- Astro particle physics

3b. Other applications:

- Beam Diagnostics
- Plasma/fusion diagnostics
- Lidar
- PET imaging







ABOUT NALU SCIENTIFIC

Agile Small Business in Honolulu, Hawai'i

- Located at the Manoa Innovation Center near U. of Hawaii
- 20 staff members-diverse background
- Access to advanced design tools
- Rapid design, prototyping and testing

Technical Team:

IC design (7x)	Analog + digital System-on-Chip (SoC)
Hardware design (3x)	Complex multi-layer PCBs
Firmware design (3x)	FPGAs, CPUs
Software design (4x)	GUI, analysis, documentation
Scientific (3x)	Plasma, medical, HEP/NP physicists

Exclusive Distributor Agreement for North America

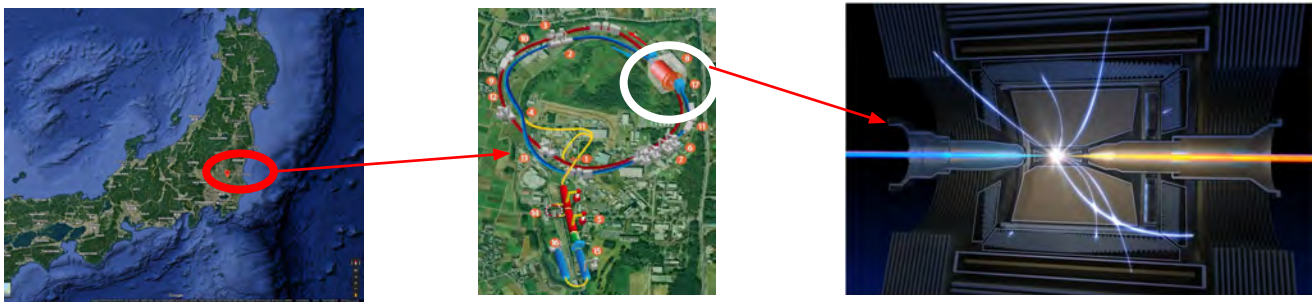
- Sales of ASICs, eval boards
- Enhanced OEM opportunities

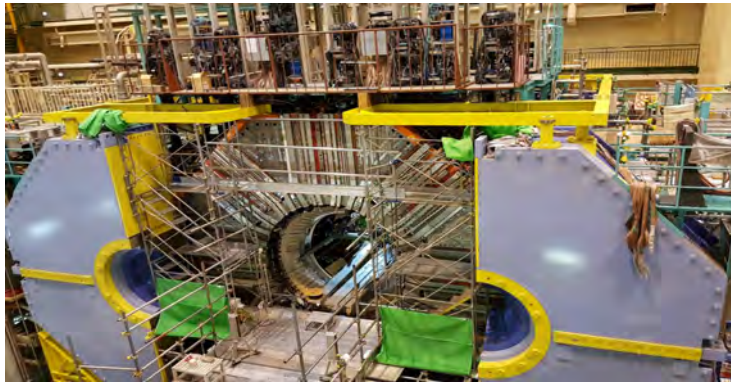
CAEN Technologies Inc.

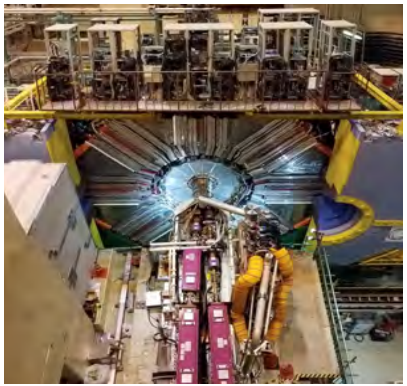
Nalu = 'wave' in native Hawaiian language

How we got started - BELLE II

Belle II Upgrade was a 26+ Country, 900 Member Collaboration







2015 **2018**

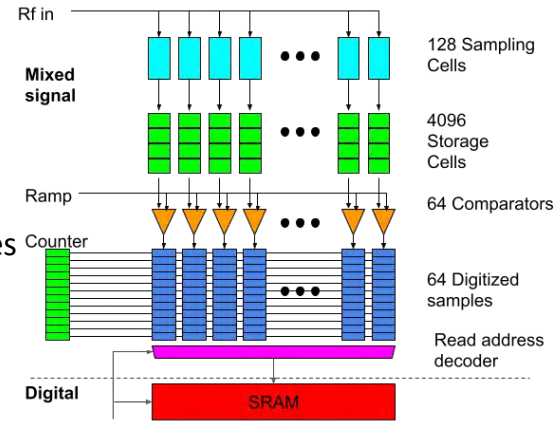
Nalu Staff designed and implemented front-end electronics and FW for KLM (muon system) and iTOP (Cerenkov-based PID) sub-detectors.

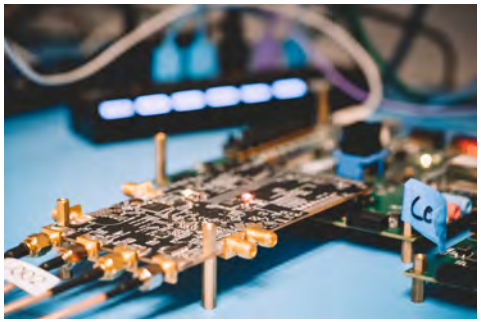
Belle II: e+ e- experiment at 40x luminosity of Belle -> Detector needs to operate at severe beam background. L1 trigger at 30 kHz./

Current SoC-ASIC Projects

Project	Sampling Frequency (GHz)	Input BW (GHz)	Buffer Length (Samples)	Number of Channels	Timing Resolution (ps)	Available Date
ASoC	3-5	0.8	16k	4	35	Rev 3 avail
HDSoC	1-3	0.6	2k	64	80-120	Rev 1 avail
AARDVARC	8-14	2.5	32k	4	10	Rev 3 avail
AODS	1-2	1	8k	1-4	100-200	Rev 2 avail
UDC	8-10	1.5-2	4k	16/32	10	Rev 1 avail

- Waveform digitizing benefits:
  - Pileup, sensor damage
  - Feature extraction
- Readout size and power is constrained
- No one form fits all:
  - Various sensor arrays and densities
  - Analog pre-processing
  - Timing resolution
  - Types of features





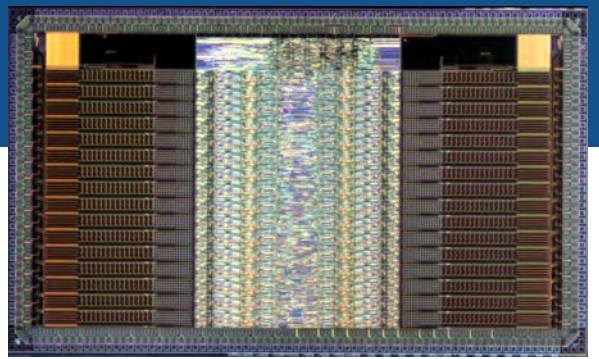
HDSoC V1 DESIGN DETAILS

High density waveform digitizer with dead-timeless readout

- High Density: 64 channels (V1:32, V2:64)
- Highly integrated, SiPM gain + bias
- Commercially available, low cost CMOS

Parameter	Spec
Sampling Rate	1-2 GSa/s
ABW	> 600MHz
Depth	2k Sa
Trigger Buffer	~2 us*
Deadtime	0**
Channels	64
Supply/Range	2.5
ADC bits	12
Timing accuracy	80-120ps
Technology	250 nm CMOS
Power	20-45mW/ch

- On chip calibration
- Serial interface
- On chip feature extraction
- Virtually dead-timeless
- 32 ch proto chip fabricated
- Phase II SBIR in progress
- Rev 1 Chip under test
- Next steps: more testing, rev 2 fab

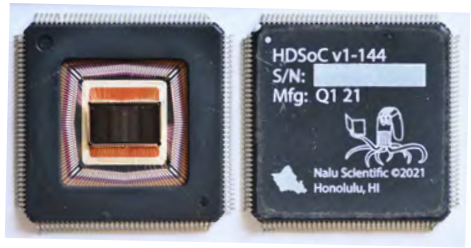


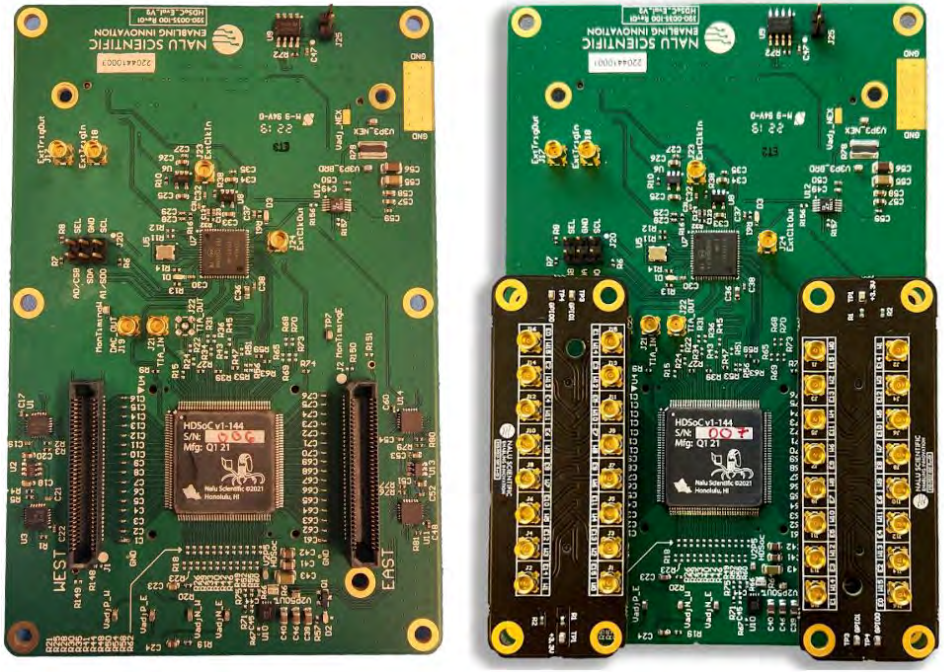
HDSoC v1 die shot

** Simulated Up to 240 KHz / ch with single serial link using on-chip self trigger and feature extraction.
Up to 400 kHz / ch with additional serial links.

HDSoC

- **V1 Fabrication:**
  - 32 channel prototype fabricated
  - 144 pin package purely for bring-up
  - Smaller QFN-100 available for integration
- **V1 Testing:**
  - FMC eval card under testing
  - FW, SW developed
  - Timing generators works well
  - All channels can digitize and readout
  - TIAs work, need more tests
  - All digital functions and serial link ok
  - Bias and readout SiPMs
- **V2 Design/Fab:**
  - 64 channels,
  - 144 pin LQFP
  - Available ~ March 2023

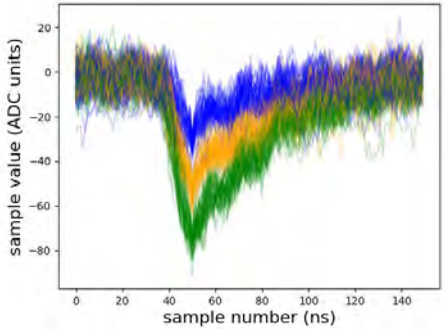


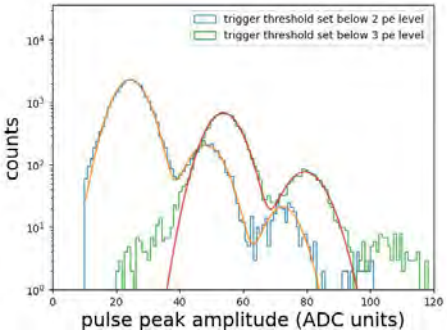


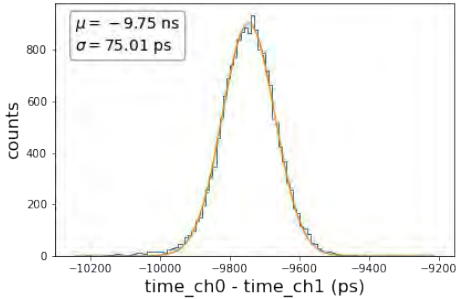
New FMC Eval board with High Density Connectors and breakout

HDSoC

- **Energy deposited by optical photons/photoelectrons (PEs):**
  - Onsemi J-Series 4x4 array of 3 x 3 mm2 SiPMs
  - HDSoC V1 channel 0 was set to trigger on signals corresponding to two PEs and above
  - 2, 3 and 4 PEs resolved at 24.4 ± 4.7, 48.2 ± 4.9 and 72.3 **± 4.7 ADC units**
-
- **Inter-channel timing measurements:**
  - Two copies of 100 MHz 450 mV unipolar sine burst, generated from a signal generator, sent to channels 0 and 1 of HDSoC V1
  - Delay of about 10 ns set between the two signals
  - Timing calibration performed using bin-occupancy fraction method on channels 0 and 1 using same data
  - Standard deviation of 75 ps observed in the distribution of difference in time-of-arrival of two copies of unipolar sine burst delayed with respect to each other



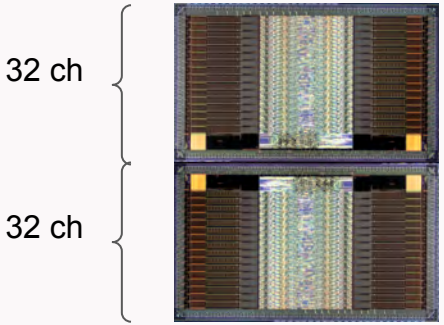


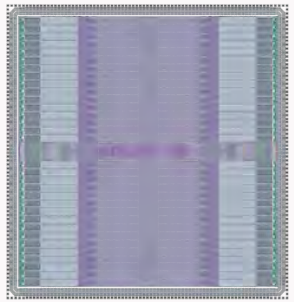


IEEE NSS-MIC 2022- Milan, Italy

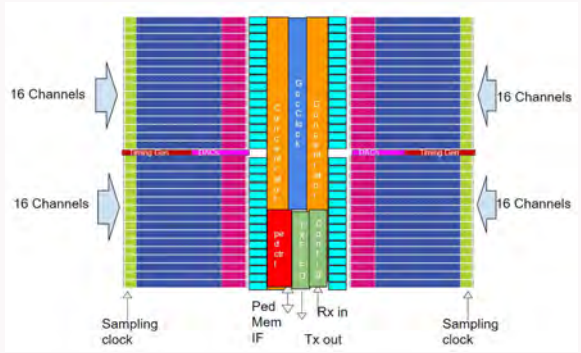
IEEE NSS/MIC Conf Oct 2021, conference paper available

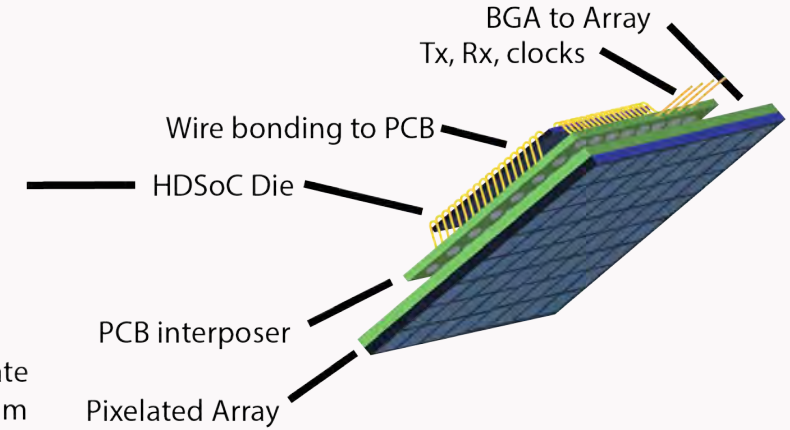
Moving to 64 ch HDSoC





Nalu Scientific
HDSoC V1 64 channel estimate
64 channel = 7.2 mm x 7.4 mm





Conclusions and future work

- **HDSoC v1**
  - All channels functional
  - Proper multi-window, multi-channel acquisition, self triggering, output streaming
  - Some issues with noise and power/ TIA BW
  - Boards available for testing for interested parties
- **HDSoC v2**
  - Available for testing by beginning 2023
  - HDSoC v1/2 may be used in beam tests for various EIC sub detectors
  - Opportunity to implement EIC specific (sensor, backend) needs in future revisions or branches
- **HDSoC is a novel, low cost, high channel count, high density, streaming readout capable, waveform-sampling ASIC** that can, in the words of our Letter of Support writers, significantly reduce cost, power, mass and volume in the design of readout systems optimized for use in large future detectors such as GEMs for TPCs, and for tracking and particle identification detector systems such as those being developed for EIC and other smaller detectors. The HDSoC is additionally well-suited for incorporation in portable radiation imaging systems such as for e.g. radiological source localization and identification, as well as portable detectors such as compact, high-efficiency neutron scatter cameras for non-proliferation and other national security missions.

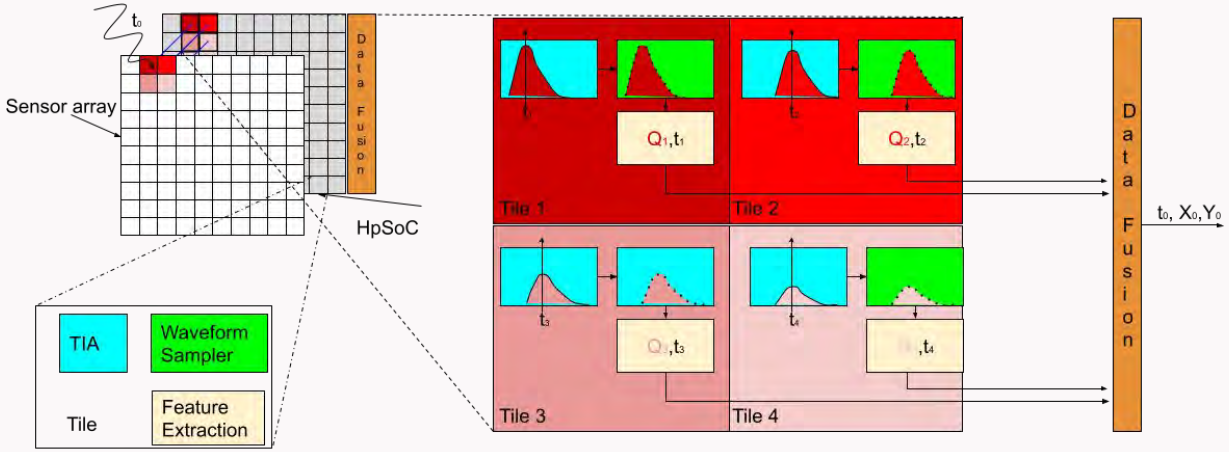
High Pitch SoC (HPSoC) - concept

- State of the art photodetectors (e.g. LGADs) -> excellent spatial and timing precision.
- Limited by existing readout electronics.
- Time-to-Digital Converter (TDC) and time-over- threshold (TOT) readout limitations:
  - Indirect estimate of integrated charge,
  - Limited sub-pixel spatial resolution
  - No correction for pile-up,
  - Sensitivity to sensor aging (radiation)
  - Time errors (timewalk, baseline wander, and waveform shape variations).
- Use full waveform information would solve all issues, but:
  - Expensive in area/power
  - Too large data BW required
- Proposed solution: HPSoC:
  - full waveform digitization per pixel,
  - On-chip feature extraction
  - On chip data fusion (sub-pixel spatial resolution)

Parameter	Specification	Comment
Channel no.	100+	(pitch 300-500 µm)
Sample rate	10 GSa/s	
Bandwidth	2 GHz	
No. bits	10	
Supply Voltage	1.0V	2.5V for digital I/O
Timing accuracy	5ps	With calibration
Front-End stage	Embedded TIA	Optimized for AC-LGADs and other fast sensors
Analog buffer length/channel	256	Effectively operating with a 2 banking system to allow for bursty signals
Power/channel	2mW	Trade-off with integration
Integration	System-on-Chip	Digitizer. Feature Extraction, data fusion

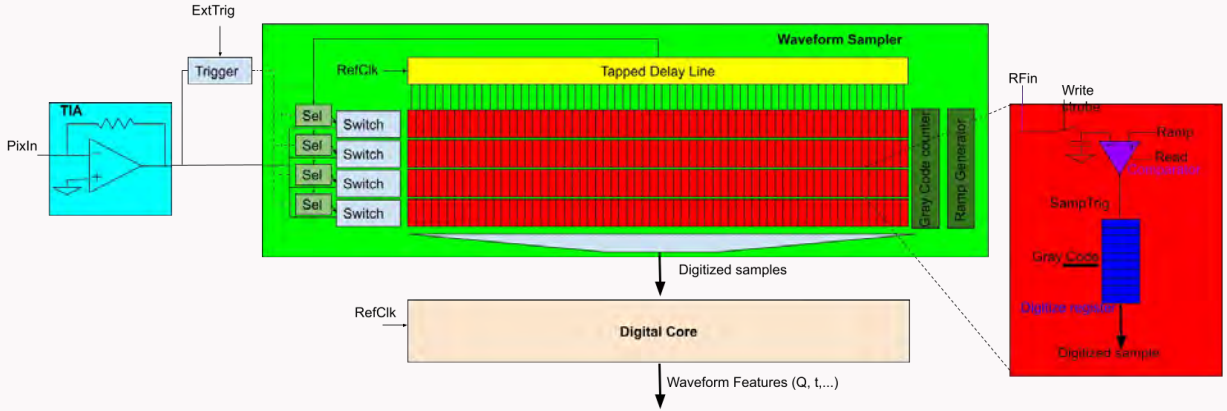
Target Structure

1. Dense sensor array readout (target of ~300um pitch)
2. Modular, independent (“tiles”), per pixel
3. On chip signal amplification (TIA+gain)
4. Continuous waveform sampling and triggered digitization - “ping-pong” operation to avoid deadtime.
5. On the fly timing and amplitude (charge) extraction
6. “Data fusion” and export.

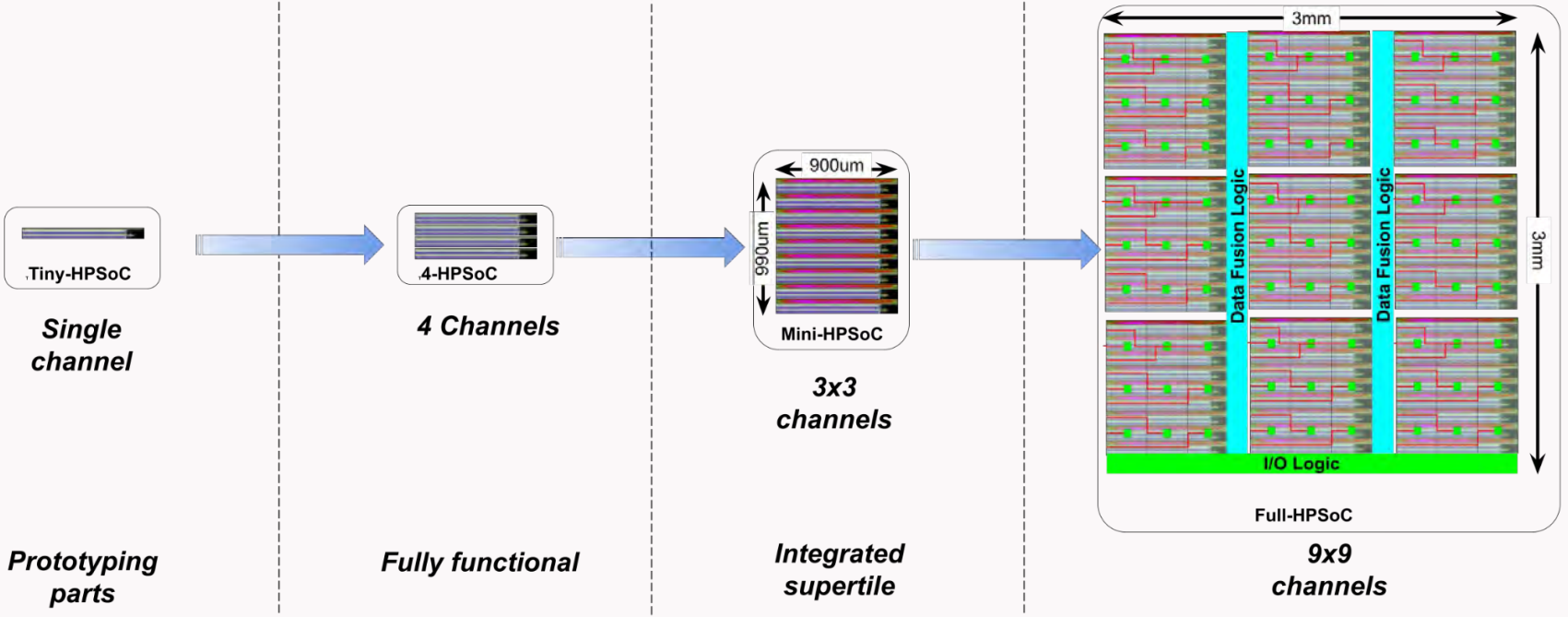


Channel Architecture

1. Input TIA (plus voltage buffer stage to drive sampling array)
2. Internal discriminator
3. Self triggering/selection of subsets of sampling array (controlled by trigger - performing “ping-pong” operation)
4. Sampling array continuously operating on a small set of samples (128), driven by local strobe generation via a tapped delay line
5. Internal comparator in sampling cell to perform on-the fly conversion (single ramp or “Wilkinson” ADC)
6. MUXing of data to digital core for further elaboration

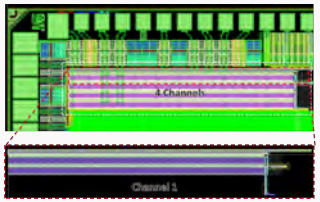


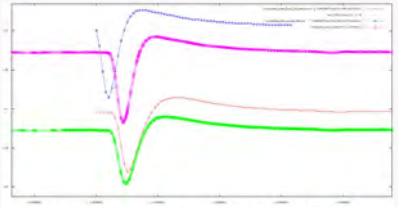
"Evolution" of HPSoC

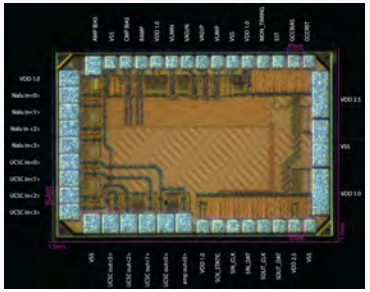


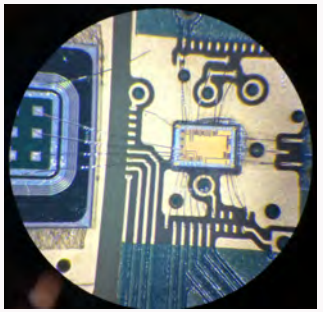
Status of project

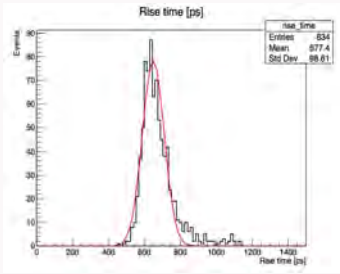
1. Pre-amplification stages: a TIA followed by wide-band gain stage: provide extra gain, can drive capacitive load (sampling array)
2. Mixed-Signal components: 3 different acquisition channels designed, laid out and manufactured.
3. HPSoC chip manufacturing and test - fabricated die with all features from 2 and 3
4. HPSoC test: 2 boards
   a. Front end testing - calibration and LGAD readouts (board design and testing performed by colleagues at SCIPP)
   b. Mixed signal (still ongoing)

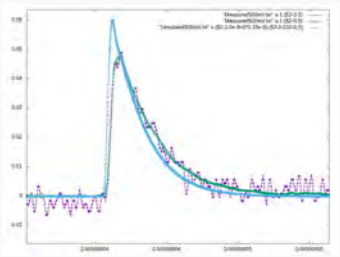


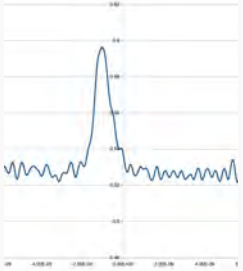




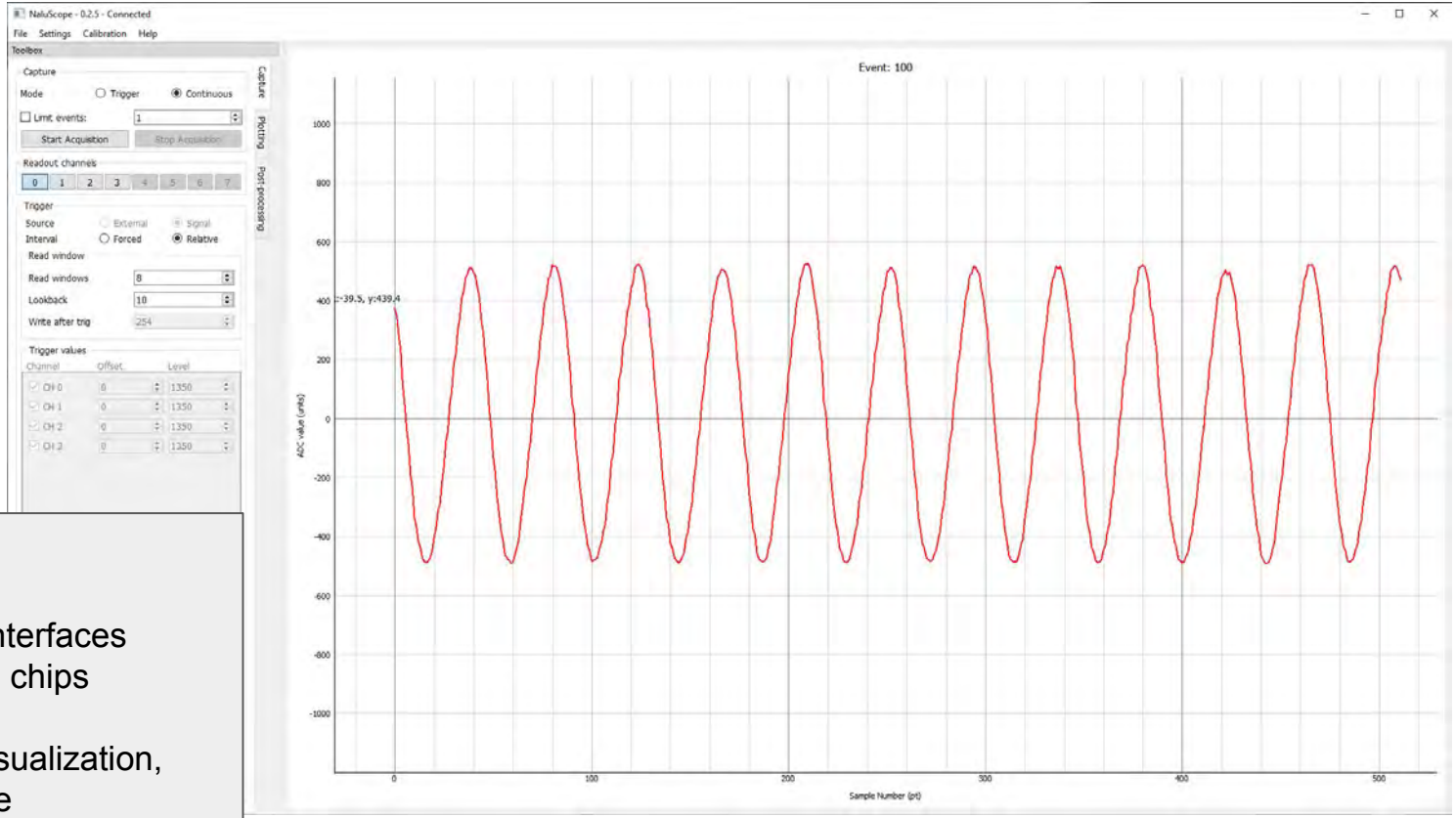






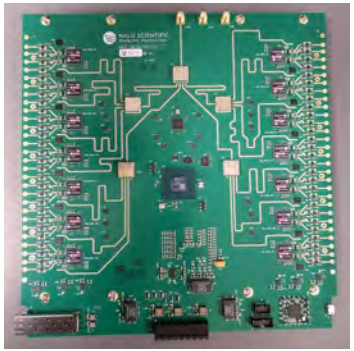


NaluScope Common Software and GUI

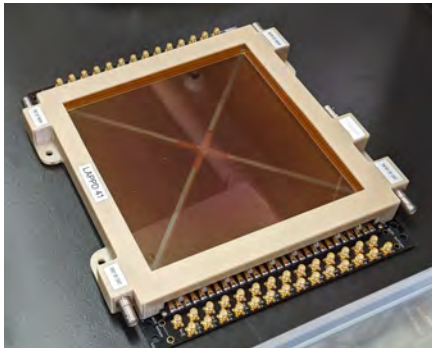


- Windows/Linux PC
- USB interface
- GUI, CLI/scripting interfaces
- Common to all Nalu chips
- DAQ configuration
- Data exploration, visualization, curation and storage
- Plug and play with eval cards

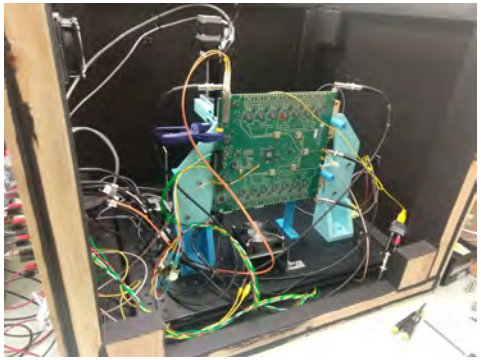
Integration efforts - HIPeR



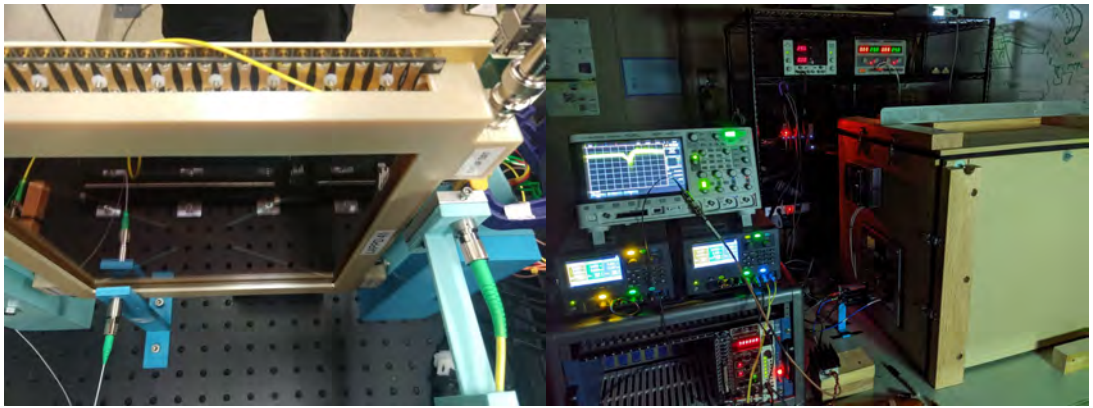
AARDVARC based readout

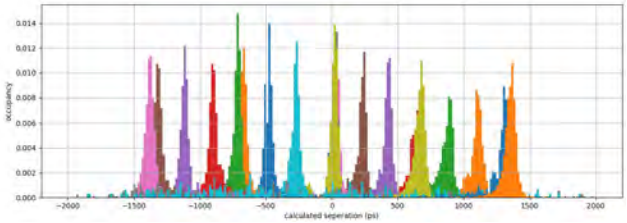


Incom's Gen 1 LAPPD



Integration and testing (UH)

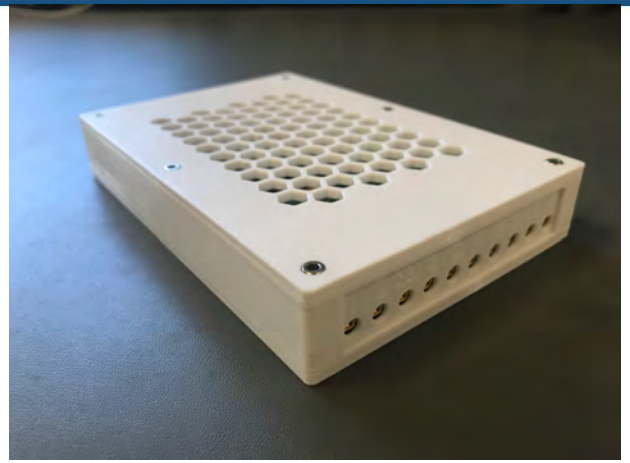


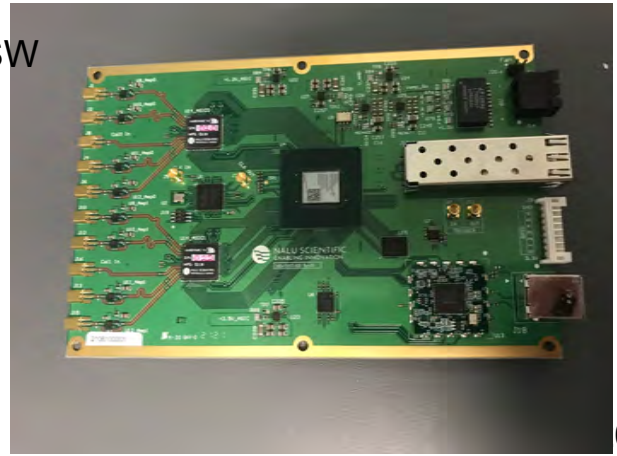


Nalu Scientific Phase I SBIR in collaboration with Incom and University of Hawaii.

8 Channel Digitizer Board using AARDVARC Chip

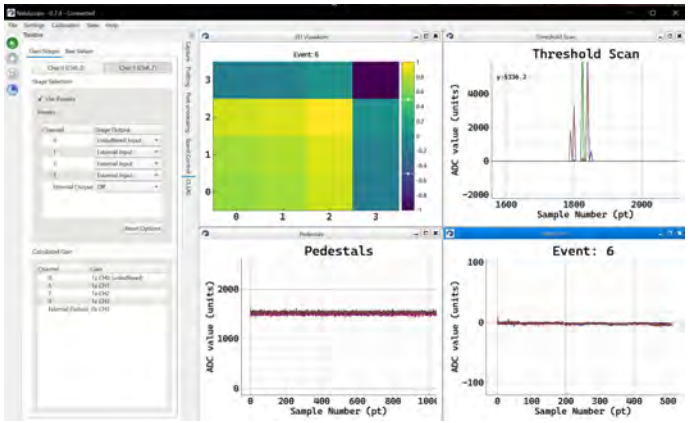
Product Name:	**DSA C10-8+**
Product Description:	8 channel, 10 GSa/s digitizer with built-in amplifier
Dimensions:	~ 6” x 4” x 1”
Gain:	19.5dB, replaceable
Bandwidth:	~1.8 GHz
Digitizer Chip:	AARDVARC V3
Sample rate:	9-14 GSa/s
Power:	USB
Data:	USB/UART, future ethernet
Integration:	Amps, chip, FPGA, clock, regulators, comm, FW, SW
Trigger:	Internal, External, Software

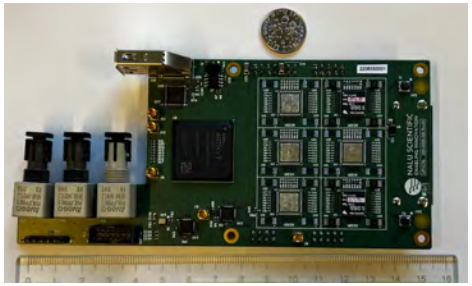


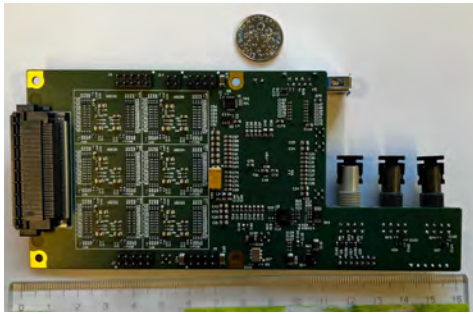


96-channel board using UDC - DSA E10-96

Product Name:	**DSA E10-96**
Product Description:	96 channel, 10 GSa/s digitizer
Dimensions:	~ 12” x 4” x 1”
Bandwidth:	~1.2 GHz
Digitizer Chip:	UDC V1
Sample rate:	9-12 GSa/s
Data:	USB 3/UART, future ethernet
Integration:	chip, FPGA, clock, regulators, comm, FW, SW
Trigger:	Internal, External, Software
Software:	GUI, script, Python

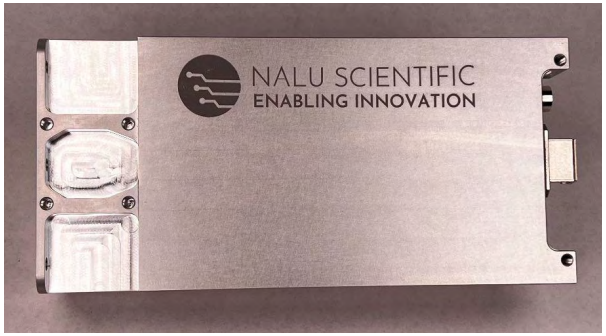






PCB

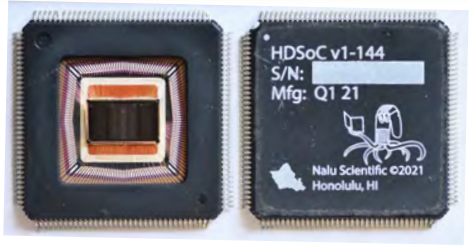
96 ch UFL breakout

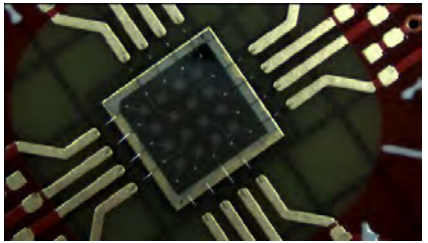


Enclosure

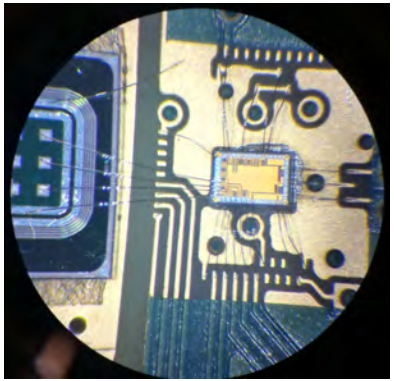
Conclusions

- **Products:**
  - Digitizer microchips
  - Hardware integration
  - Firmware and software
- **Services:**
  - Custom chip/HW design
  - Software and firmware design
  - Custom readout system development
  - Prototyping
- **Expertise:**
  - Electronics engineering
  - Radiation detection
  - Integration and testing
- **Collaborations:**
  - National Labs
  - Universities
  - Experiments

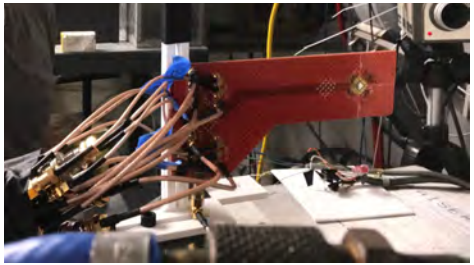


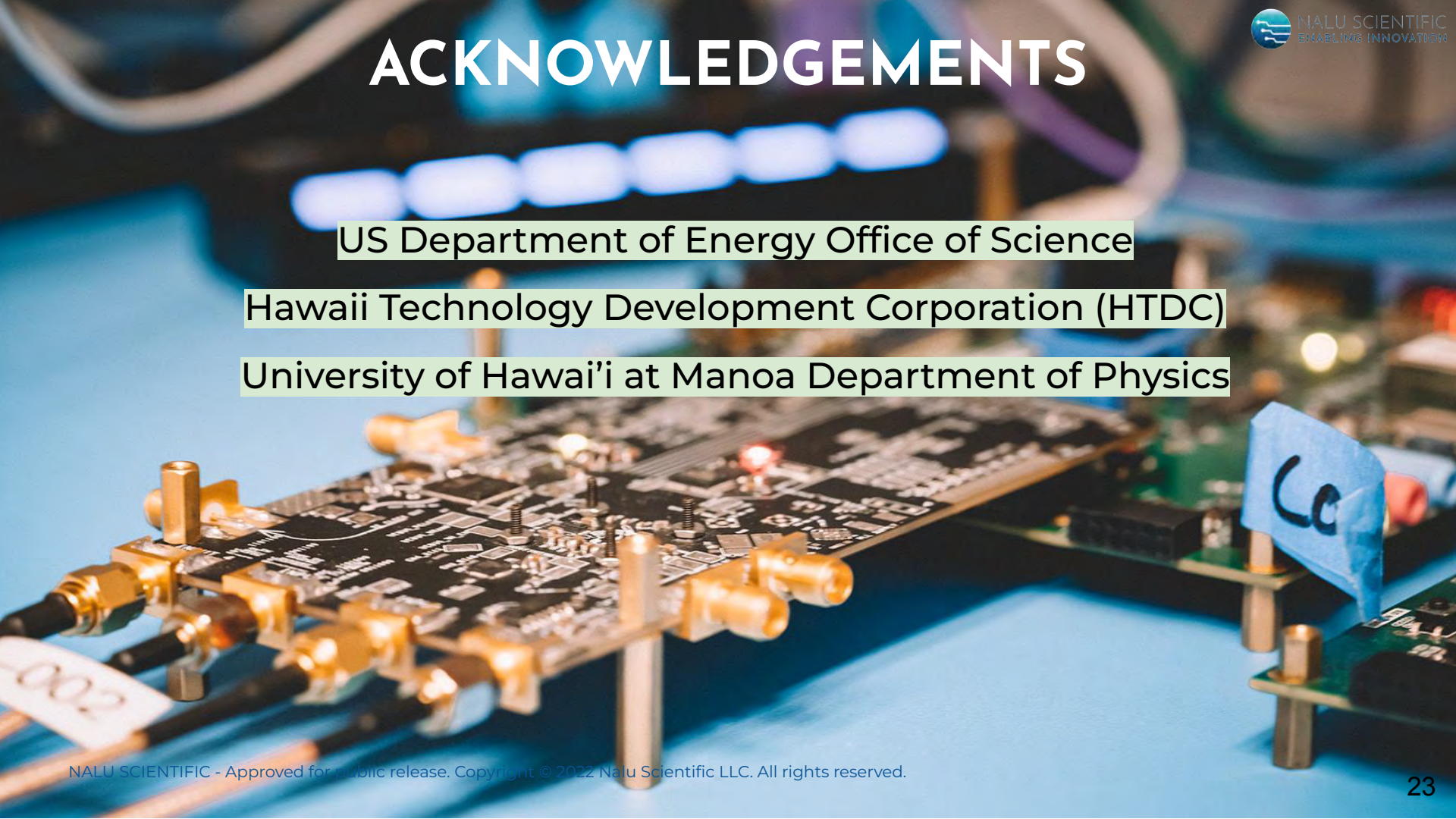


Diamond detector



AC-LGAD readout





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