Developments of ITkPixV1.1 module Quality Control tools

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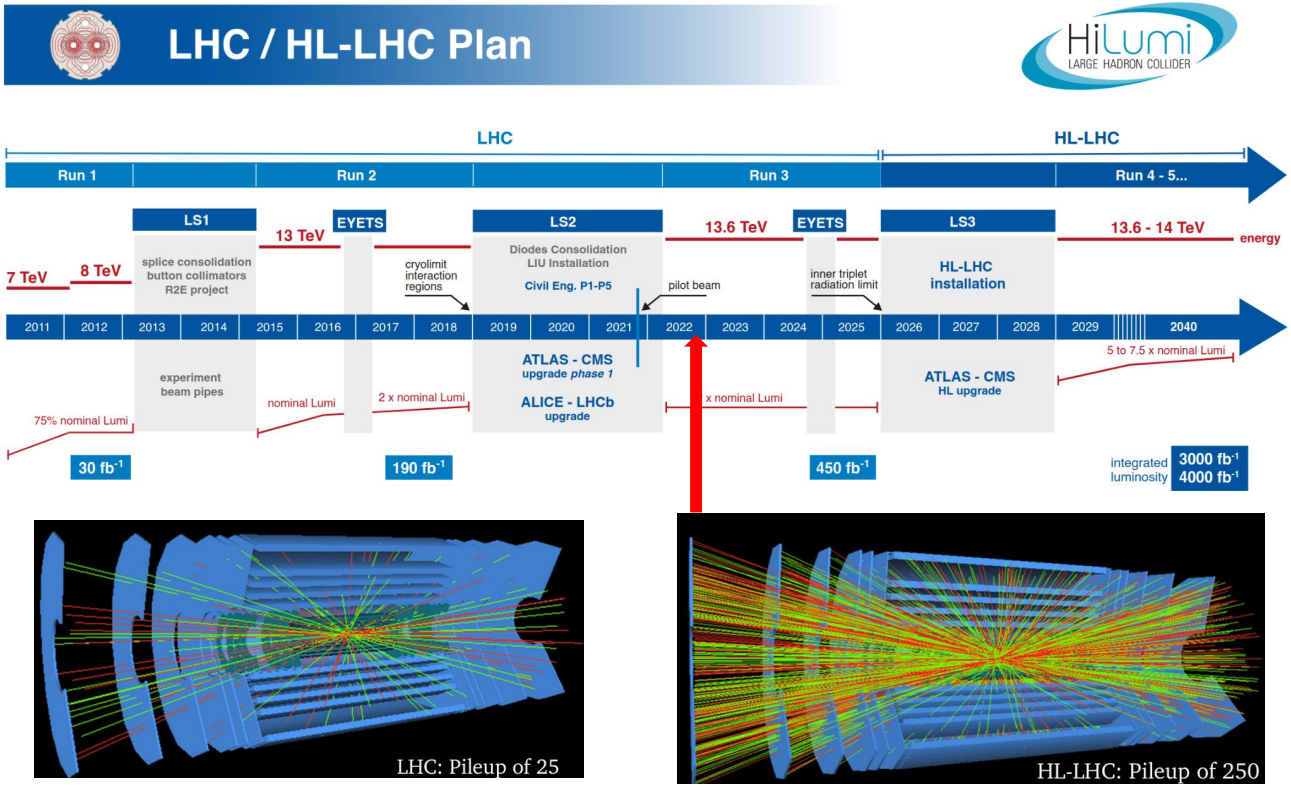
[5] CERN

Motivation - HL LHC Upgrade



High Luminosity (HL) LHC:

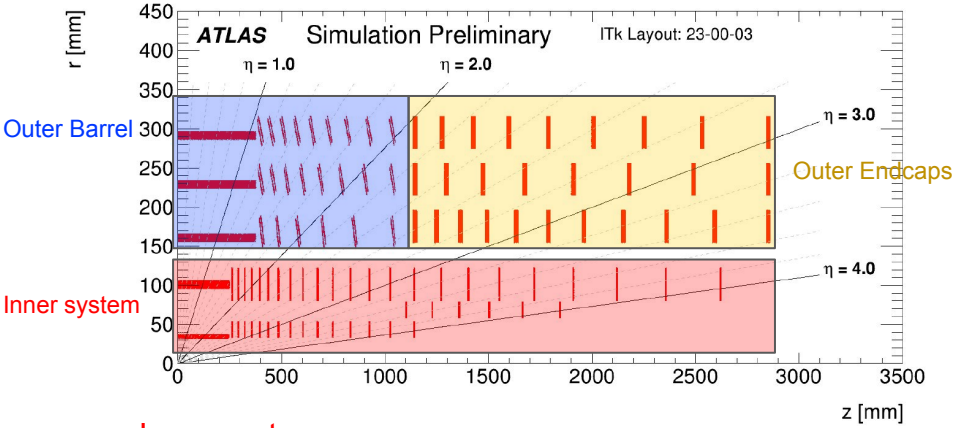
- Peak luminosity: $1 \cdot 10^{34} \rightarrow 5 - 7 \cdot 10^{34}$ cm^{-2} s^{-1}
- Average collisions/BC: ~60 → ~200

Upgrade the tracking system

-> Inner Tracker

ATLAS Inner Tracker (ITk) Upgrade

ITk Pixel Detector



Inner system:
2 barrel layers, staves L0 and L1
3 ring flavours, R0, R0.5 and R1
Outer Barrel:
3 layers, staves and inclined rings
Outer Endcaps:
3 layers of endcap rings

~9.2k modules

ATL-ITK-PUB-2021-024

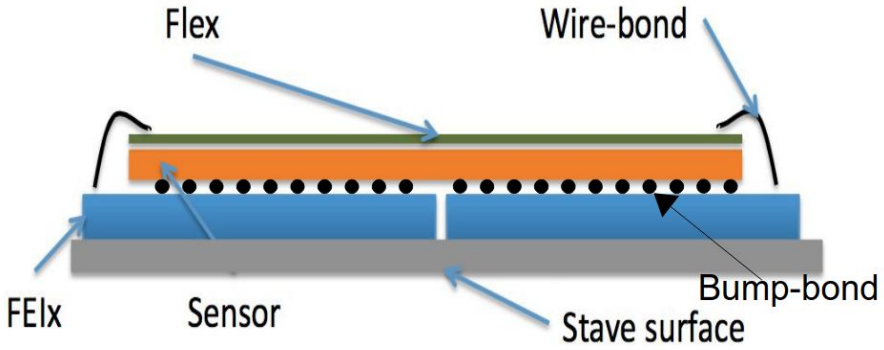
Replace current Inner Detector with all-silicon Inner Tracker(ITk), consisting of strip detector and pixel detector

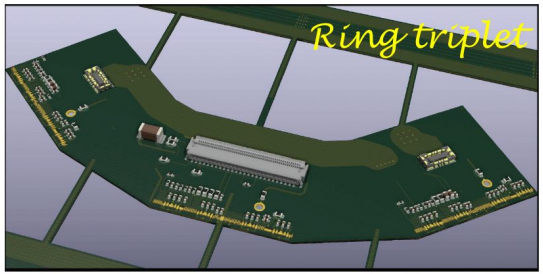
Advantages

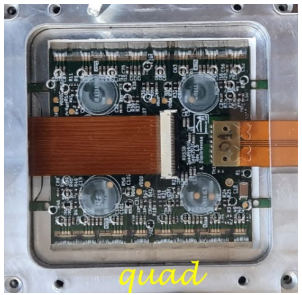
- Better radiation tolerance
- Reduced detector material
- Higher readout rates
- Extended detector acceptance to $|\eta|=4$
- Improved performance for high pT tracks

ITk pixel module

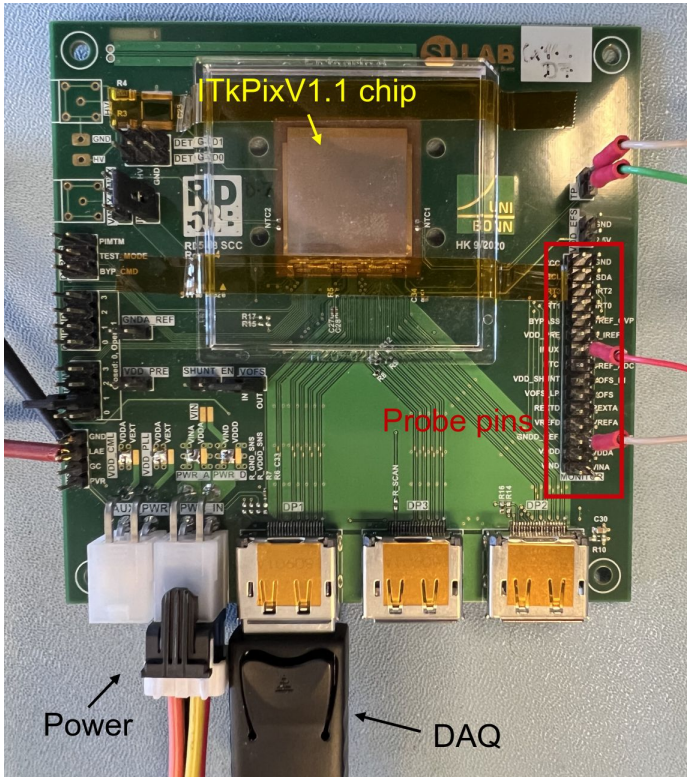
- module: silicon sensors are bump bonded to readout chips(front-end chips), then glued to a module hybrid(flex)
- Various sensor possibilities: 3D and planar
- Module options
  - Triplet module(the innermost layer, L0)
  - Quad module(other outer layers, L1-L4)







ITkPixV1.1 single chip card



- An ITkPixV1.1 chip mounted on a pre-printed circuit board
- Different internal voltages/currents can be easily measured through the probe pins
- Components (e.g. resistors/capacitors) can be easily replaced for various studies
- Serve as the first step before moving to more complex system (e.g. quad module)

ITkPix Module Electrical Quality Control

- Extensive electrical tests on pre-production chips/modules(ITkPixV1.1) have been performed to verify that design of module works as expected
- Need to develop procedures to calibrate and check the quality (Quality Control) of the module for (pre)production
  - ~ 25 institutes across the world will participate in the program
- Large statistics of pre-production modules will provide useful information on the components
  - Need to collect all results in single database to make global analysis on large statistic possible

So it’s important to develop common tools.

QC and calibration procedures for Pixel module

Still being developed, at the moment is composed of:

- Calibrate the ADC that digitizes the internal signals from the monitoring block (temperature, total ionizing dose, internal voltages or currents)
- Check the powering behavior of the chip
- Calibrate the injection circuit
- Check pixel efficiency and noise performance

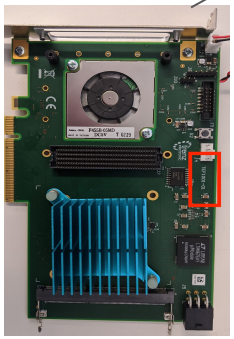
Will concentrate of first 3 type of measurements, the last one is controlled by the DAQ

Module QC Tools - Overview

- A common tool to perform electrical QC testing of ITkPixV1.1 module
- QC measurement and analysis tools are Python-based and independent packages
- Measurement package:
  - control benchtop hardware(like power supply and multimeter) and send commands or read back from DAQ
  - agnostic of the system used to control external hardware
  - produce output file containing raw measurements (voltages and counts)
- Analysis package:
  - use as input the output of measurement package and calculate important quantities from raw values
  - grade modules performances and identify which modules fail QC
  - produce output that can be stored in the production database

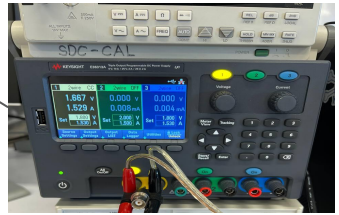
Module QC Tools - Schematics

Single chip card

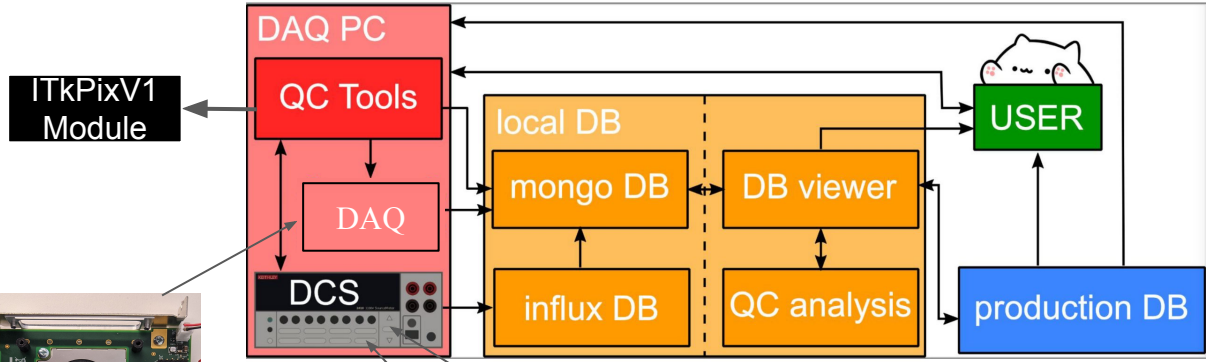


DAQ

Multimeter



Power supply



Module QC Tools - Workflow

1. Prepare json configuration use by measurement package to control DAQ and benchtop hardware

"yarr"(the DAQ system): YARR configuration, chip controller and connectivity files

Hardware control: Controlof power supply, multimeter, and temp measurement from NTC

"Tasks": detailed settings for each electrical test

```
"yarr": {
        "run_dir": "../Yarr",
        "controller": "configs/controller/specCfg-rd53b-16x1.json",
        "connectivity": "configs/20UPGR91301046/20UPGR91301046_LP.json",
        "scanConsole_exe": "./bin/scanConsole",
        "write_register_exe": "./bin/write-register"
},
"power_supply": {
        "run_dir": "../labremote_devel/scripts",
        "on_cmd": "python control_PS.py -i {i} -v {v} -a on",
        "off_cmd": "python control_PS.py -a off",
        "set_cmd": "python control_PS.py -i {i} -v {v}",
        "getI_cmd": "python control_PS.py -a getI",
        "getV_cmd": "python control_PS.py -a getI"
},
"multimeter": {
        "run_dir": "../labremote_devel/scripts",
        "dcv_cmd": [
                "python measureV.py -c 0 -p /dev/ttyUSB1 -a 1"
        ]
},
"ntc": {
        "run_dir": "../labremote_devel/scripts",
        "cmd": "python measureT.py"
},
"tasks": {
```

Module QC Tools - Workflow

1. Prepare json configuration use by measurement package to control DAQ and benchtop hardware
2. Perform measurement → output: measurement json files
    - Write measured quantities into output files
        i. Chip identifier and other metadata
        ii. No manipulation of measured data (Raw measurements)

Module QC measurement tool

Module QC Tools - Workflow

1. Prepare json configuration use by measurement package to control DAQ and benchtop hardware
2. Perform measurement → output: measurement json files
   - Write measured quantities into output files
     i. Chip identifier and other metadata
     ii. No manipulation of measured data (Raw measurements)

Module QC measurement tool

3. Perform analysis → input: measurement json files. output: plots for user, output files for database
   - Calculations are performed in this step
     i. Voltages read from multiplexer → real quantities
   - Data processing, e.g. fitting

Module QC analysis tool

Module QC Tools - Electrical tasks

Tools developed so far:

1. ADC calibration
2. VCal calibration
3. SLDO VI scan
4. Injection Capacitance
5. Analog read back & temperature measurement

Electrical QC Task - ADC Calibration

- Motivation:
  - Internal 12-bit ADC is used to read out the voltages on the monitoring multiplexer (MUX)
  - Useful to monitor the global registers, and monitor the chip status by reading out ADC (Analog-Digital-Converter) values through software

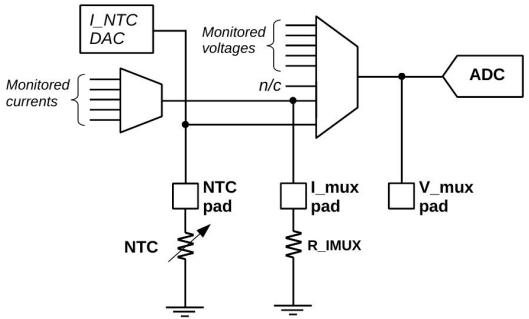


Figure 65: Diagram of monitoring block with current and voltage MUXes feeding the input of the ADC.

The ADC digitized output depends on the input and references voltages:

$$\mathrm{ADC_{out}} = A \times \frac{V_{in}}{\mathrm{Vref\_ADC}} + B + \text{nonlinear terms} \qquad (12.1)$$

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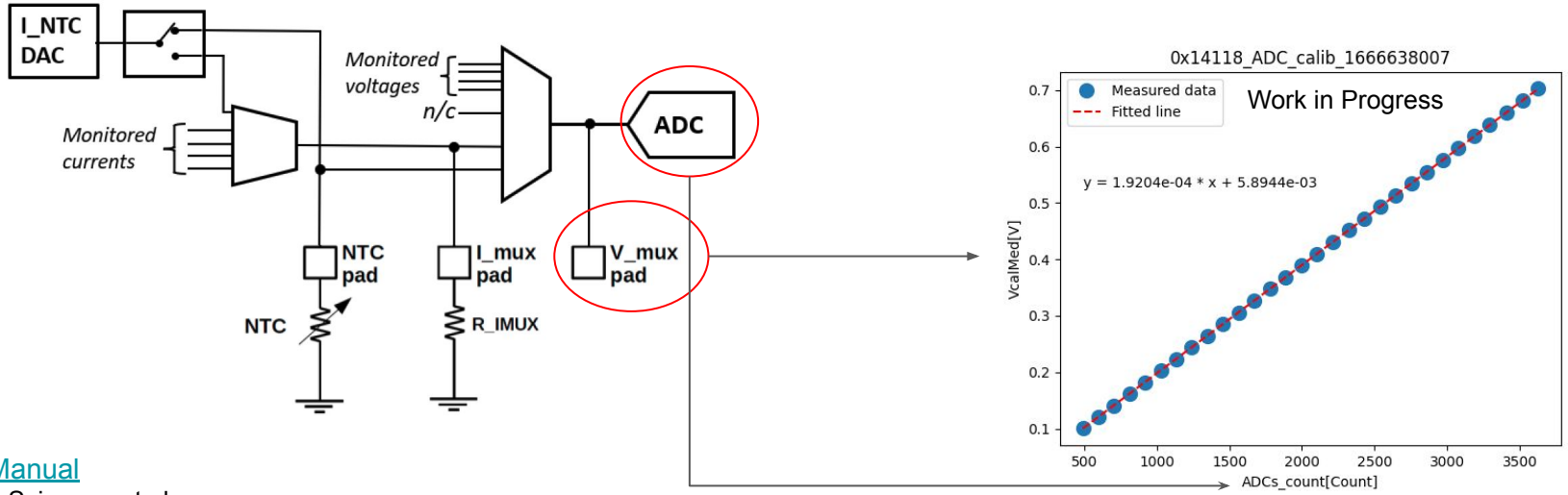
Electrical QC Task - ADC Calibration

- Goal: calibrate ADC so that all voltages and currents can be measured via the VMUX output through ADC
- Fit the measured data by a linear line
- Calibration compared to wafer probing data



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Electrical QC Task - VCal Calibration

- Vcal digital-to-analog converter(DAC)
  - Controls the injection circuits
  - Generated by two 12-bit DACs Vcal_high and Vcal_med
  - Each DAC has can operate in two ways: with high dynamic range or with small range but fine step size

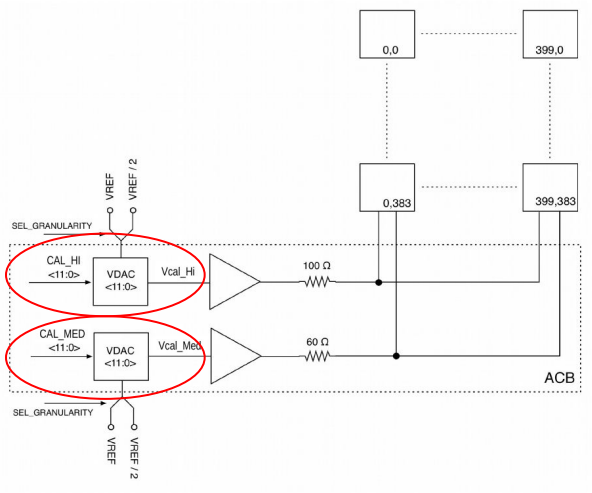
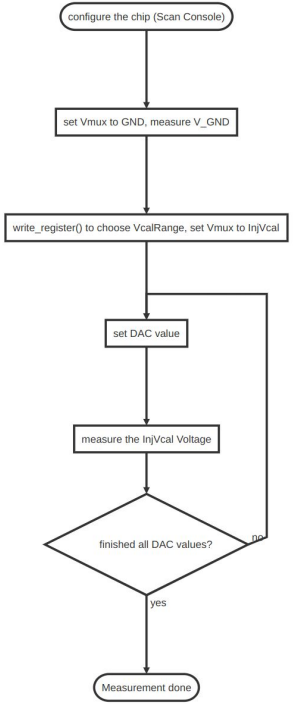
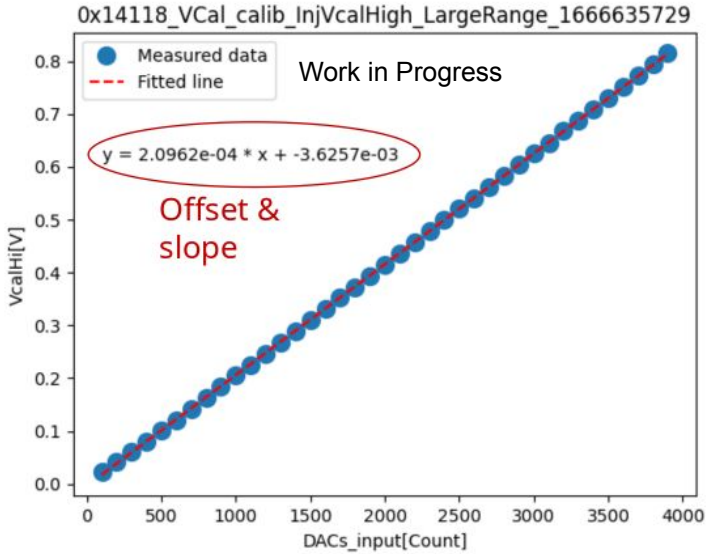


Figure 38: Generation of the injection voltages Vcal_Hi and Vcal_Med.

Electrical QC Task - VCal Calibration

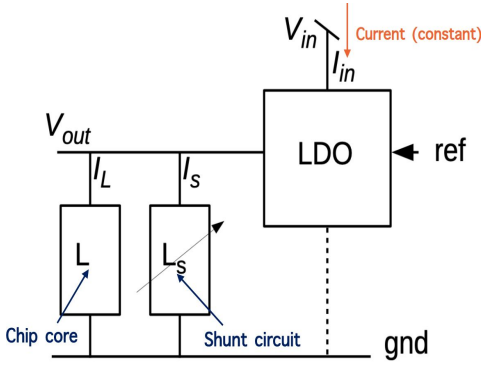
- Goal: calibrate DACs for both operational types, compare to wafer probing





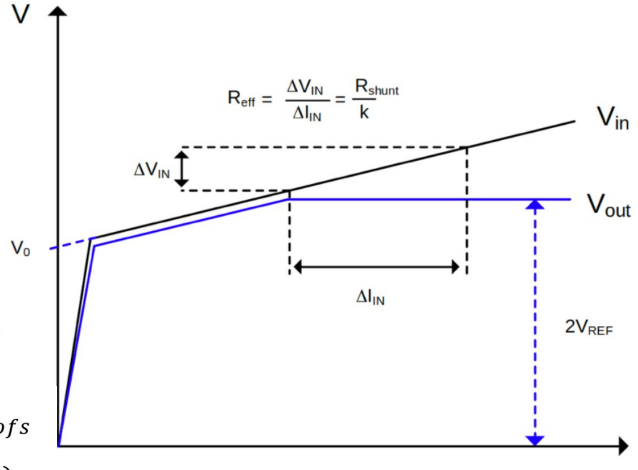
Electrical QC Task - SLDO VI scan

- The Shunt LDO regulator (SLDO) provides constant current operation with multiple chips connected in parallel
- Goal: verify if the performance of the SLDOs consistent with theory prediction



$$I_{in} = I_L + I_s = \frac{V_{in} - V_0}{R_{\text{eff}}} \longrightarrow V_{theory}(I_{in}) = R_{eff} \times I_{in} + V_{ofs}$$

$$R_{eff} = 1 \,/\, (\frac{k_A}{R_{ext,A}} + \frac{k_D}{R_{ext,D}})$$



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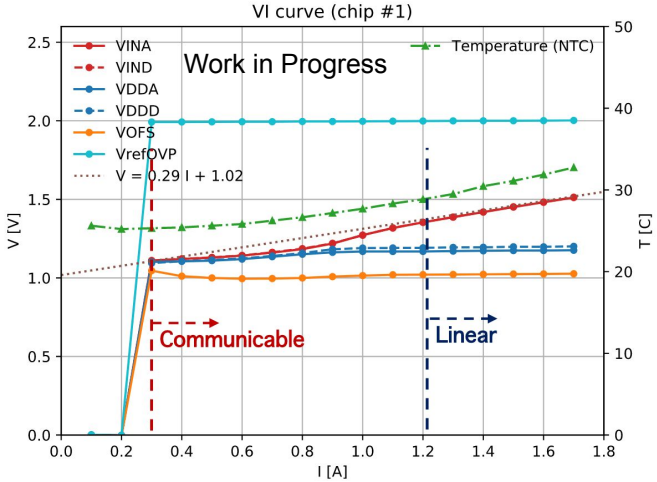
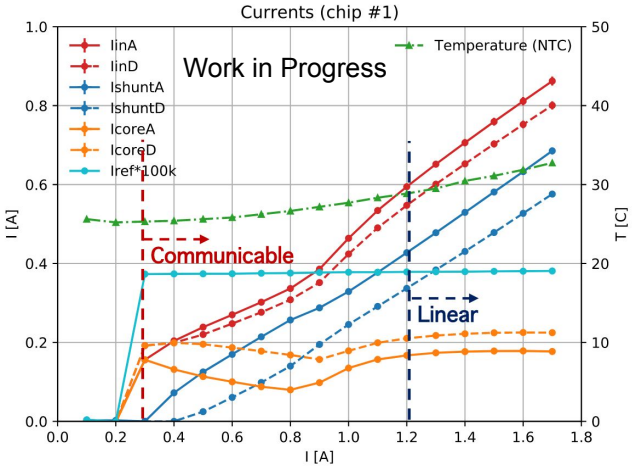
Electrical QC Task - SLDO VI scan

- Minimum current at which the SLDO is fully operational is smaller than threshold value(1.6A for low power config)
- For all currents above I_{in}^{min}, the VI curve is linear and follows the theoretical prediction (dashed line)





Electrical QC Task - Injection Capacitance

- The injection circuit is implemented in every pixel
  - Inject a known charge and record the response of pixel
  - Injected charge depends on ΔV and C_{inj}
- Each chip is equipped with a dedicated circuit to measure injection capacitance: capmeasure circuit

$$C_{meas} = 100(C_{pix} + \Delta C) + C_{par}$$

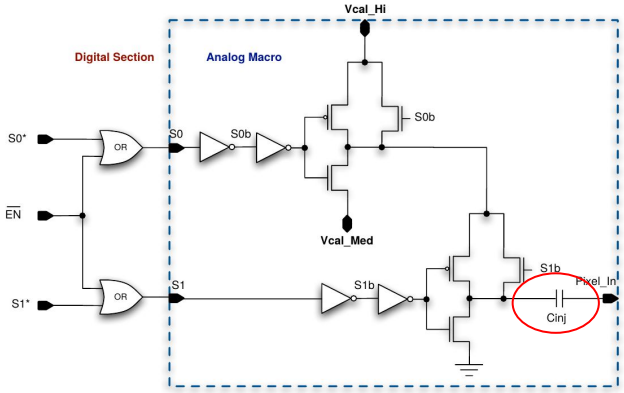
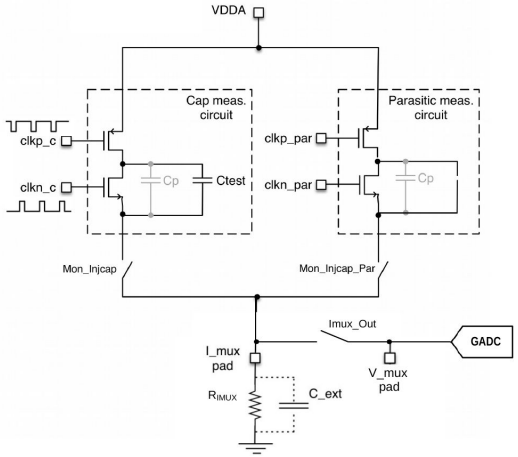


Figure 31: Calibration injection circuit in each pixel. The injection capacitor nominal value is 8.02 fF.



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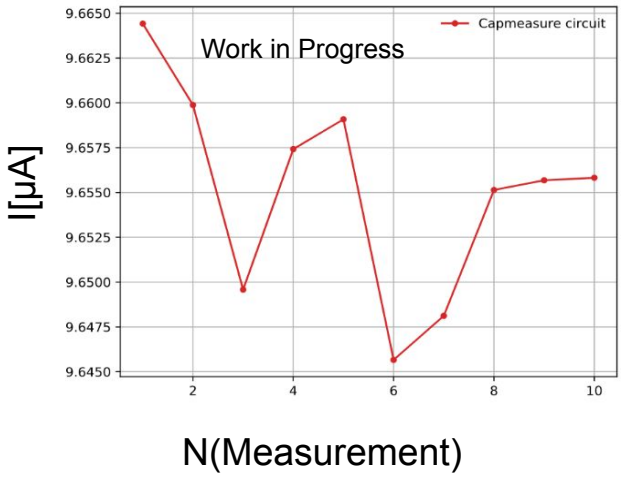
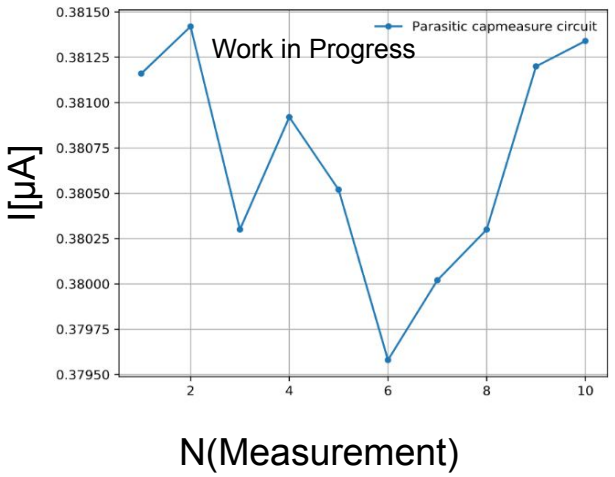
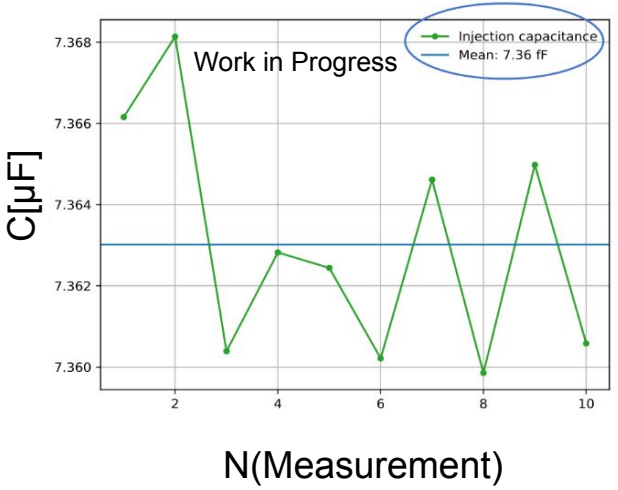
Electrical QC Task - Injection Capacitance

$$C_{meas} = 100(C_{pix} + \Delta C) + C_{par}$$



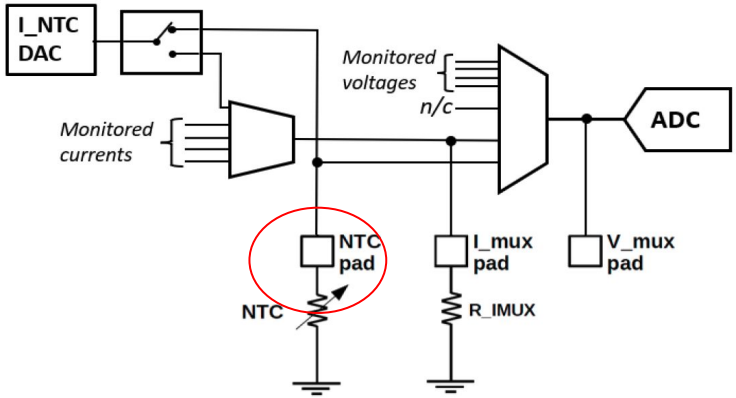


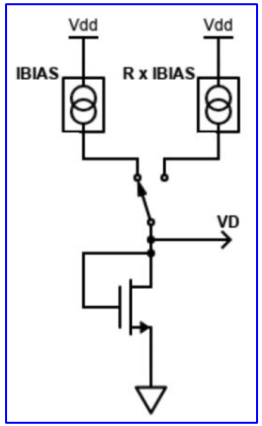


Compare average C_{pix} (7.36 fF) to nominal value (8.03 fF) → this SCC (3D, unbiased) has C_{pix} 8% lower than nominal

Electrical QC Task - Analog readback & T

- Measure internal voltages
  - Measure and record the readings from interesting Vmux and Imux channels
  - Allows us to access the status of the chip from module testing to module being integrated into local support
- Measure chip temperature
  - Compare the temperature measurements from external NTC and MOS temperature sensor
  - Check if the internal sensor is functional





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Electrical QC Task - Analog readback & T

- External NTC

$R_{ntc} = V_{ntc} / I_{ntc}$ $T = 1/(A + B\ \ln(R_{ntc}) + C\ (\ln(R_{ntc}))^3)$

Vntc (V)	Intc (A)	Rntc (Ω)	T Ext NTC (℃)
0.0735	1.096E-05	6708	**35.78**

Work in Progress

- MOS temperature Sensors

$\Delta V_D = V_D(R \times I_{bias}) - V_D(I_{bias}) = N_f \times k_B T / q \times \ln(R)$

$T = \Delta V_D \times q / (N_f \times k_B \times \ln(R))$

Work in Progress

	Vmux14 ana. SLDO		Vmux16 dig. SLDO		Vmux18 center	
Bias	**0 (IBAIS)**	**1 (R x IBAIS)**	**0 (IBAIS)**	**1 (R x IBAIS)**	**0 (IBAIS)**	**1 (R x IBAIS)**
Average VMUX (V)	0.1994	0.2904	0.1993	0.2904	0.2039	0.2948
T (℃)	**35.07**		**35.57**		**35.10**	

Summary

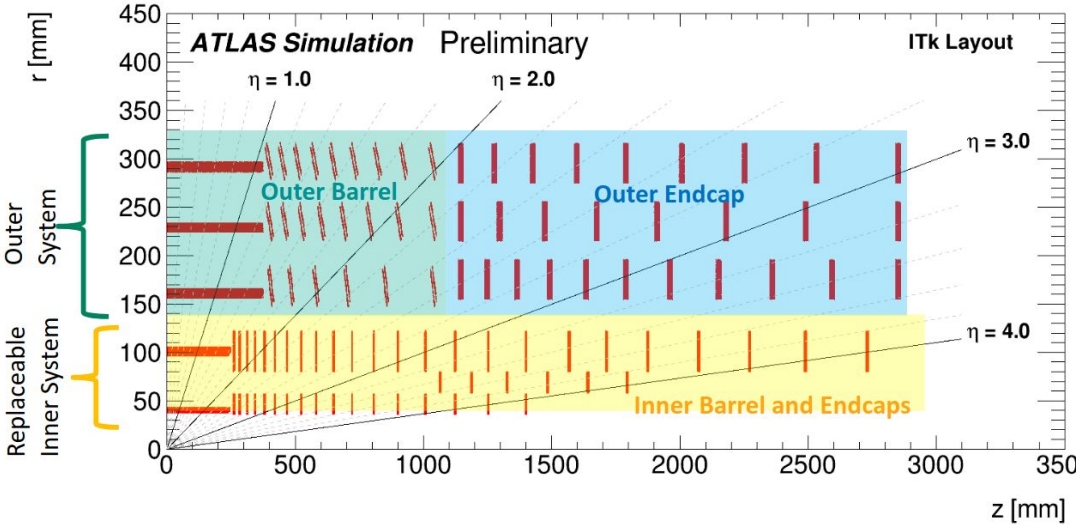
- A lot of work for many people to develop tools that could be used at different sites to perform calibration and QC of ITK pixel modules
  - Needed to guarantee uniformity in performance tested at different sites
- General philosophy and some procedures briefly described in this talk:
  - ADC calibration
  - Vcal calibration
  - SLDO VI scan
  - Injection capacitance
  - Analog readback

Backup

ITk pixel detector layout

Outer Barrel:
3 layers of flat staves and inclined rings
n-in-p planar quad modules
4472 quad modules, 7.2m^2

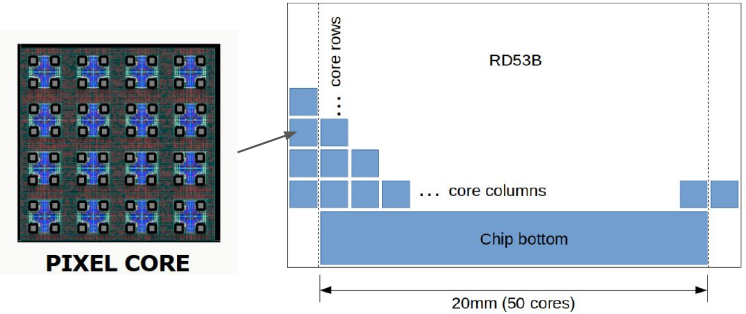
Forward pixels:
3 layers of rings
n-in-p planar quad modules
2344 quad modules, 3.75m^2

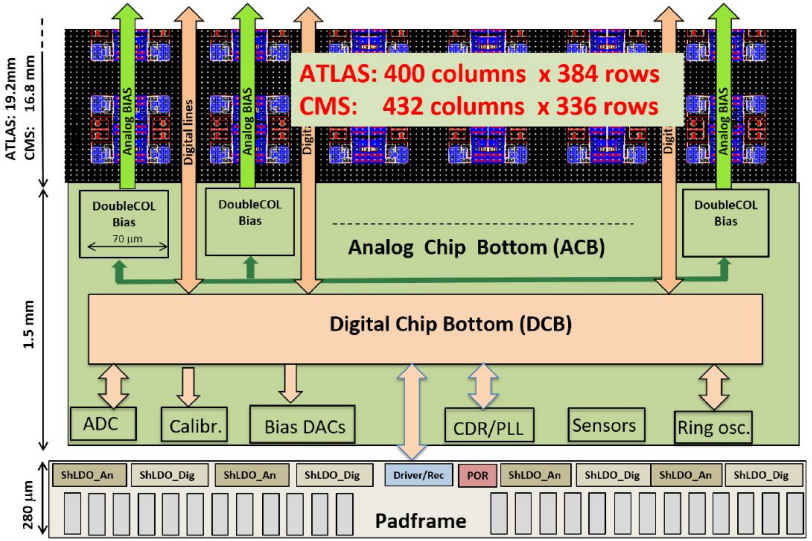


Inner System Replaceable:
2 layers of flat staves and rings
L0: 3D single modules, 1188 modules in 396 triplets, 0.5m^2
L1: n-in-p planar quad modules, 1160 modules, 2.0m^2

ITkPixV1: Floorplan

a pixel matrix and a chip bottom

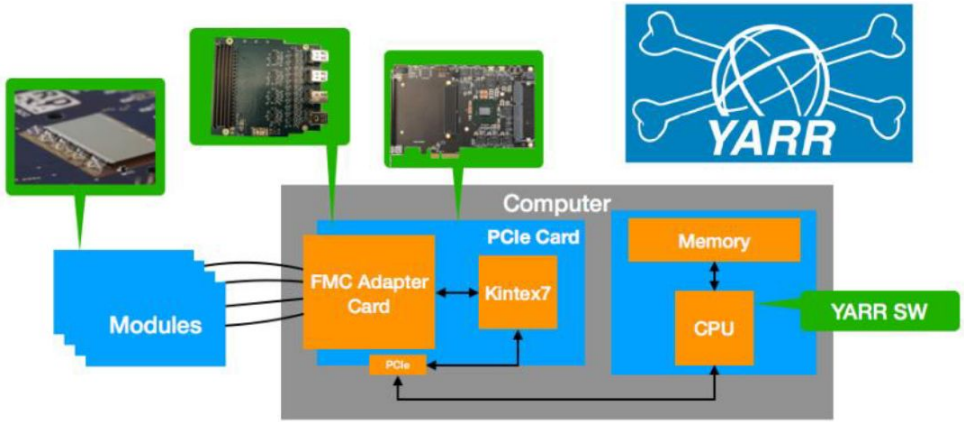




- Analog Chip Bottom (ACB): analog and mixed/signals building block for Calibration, Bias, Monitoring and Clock/Data recovery
- Digital Chip Bottom (DCB): synthesized digital logic
- Pad frame: I/O blocks with ESD protections, ShuntLDO for Serial Powering

Readout System YARR

- The Yet Another Rapid Readout (YARR) system is a data acquisition system designed for the pixel readout chips used in the Pixel Detector
- The module QC tool is based on the YARR
  - YARR FW - FPGA board
  - YARR SW - C++ based
- Communication with the module
  - Connectivity file
  - Controller file
- Configure the module
  - WriteRegister
    - Set vmux value
    - Set DAC value
    - Etc…



First test results from the ITkPixV1 pixel readout chip
T. Heim et al

VMUX / IMUX

15.5 IMUX and VMUX selection values

Setting	Selected Input	Setting	Selected Input	Setting	Selected Input
0	IREF main ref. current	11	Capmeasure parasitic	22	DIFF FE Preamp Top-Left
1	CDR VCO main bias	12	DIFF FE Preamp Main array	23	DIFF FE VTH1 Right
2	CDR VCO buffer bias	13	DIFF FE PreComp	24	DIFF FE Preamp Top
3	CDR CP current	14	DIFF FE Comparator	25	DIFF FE Preamp Top-Right
4	CDR FD current	15	DIFF FE VTH2	26	not used
5	CDR buffer bias	16	DIFF FE VTH1 Main array	27	not used
6	CML driver tap 2 bias	17	DIFF FE LCC	28	Ana. input current/21000
7	CML driver tap 1 bias	18	DIFF FE Feedback	29	Ana. shunt current/21600
8	CML driver main bias	19	DIFF FE Preamp Left	30	Dig. input current/21000
9	NTC_pad current	20	DIFF FE VTH1 Left	31	Dig. shunt current/21600
10	Capmeasure circuit	21	DIFF FE Preamp Right	32-62	not used
				63	high Z

Table 26: Current multiplexer (I_mux) assignments for ATLAS chip.

Setting	Selected Input	Setting	Selected Input	Setting	Selected Input
0	Vref_ADC (GADC)	10	DIFF FE VTH1 Main array	31	Vref_CORE
1	I_mux pad voltage	11	DIFF FE VTH1 Left	32	Vref_PRE
2	NTC_pad voltage	12	DIFF FE VTH1 Right	33	VINA / 4
3	VCAL_DAC / 2 (Sec. 6.3)	13	RADSENS Ana. SLDO	34	VDDA / 2
4	VDDA / 2 from capmeasure	14	TEMPSENS Ana. SLDO	35	VrefA
5	Poly TEMPSENS top	15	RADSENS Dig. SLDO	36	VOFS / 4
6	Poly TEMPSENS bottom	16	TEMPSENS Dig. SLDO	37	VIND / 4
7	VCAL_HI	17	RADSENS center	38	VDDD / 2
8	VCAL_MED	18	TEMPSENS center	39	VrefD
9	DIFF FE VTH2	19-30	Ana. GND	40-62	not used
				63	high Z

Table 27: Voltage multiplexer (V_mux) assignments for ATLAS chip.

VI SLDO specification details

type of module	I_{in}/FE chip [A]	VDDA,VDDD [V]	VinA,VInD [V]	Voffs [V]
L0/triplets	???	1.2 ± 0.01	$??? \pm 0.025$V	1.1 ± 0.01
L1	???	1.2 ± 0.01	$??? \pm 0.025$V	1 ± 0.01
L2-L4	1.526A	1.2 ± 0.01	$1.528\text{V} \pm 0.025\text{V}$	1 ± 0.01

Table 2: Nominal values for internal voltages

type of module	I_{in}/FE chip [A]	I_{in}A [A]	I_{in}D [A]	IRef [A]
L0/triplets	???	???A±???A	???A±???A	20 ± 0.3
L1	???	???A±???A	???A±???A	20 ± 0.3
L2-L4	1.526A	$0.654\text{A} \pm 0.058\text{A}$	$0.872\text{A} \pm 0.058\text{A}$	20 ± 0.3

Table 3: Nominal values for internal currents, with target minimum overhead during operation of 10%

type of module	I_{in}/FE chip [A]	IshuntA [A]	Overhead(A)	IshuntD [A]	Overhead(D)
L0/triplets	???	???A±???A	???	???A±???A	???
L1	???	???A±???A	???	???A±???A	???
L2-L4	1.526A	$0.114\text{A} \pm 0.058\text{A}$	10%	$0.190\text{A} \pm 0.067\text{A}$	18.7%

Table 4: chip shunt current and overhead while testing, with target minimum overhead during operation of 10%

type of module	Condition	Threshold
L0/triplets		I_{in}^{min} <???
L0/triplets	for $I_{in} > I_{in}^{min}$	$\lvert V(I_{in}) - V_{theory}(I_{in})\rvert$ <???
L1		I_{min} <???
L1	for $I_{in} > I_{in}^{min}$	$\lvert V(I_{in}) - V_{theory}(I_{in})\rvert$ <???
L2-L4		$I_{in}^{min} < 5.1\text{A}$
L2-L4	for $I_{in} > I_{in}^{min}$	$\lvert V(I_{in}) - V_{theory}(I_{in})\rvert < 0.03V$

Table 5: Requirements for SLDO