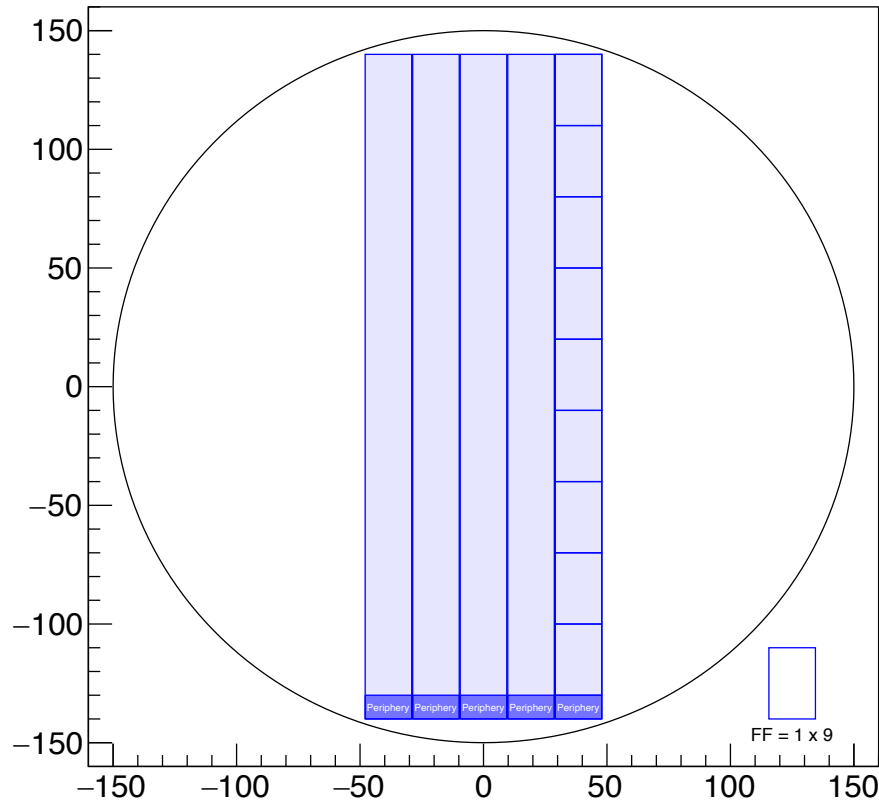


ePIC Silicon Disks

- Sensor requirements
 - Requires smaller format sensors for improved yield and tiling flexibility
 - Multiple sensor formats needed – changes to stitching plan & periphery
 - Studying optimum tiling geometry
 - Location of periphery informs design of cooling circuit
 - Layout informs material budget (e.g. sensor overlaps)
 - Both aspects needed for detailed mechanical design
 - Study will also inform cost of silicon
 - Assume 5 disks in +z and -z
 - See Ernst Sichtermann: <https://indico.bnl.gov/event/16261/> from 23 June
 - Take care of the offset between the centre of the beam pipe from the nominal beam line away from the IP
 - Not a completely trivial problem, so write some code to make study easier and to explore different options
 - This is not the final word but a starting point for further discussion

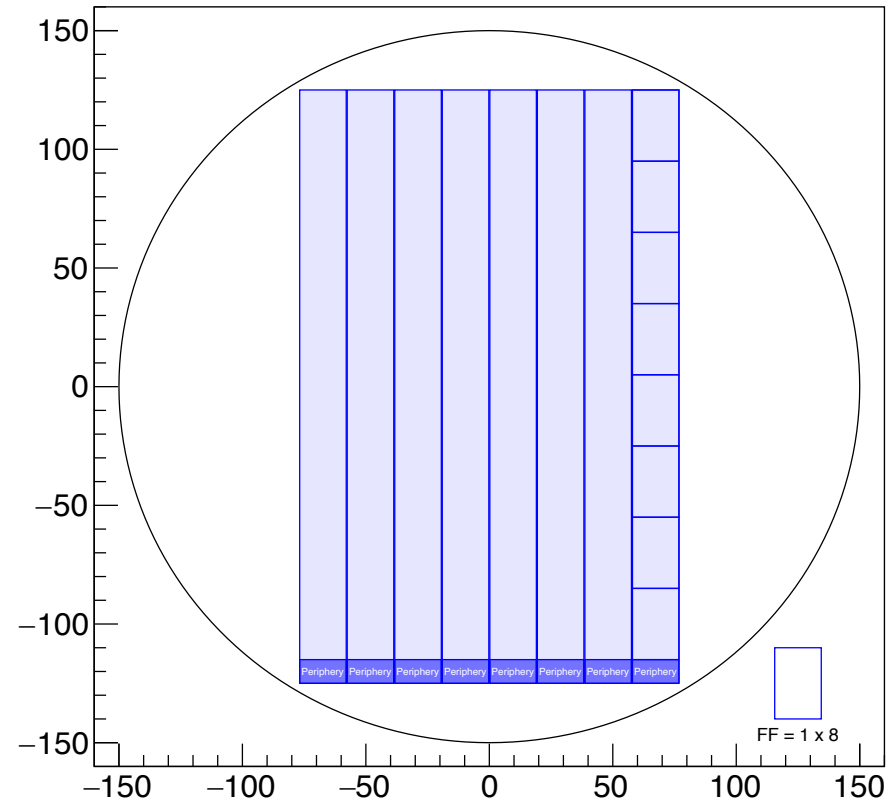
EIC LAS – Wafer Usage

EIC-LAS



Max 5 (1 x 9) sensors per wafer
45 reticles

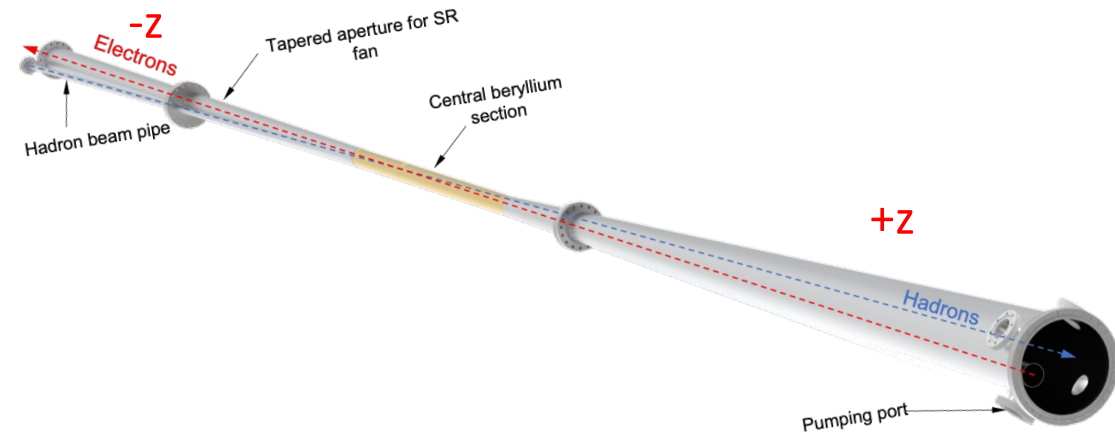
EIC-LAS



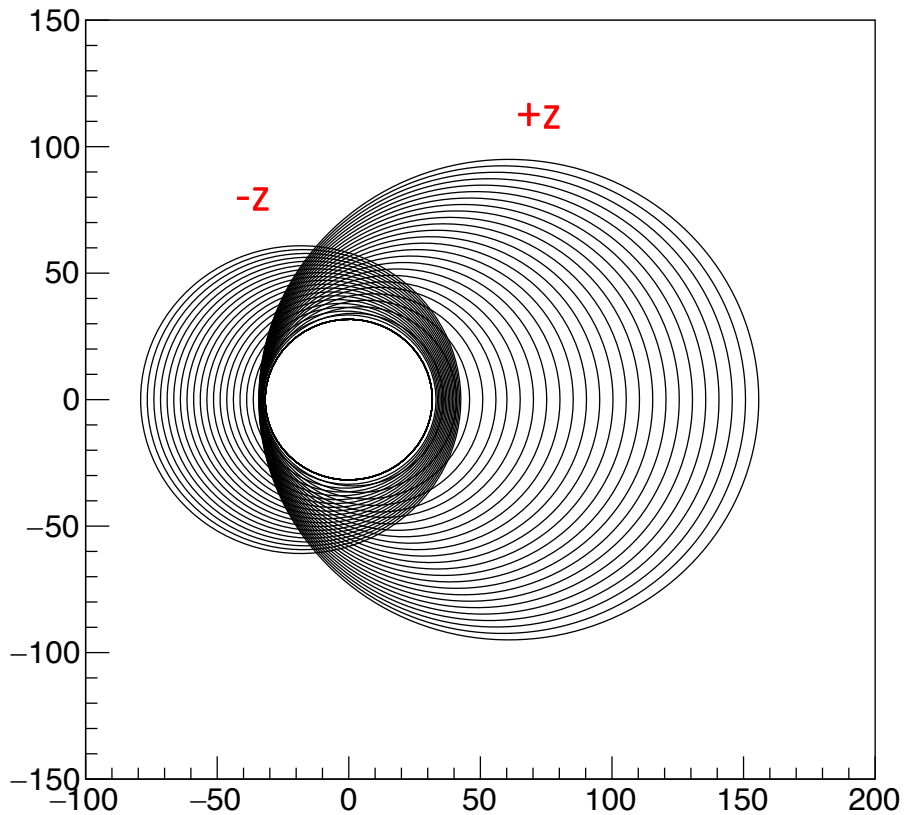
Max 8 (1 x 8) sensors per wafer
64 reticles

How many sensors of each type are needed?

Beam pipe model



EIC Beampipe



Beampipe profile; 100 mm steps

Model output

The beam pipe radius has been modelled as a function of z from the original CAD drawings

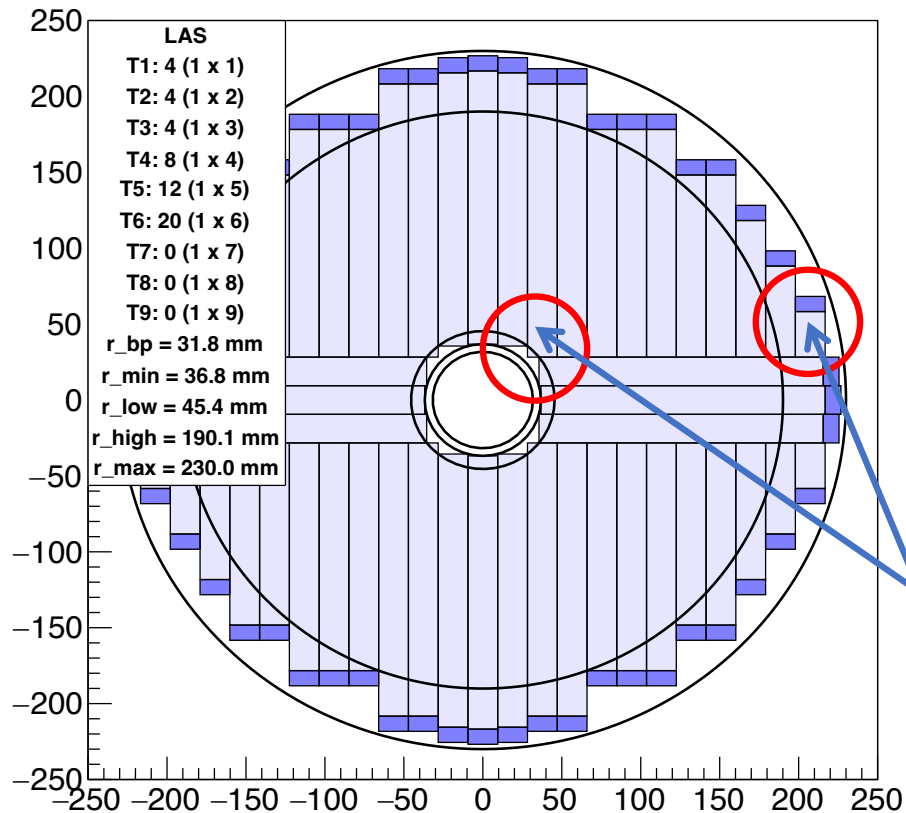
	Z - ePIC	R_bpip	x_offset	R_inner	R_outer
5n	-1350	41.08	-5.30	46.1	430
4n	-1000	35.76	-1.81	40.8	430
3n	-700	31.76	0.00	36.8	430
2n	-450	31.76	0.00	36.8	430
1n	-250	31.76	0.00	36.8	230
1p	250	31.76	0.00	36.8	230
2p	450	31.76	0.00	36.8	430
3p	700	32.86	0.56	37.9	430
4p	1000	40.58	7.85	45.6	430
5p	1350	49.12	16.02	54.2	430

Dimensions are mm

Disk tiling algorithm

EIC-SVT Disk-1 Tile

The algorithm



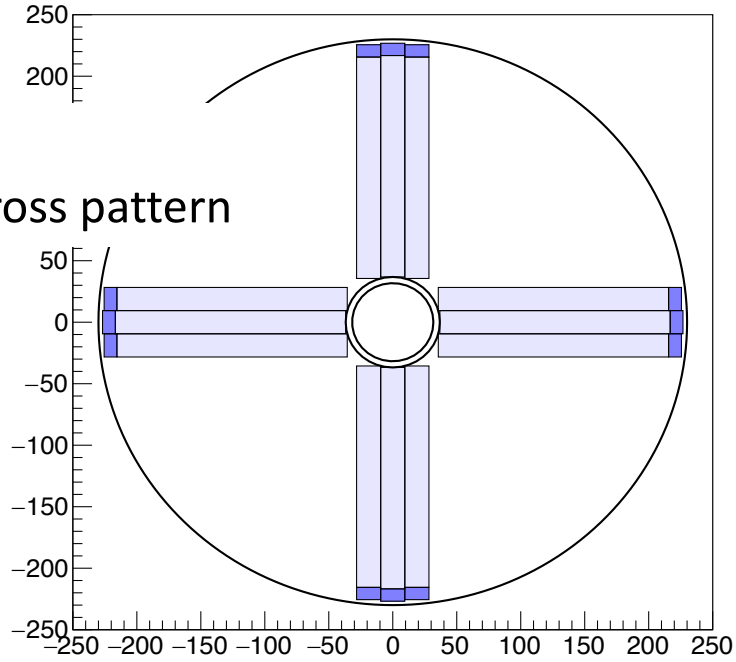
$z = +/- 250$ mm

Central cross = 3 sensors

- Try to keep periphery to larger radii
- Two designs, each based on a central cross pattern smaller than the inner diameter of the disk
- Design #1 = vertical tiles (shown)
- Design #2 = herringbone pattern (alternating vertical and horizontal tiles)
- The minimum disk radius (r_{min}) is 5 mm larger than the beam pipe radius (r_{bp}) for bake out
- Sensor and periphery must be contained within the min and max radii of the disk (r_{min} and r_{max}).
- For each disk, the algorithm calculates the smallest and largest radii with full acceptance (r_{low} and r_{high})
- The algorithm does not permit any sensor overlap
- Acceptance at small radii could be improved by allowing some sensor overlap; placing overlapping sensors on the reverse side of the disk (in progress)
- Limits on the max and min sensor length can be applied
- Study the number of sensor variants that are needed

EIC-SVT Disk-1 Tile

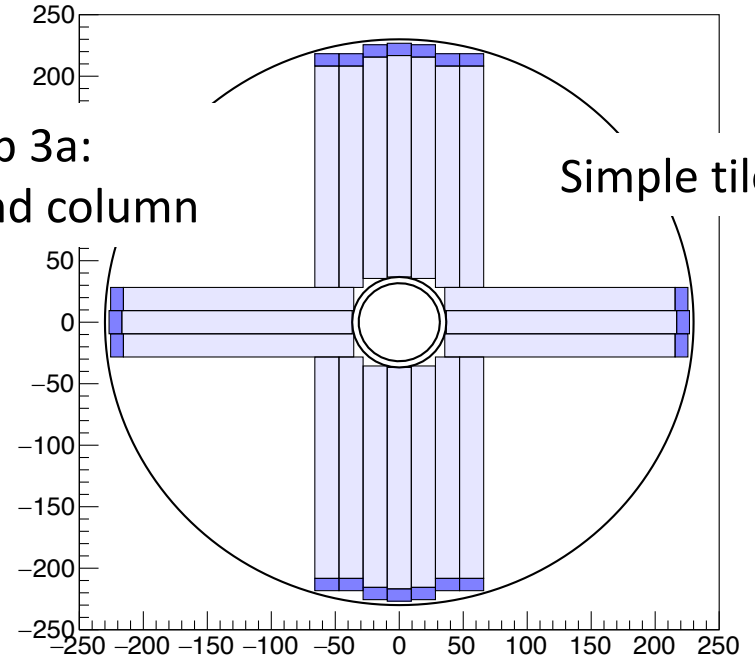
Step 1:
Draw cross pattern



EIC-SVT Disk-1 Tile

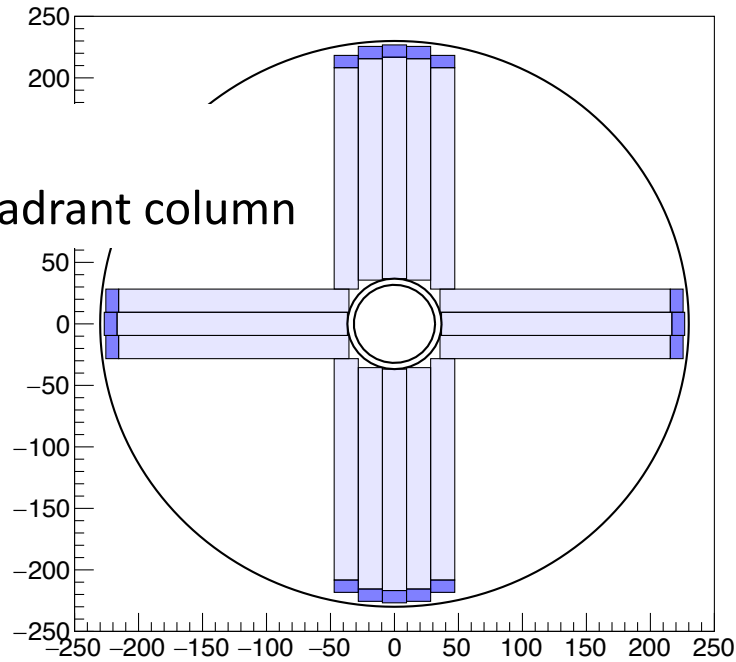
EITHER Step 3a:
Draw second column

Simple tile



EIC-SVT Disk-1 Tile

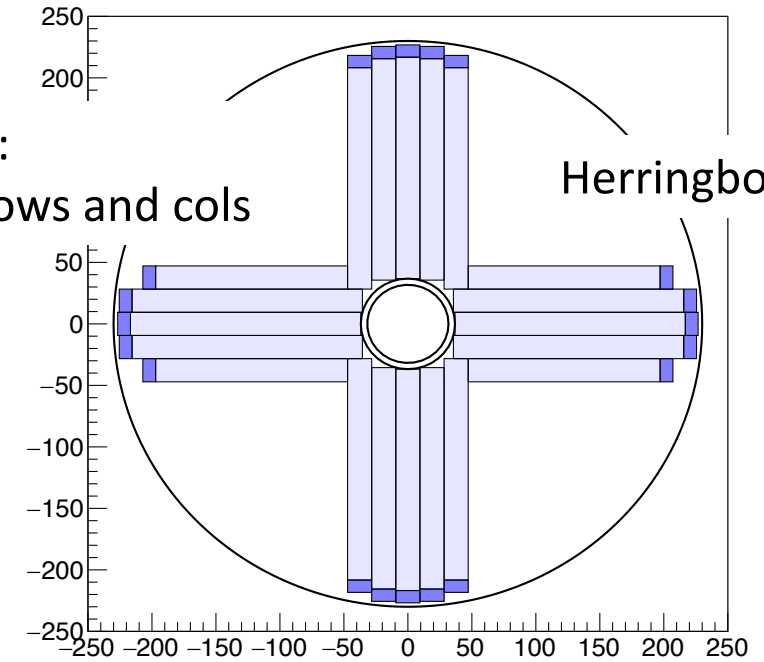
Step 2:
First quadrant column



EIC-SVT Disk-1 Tile

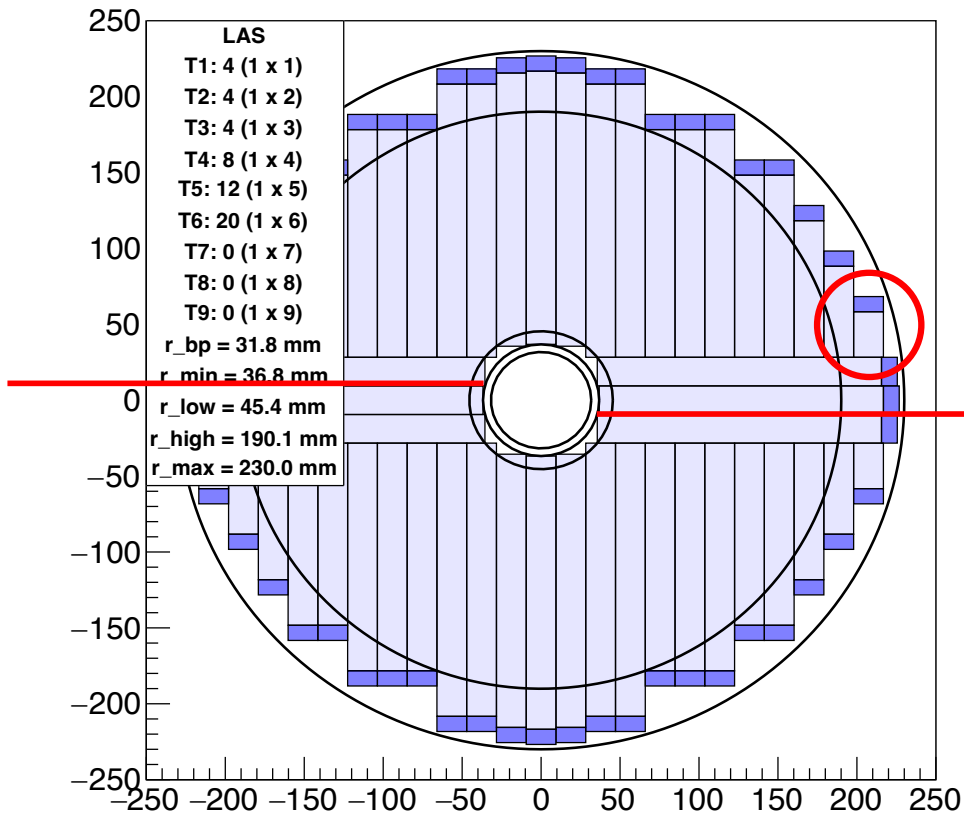
OR Step 3b:
Alternate rows and cols

Herringbone



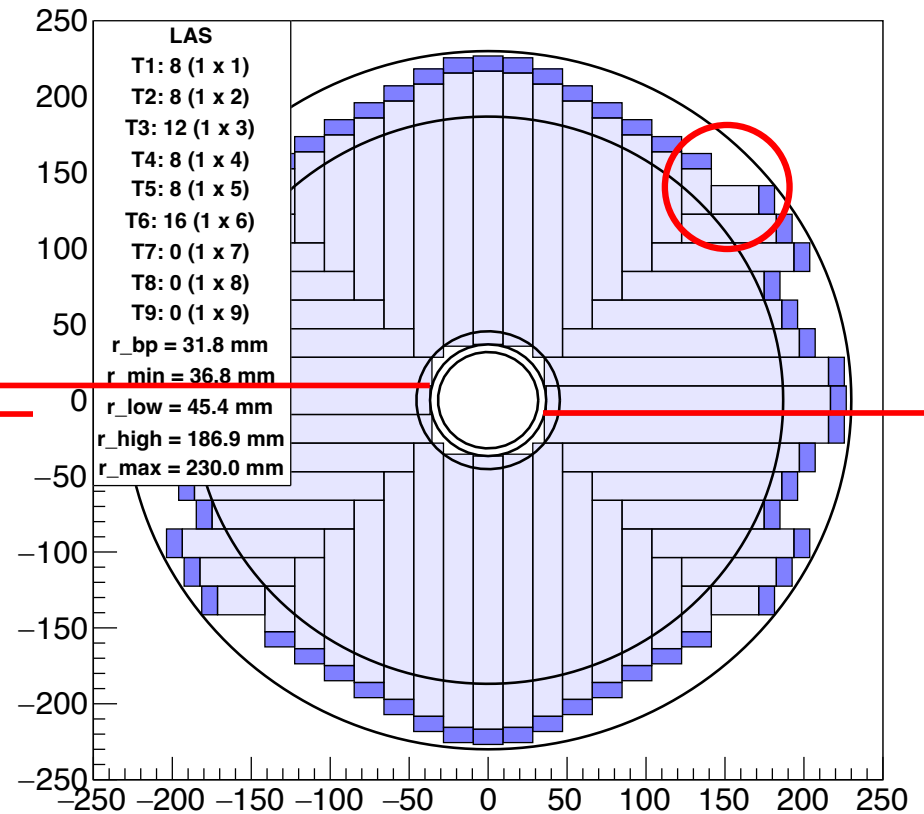
Disk 1

EIC-SVT Disk-1 Tile



52 sensors
236 reticles

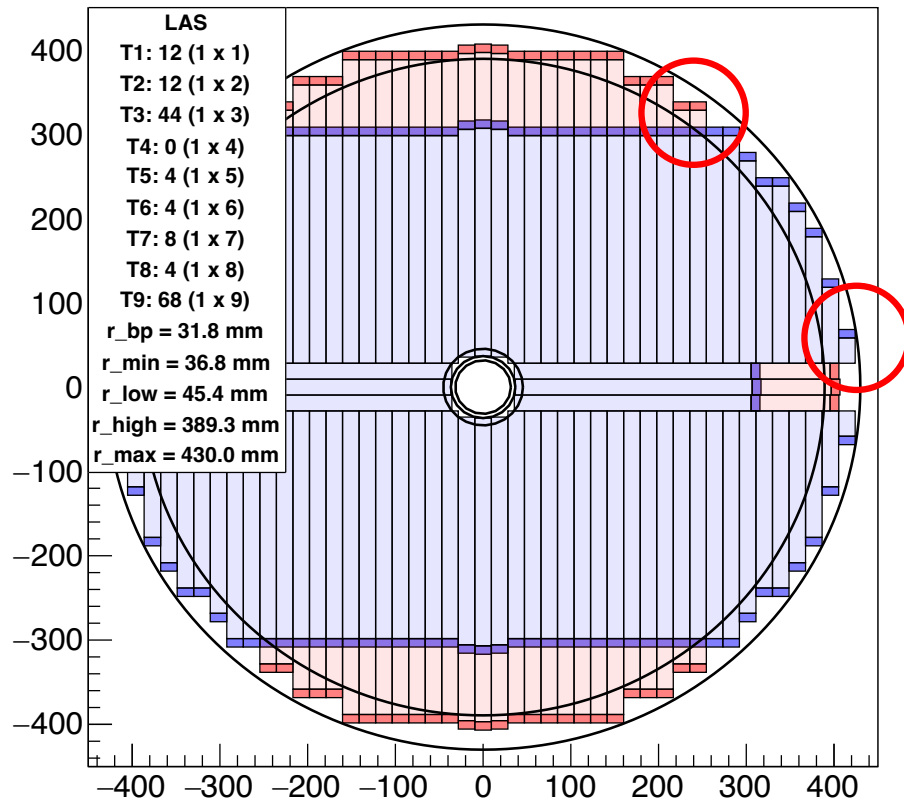
EIC-SVT Disk-1 Tile



60 sensors
228 reticles

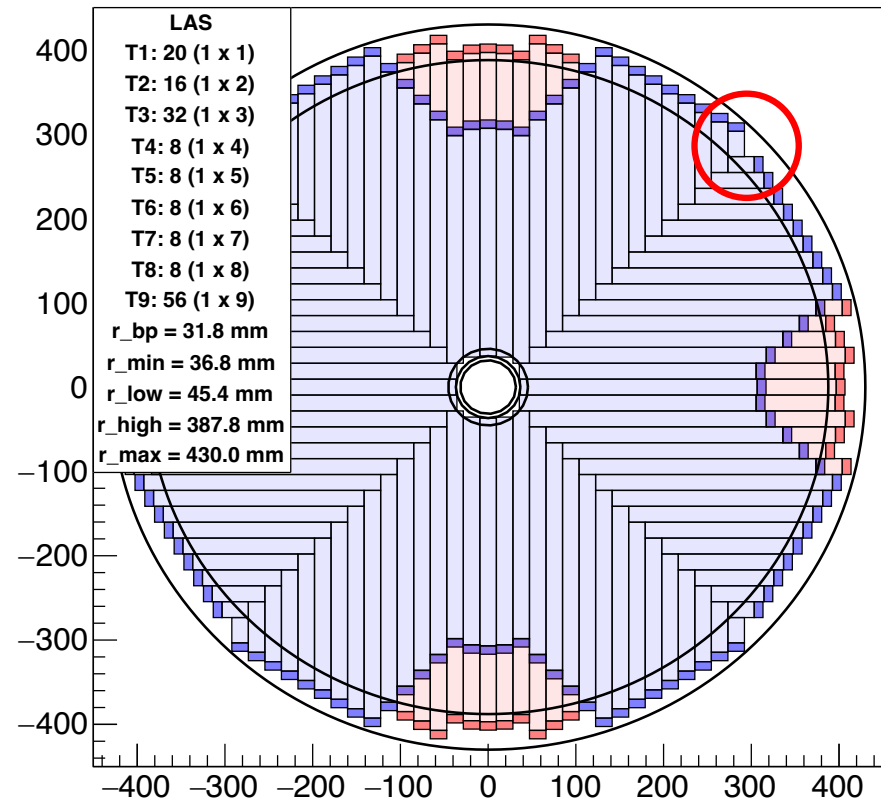
Disk 2/3n

EIC-SVT Disk-2/3n Tile



156 sensors
912 reticles

EIC-SVT Disk-2/3n Tile

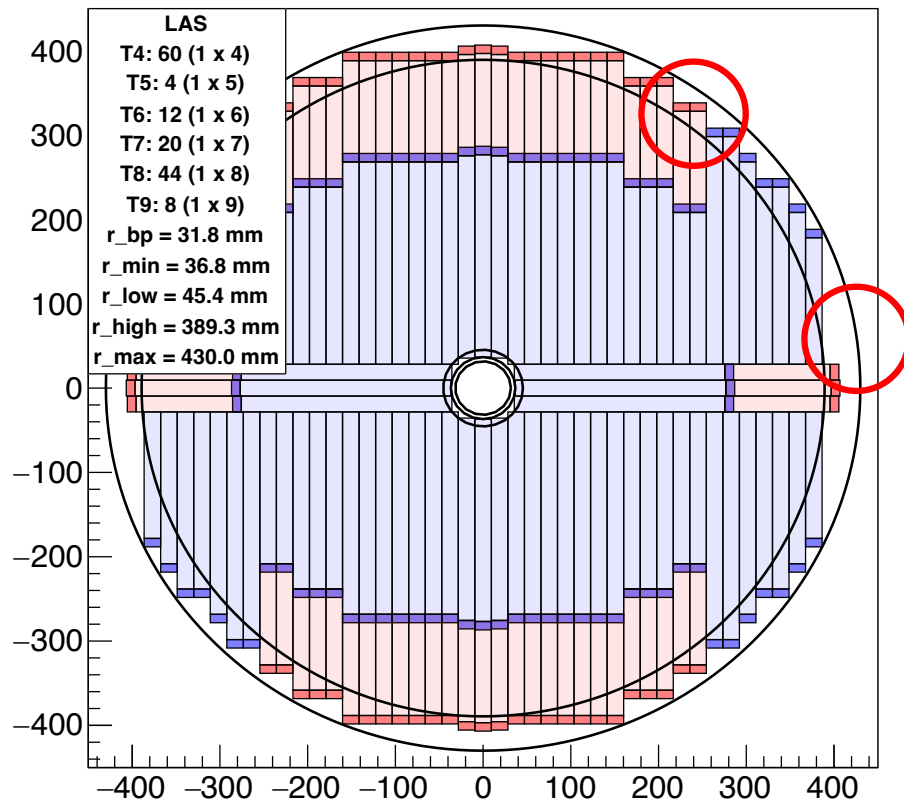


164 sensors
892 reticles

Note: Sensors in red on reverse side of disk
overlap digital periphery of inner sensors in blue

Disk 2/3n – restricting sensor size

EIC-SVT Disk-2/3n Tile

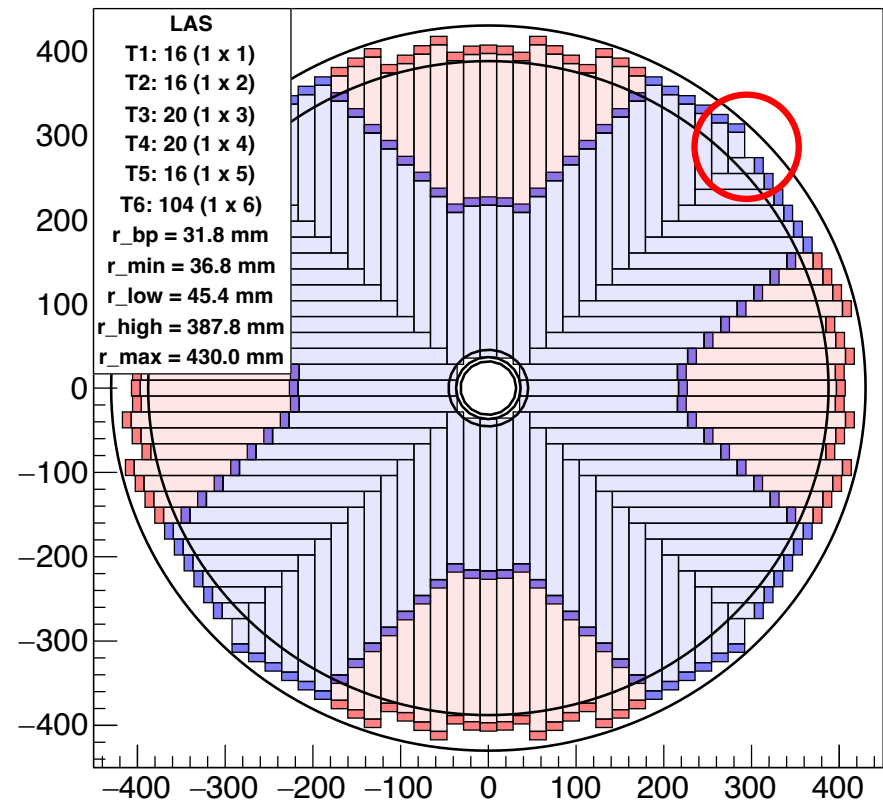


148 sensors

896 reticles

Fewer, longer sensors T4 – T9

EIC-SVT Disk-2/3n Tile

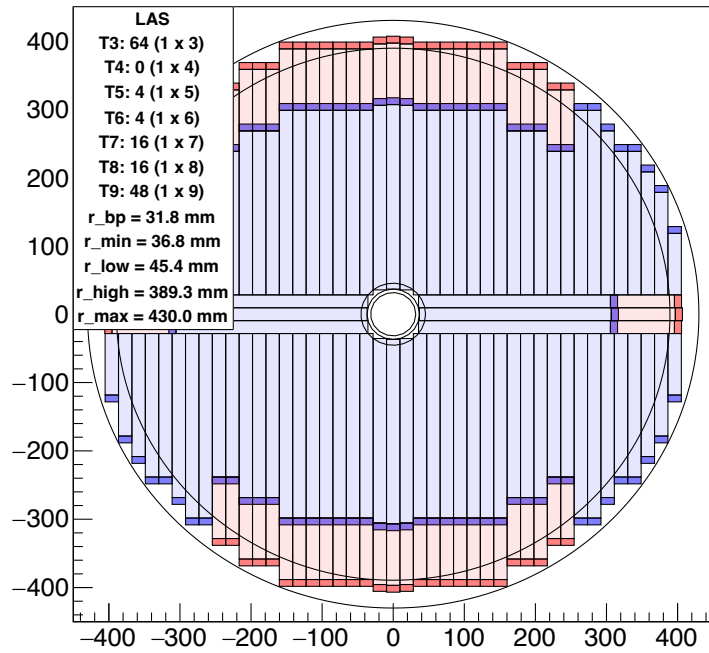


192 sensors

892 reticles

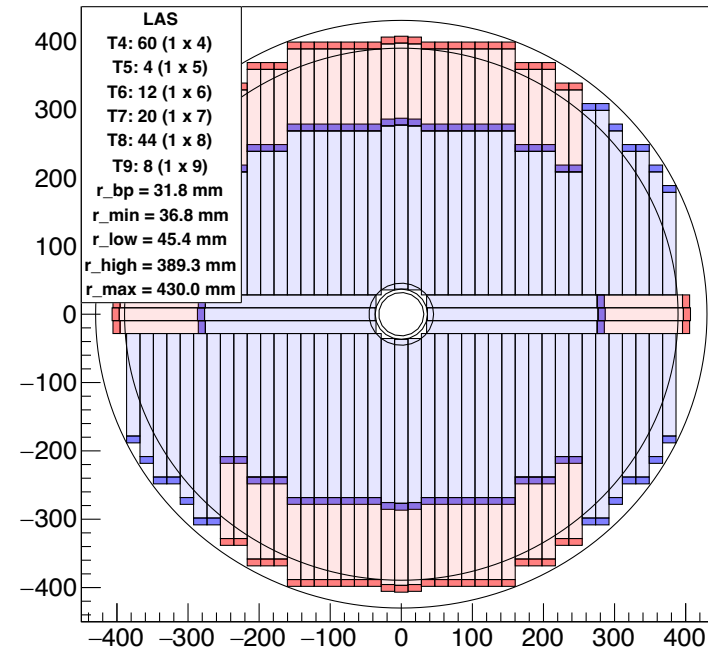
More, shorter sensors T1 – T6

EIC-SVT Disk-2/3n Tile



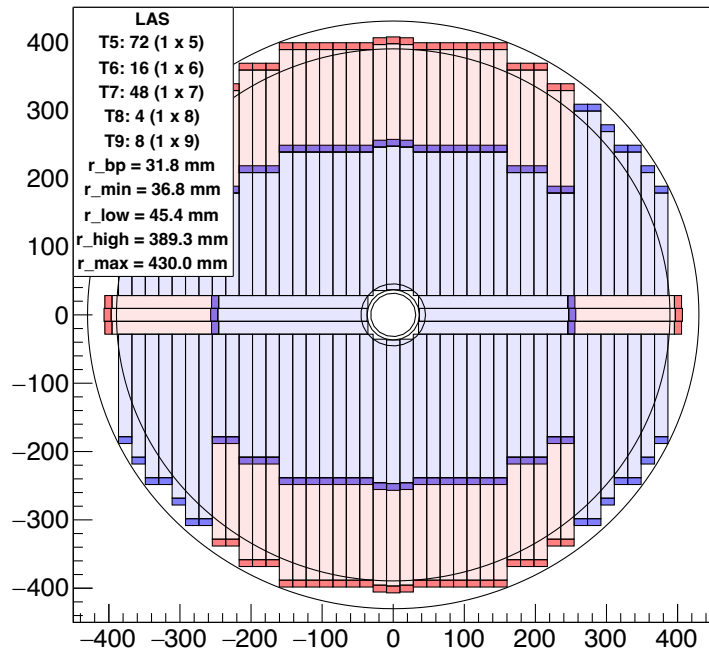
T3 – T9

EIC-SVT Disk-2/3n Tile



T4 – T9

EIC-SVT Disk-2/3n Tile



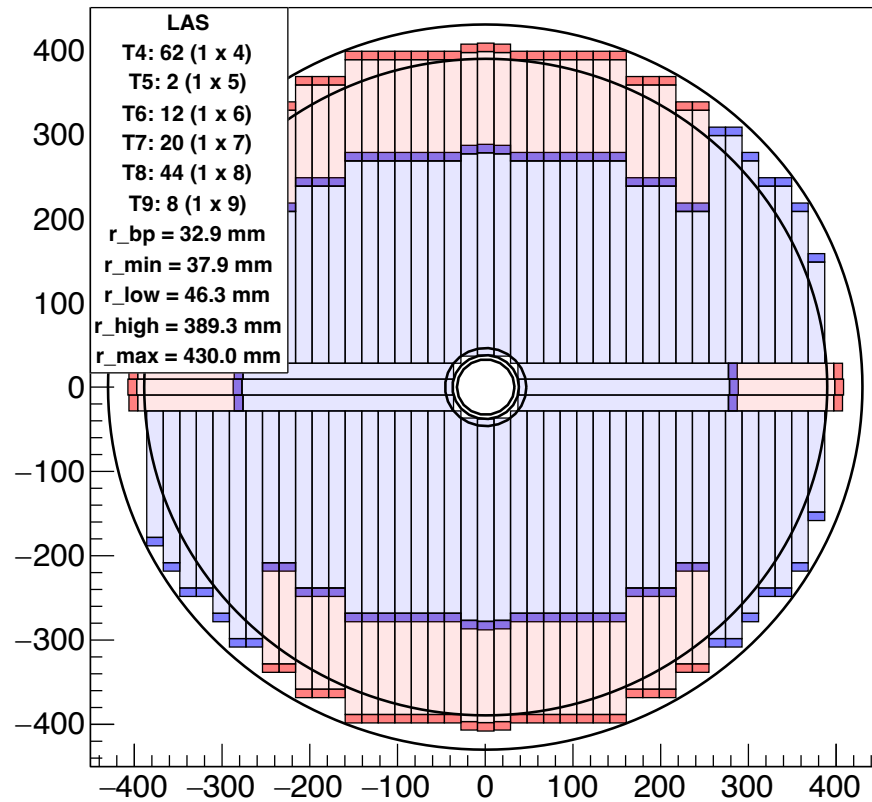
T5 – T9

Greater prospect of reducing number of sensor types with the simple tiling design

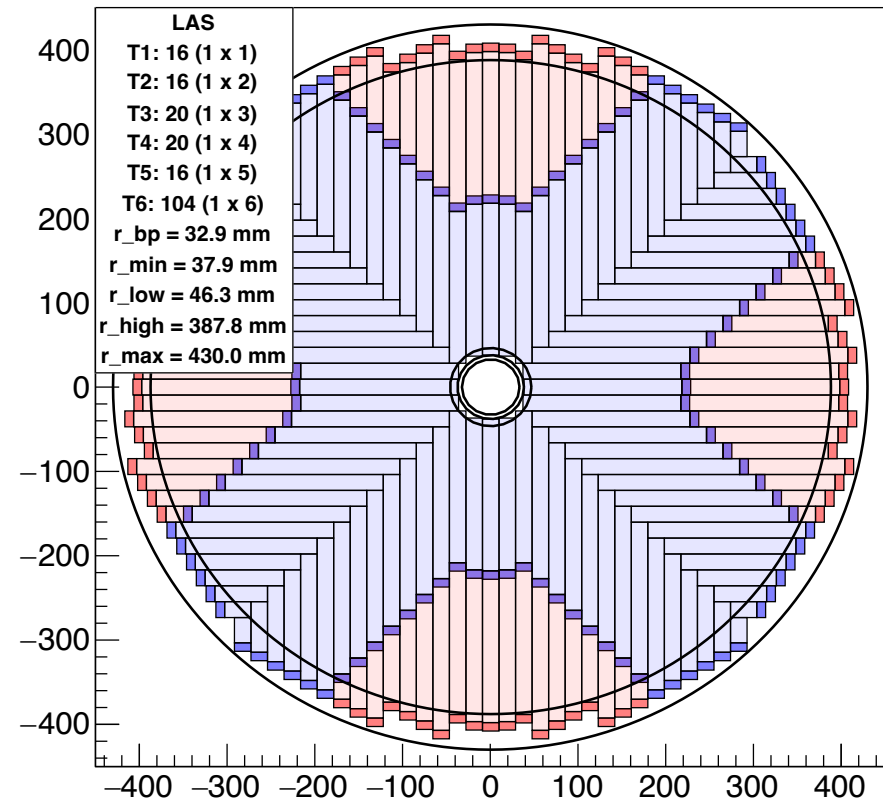
However, the reduction in sensor types pushes periphery inwards, adding material due to flex cables running over the outer sensors at larger radii

Disk 3p – restricting sensor size

EIC-SVT Disk-3p Tile

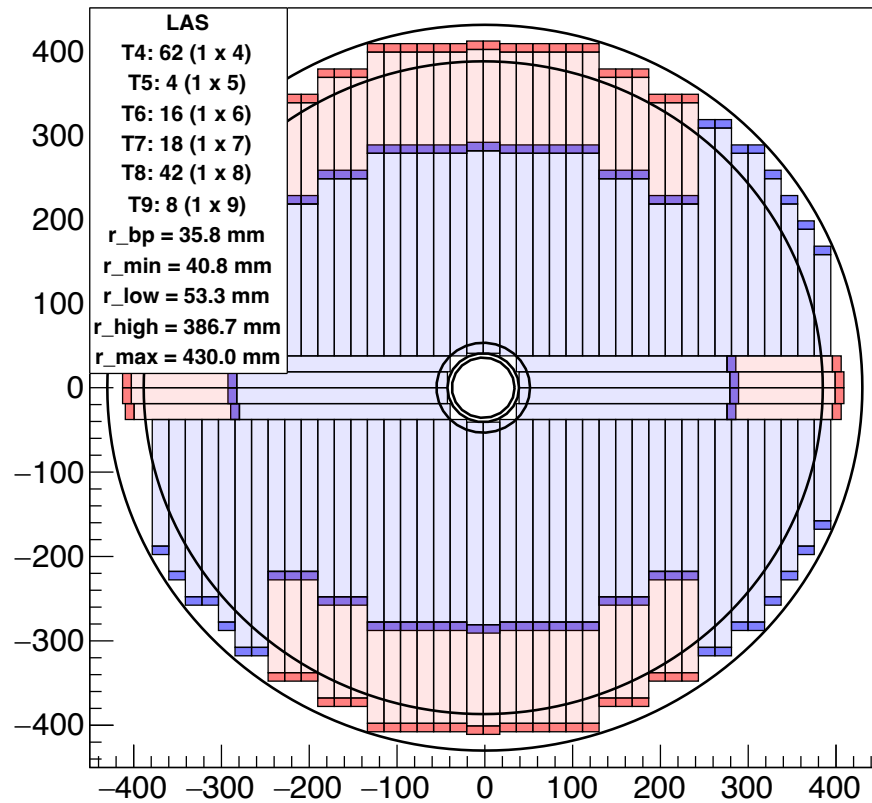


EIC-SVT Disk-3p Tile

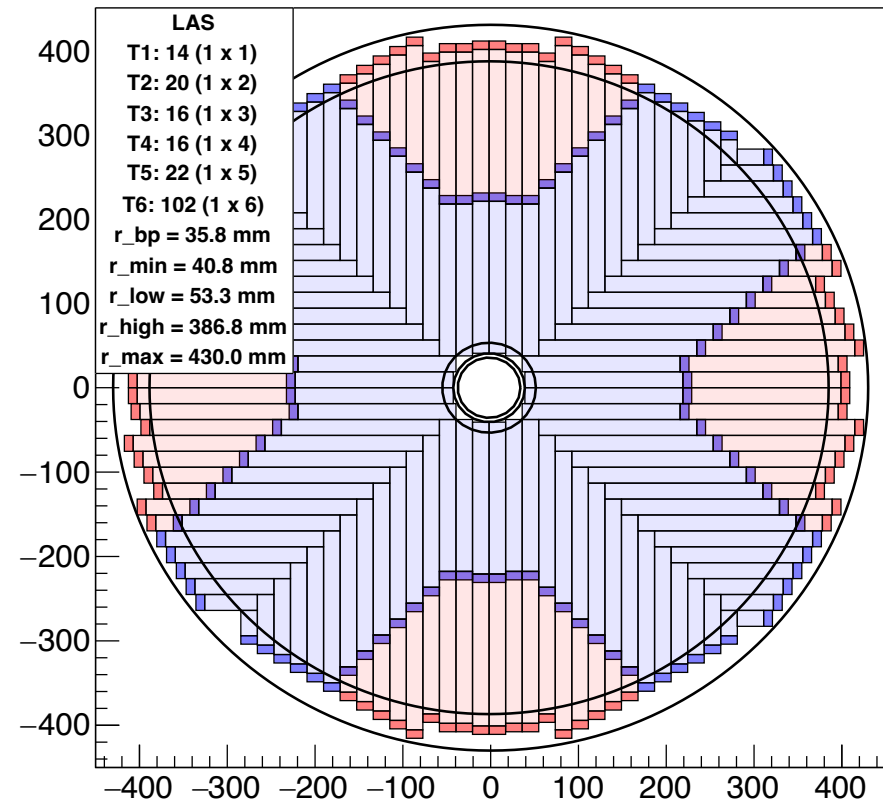


Disk 4n – restricting sensor size

EIC-SVT Disk-4n Tile

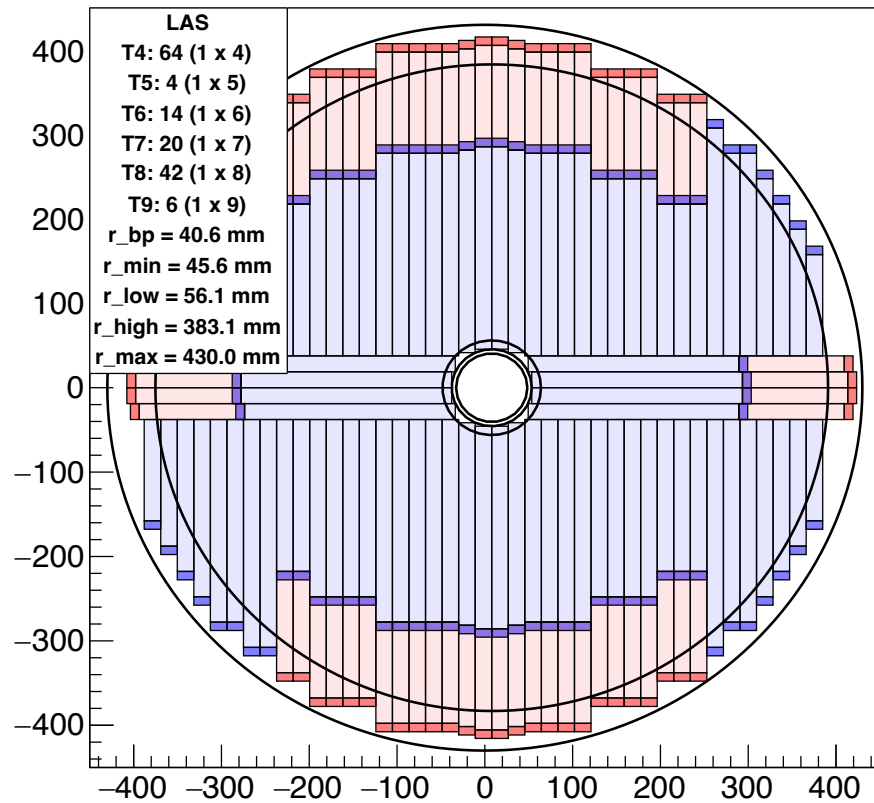


EIC-SVT Disk-4n Tile

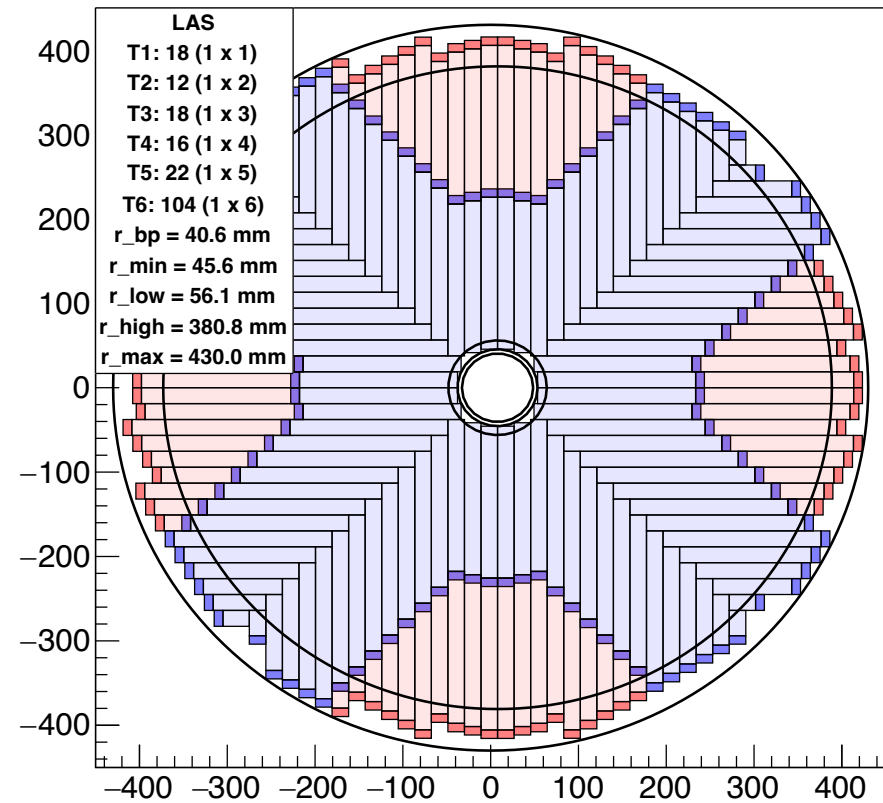


Disk 4p – restricting sensor size

EIC-SVT Disk-4p Tile

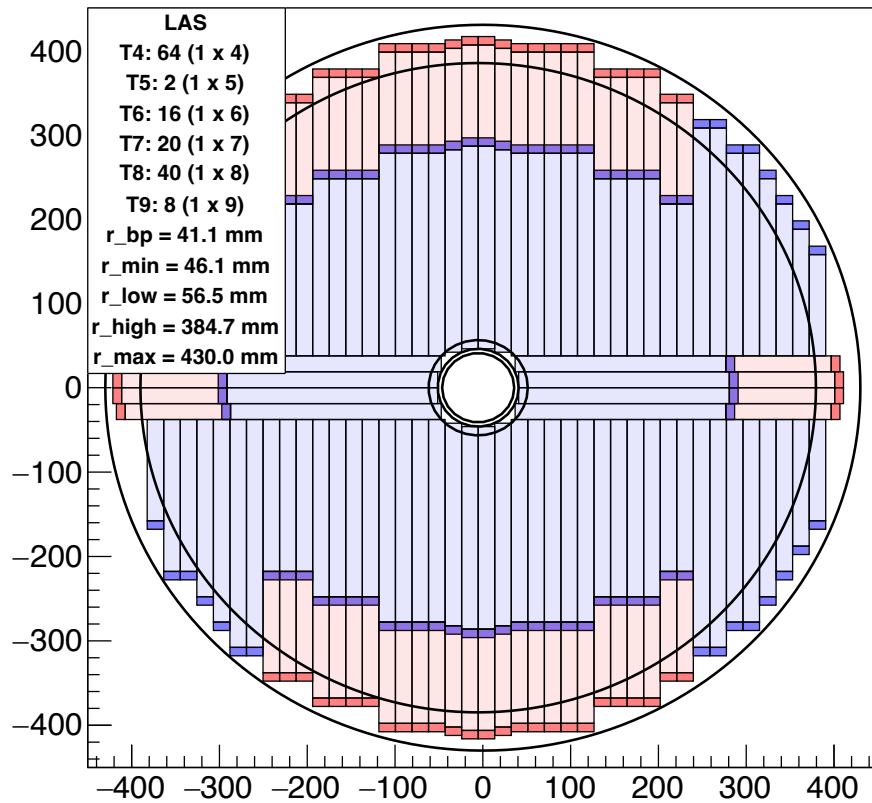


EIC-SVT Disk-4p Tile

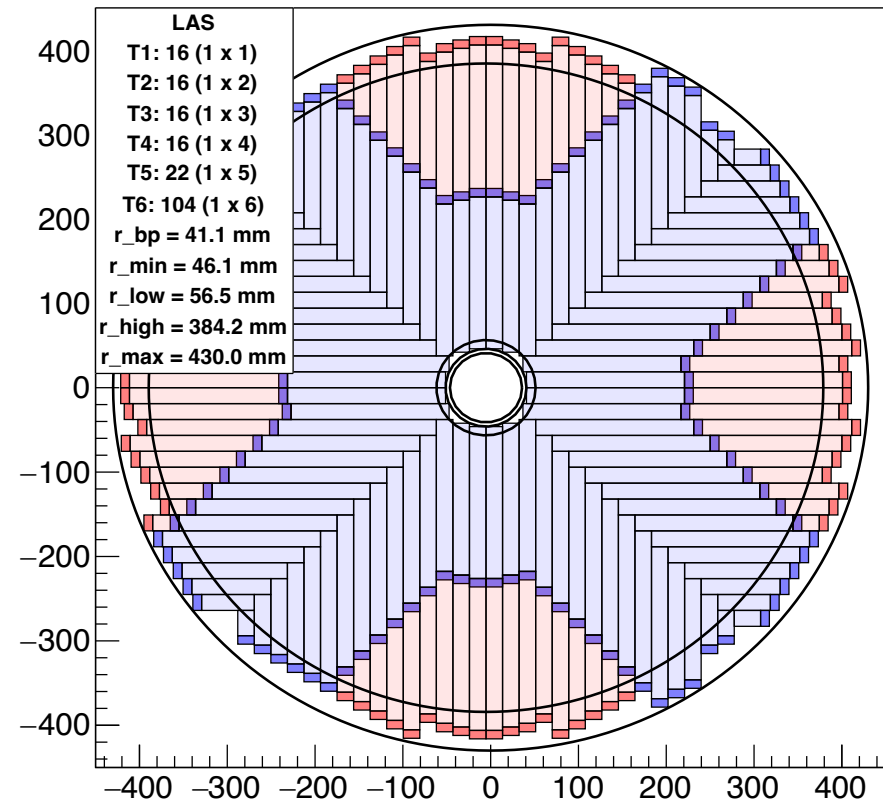


Disk 5n – restricting sensor size

EIC-SVT Disk-5n Tile

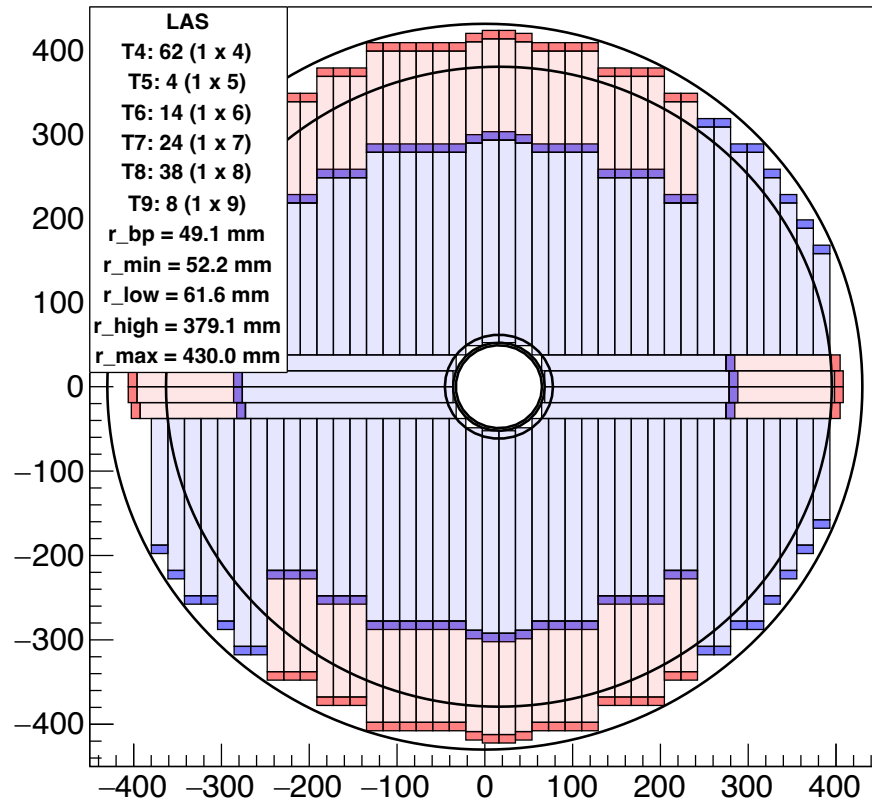


EIC-SVT Disk-5n Tile

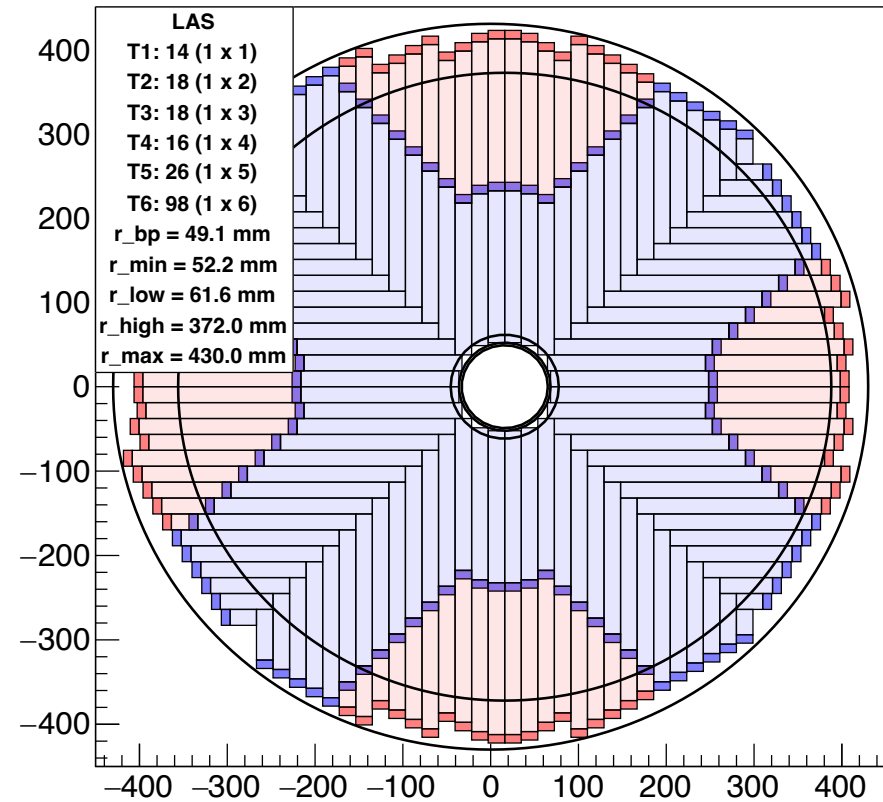


Disk 5p – restricting sensor size

EIC-SVT Disk-5p Tile



EIC-SVT Disk-5p Tile



Conclusions

- EIC Disks
 - Multiple sensor formats needed – requiring changes to stitching plan & organisation of the digital periphery
 - Attempt to minimise the number of formats by restricting the maximum and/or minimum sensor length
 - How hard do we need to work to improve acceptance at small radii?
 - Compare acceptance (e.g. hits per track) with complete azimuthal acceptance (between r_{low} and r_{high}) with physical disk dimensions (r_{min} and r_{max})
 - Simple tiling (most sensors lying in the same direction) requires fewer sensors and gives slightly better coverage
 - Simple tiling enables the smaller sensor variants to be eliminated and reduces the number of the longest variant. This potentially results in more efficient silicon wafer usage.