EICROC

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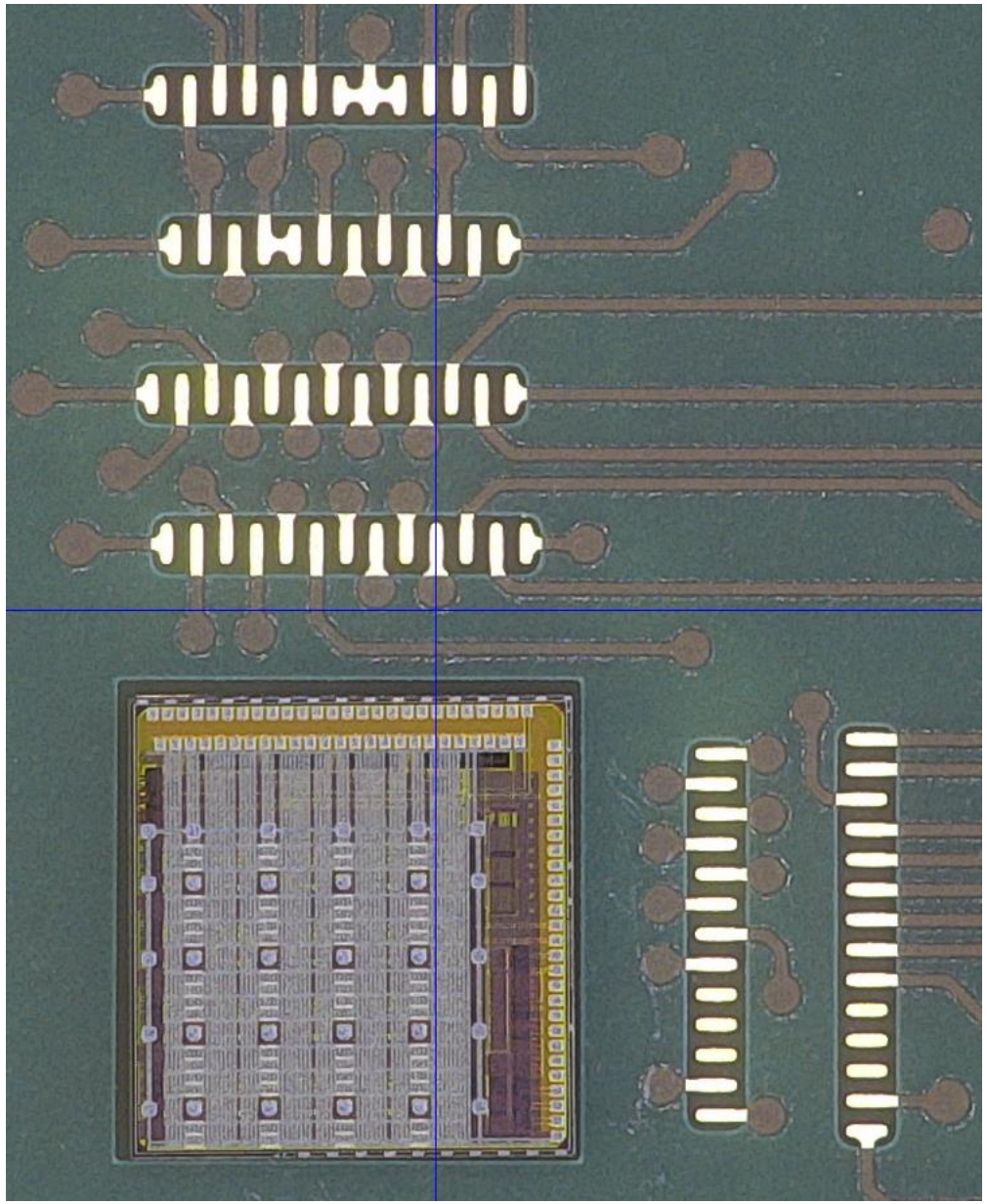
Organization for Micro-Electronics desiGn and Applications

FY22 report: EICROC0 design and fabrication

- EICROC0 is a 16-channel testchip for AC-LGADs at EIC
  - Based on ALTIROC (ATLAS HGTD) front-end and HGCROC (CMS HGCAL) ADC/TDC
  - Reads 500x500 um pixels for sensor evaluation
  - Readout designed for testbeam (not EIC)
  - Fabricated in march 2022, received beg july 2022
  - now at bonding at BNL



EICROC power consumption

Am I correct in understanding the power consumption of the EICROC to be 1-2 mW/ch (e.g. pixel), or is it something different from this? Regardless of the correct answer, what does this power consumption reference – the power consumption of the device simply being turned on, or expected power dissipation during full operation with expected occupancies?

- The *target* power consumption is indeed 1-2 mW/ch. This will not increase a lot (~10%) during operation. Most of the components dissipate regardless of the rate (discriminator, preamp, digital part…). If the ADC is gated (which is the goal), it should not increase the power consumption significantly.

EICROC form factor

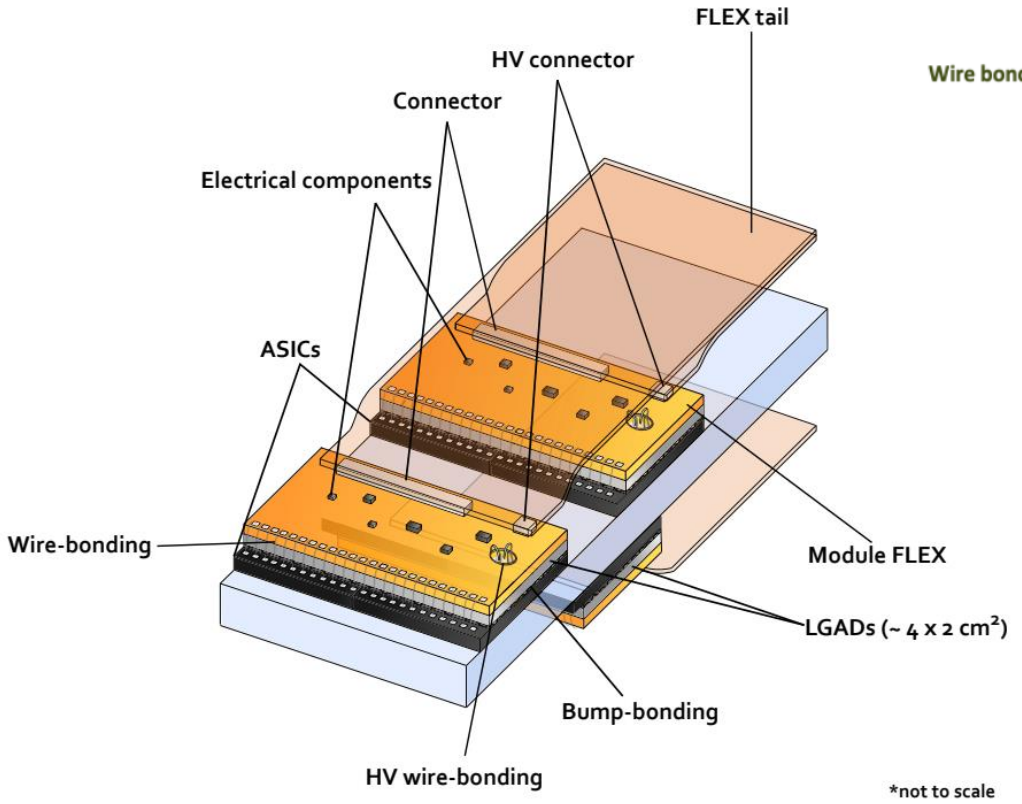
Is it possible to adjust the form-factor of the ASIC, or is this fixed? Currently, we assume a roughly 3.2 x 3.2cm package for a single sensor with 4 ASICs bonded to the back. This is normally fine, but we were wondering if there is a possibility to bond a half-sized sensor to two ASICs (like a rectangular layout with 1.6cm by 3.2cm), or to even do a single sensor + ASIC.

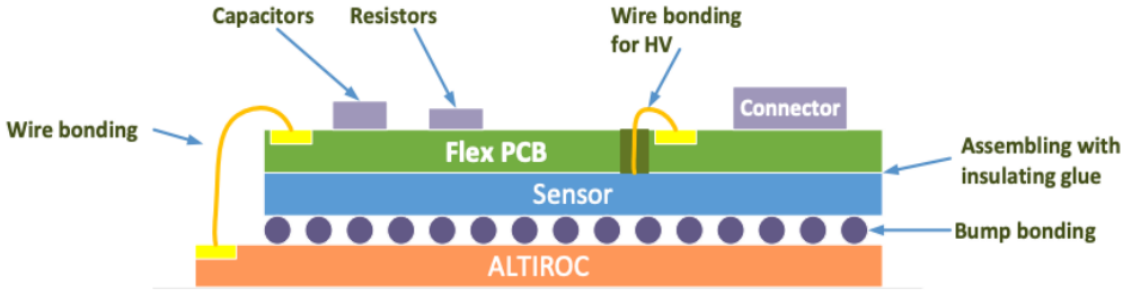
- The form factor is open, but the ASIC size cannot exceed the reticle size (24x32 mm). After that, all is possible, taking into account that one side of the chip is used for "end of column" balcony and bonding pads.

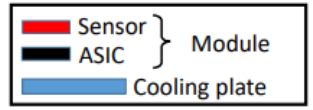
- Larger dimensions imply potential issues due to voltage drops and power distributions, so final size should be decided soon and tested.

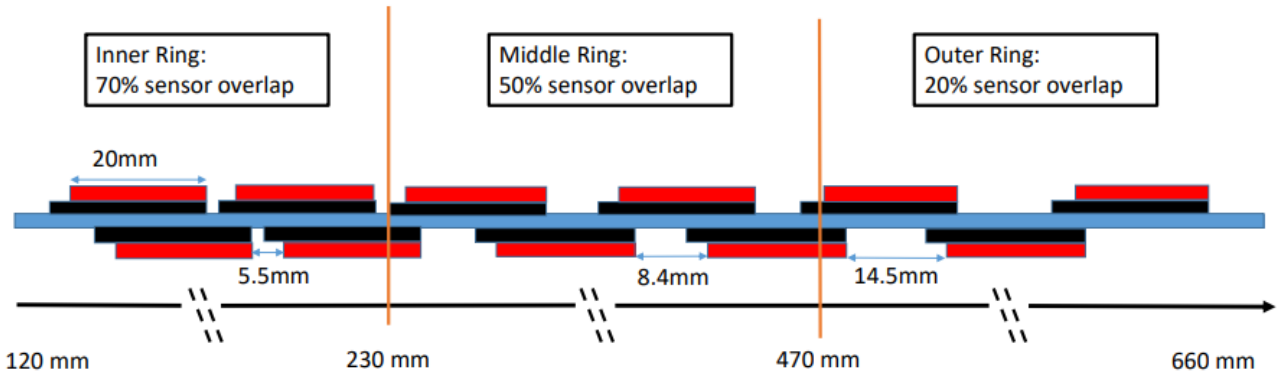
EICROC readout and cooling

We are wondering if you guy had any idea as to how the ASIC readout might look when the full system is implemented. Since the ASICs are bonded to the back of the sensor, this implies that we'd need to run power + readout cabling all the way to the inner-part of the detector. Is this the case? If so, do you guys have any idea what this might look like (e.g. thin ribbon cables, or heavier lines)?

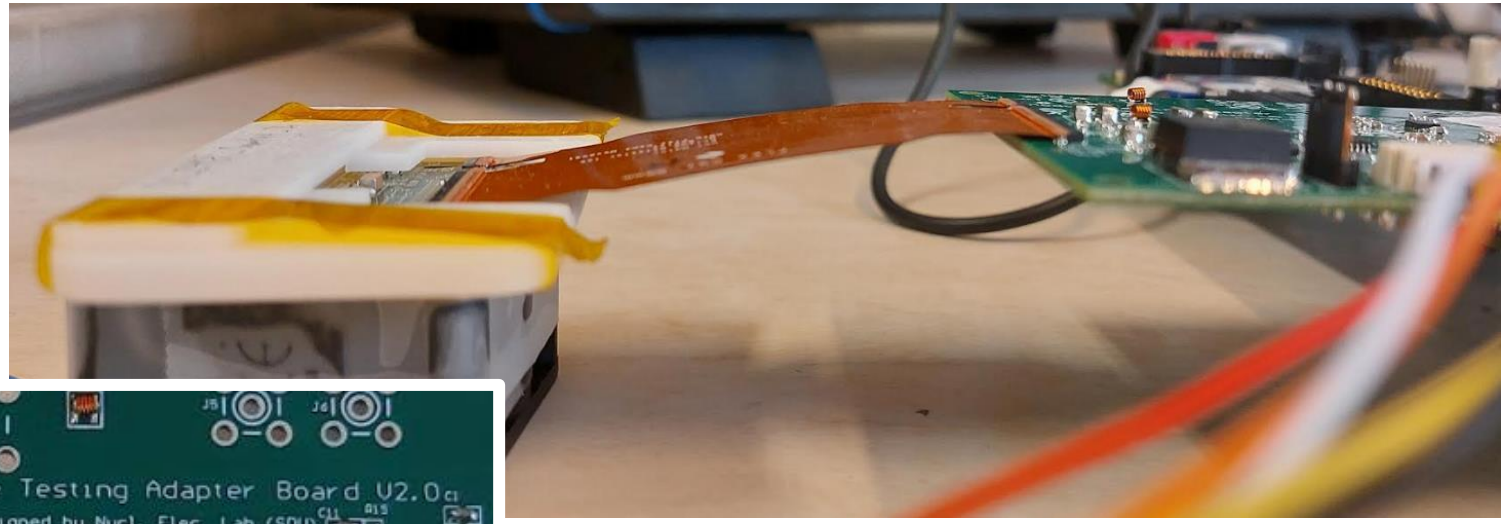


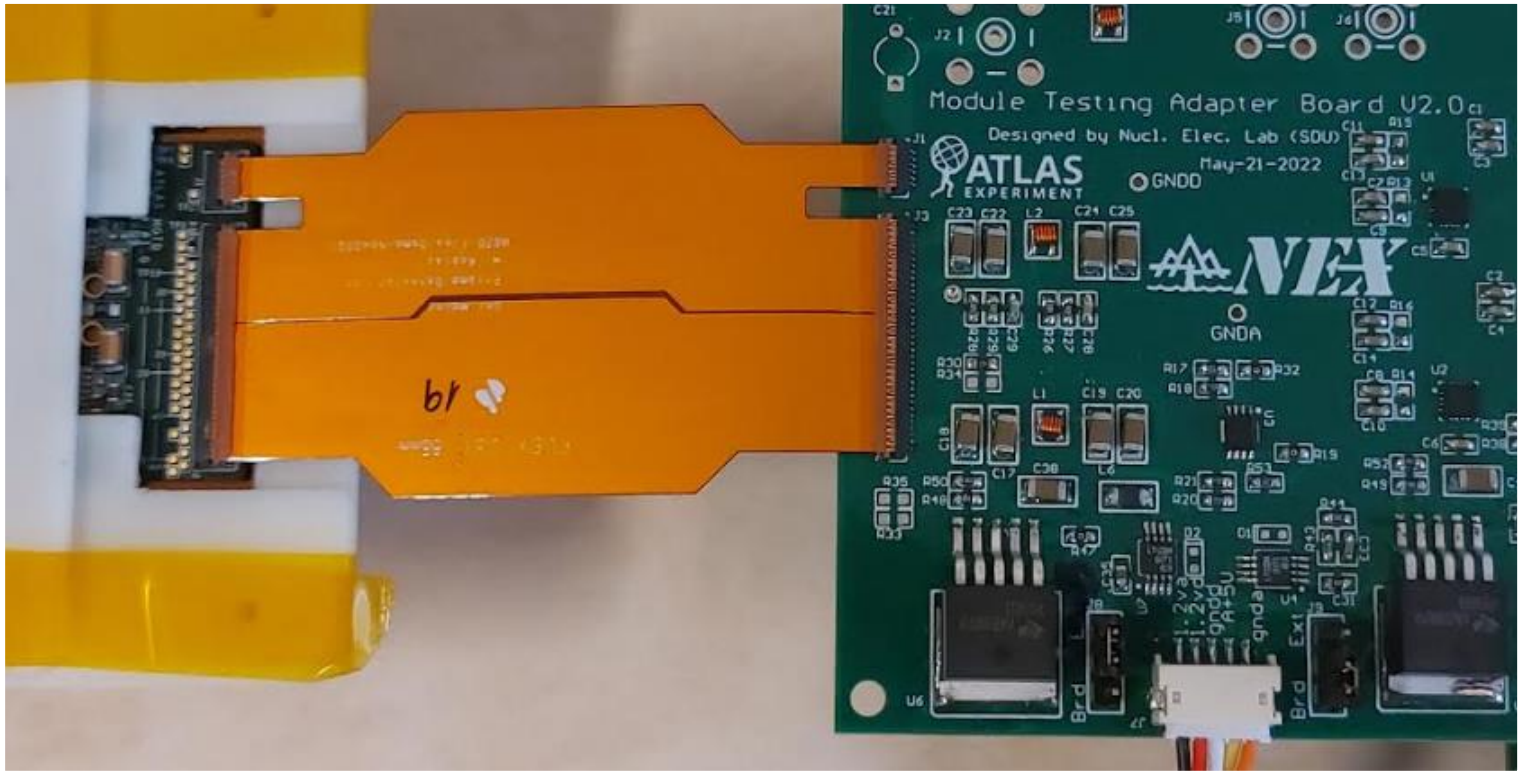




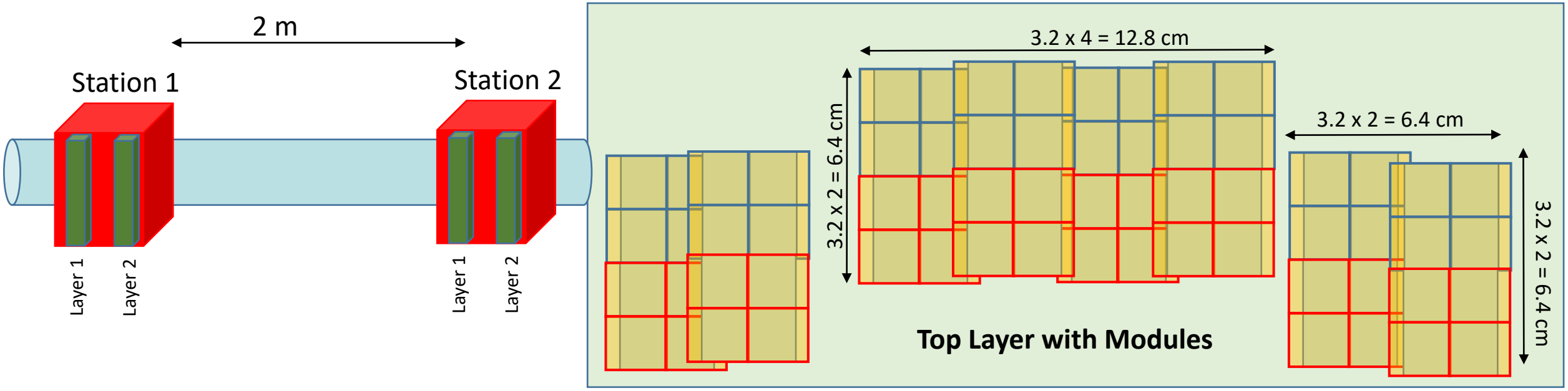


HGTD flex cable





Roman Pots: possible module arrangement



128 ASIC per layer, a total of 512 ASIC (most probably 1024 pixels per ASIC)