Developments at Fermilab

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eRD112/LGAD Consortium Meeting

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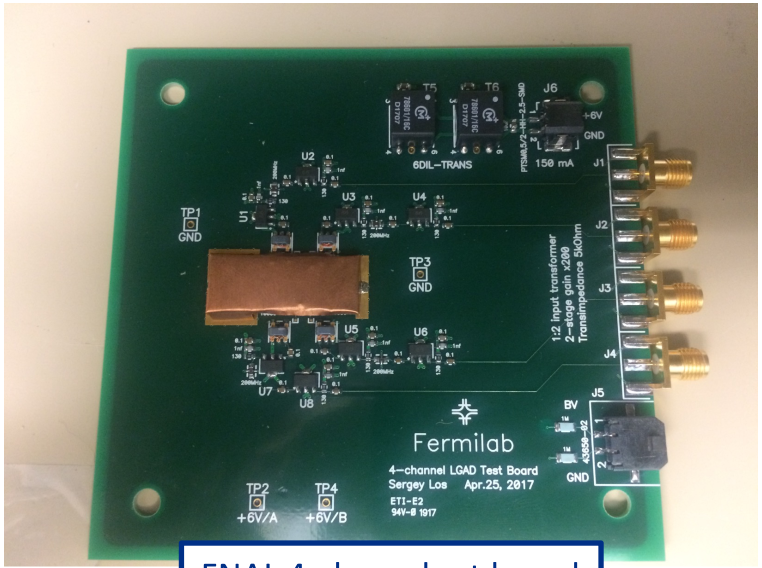
Involvement

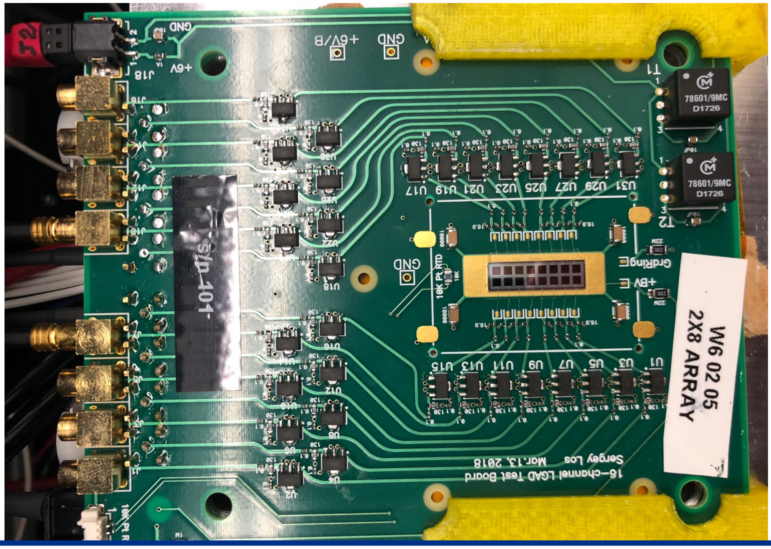
- Have been involved in several areas of AC-LGAD R&D
  - Development of readout electronics for sensor characterization, used widely in many measurements in the community
  - Extensive infrastructure and expertise in testing of prototype LGAD sensors at FTBF and SiDet
  - Development of fast timing ASIC, design of readout electronics, and measurements of performance

Readout electronics for precision timing sensors

- Developed readout boards for the characterization of LGADs
  – 4-,16- and 26-channel boards are a **cost-effective and simple way to test** large channel count sensors
- Several iterations produced and improved over time
  - Have been critical in measurement campaigns for DC-LGADs for CMS Timing detector, and generic R&D on AC-LGAD sensors,



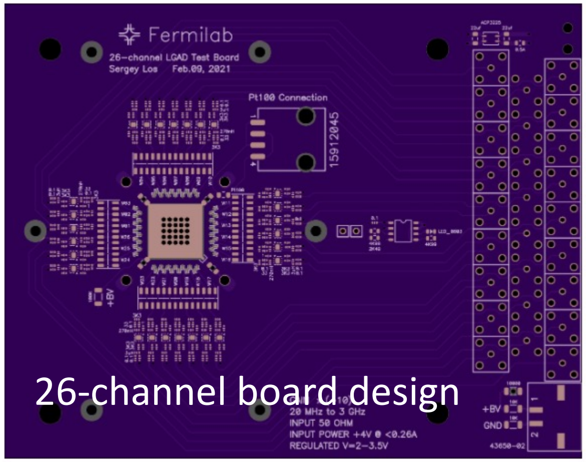
FNAL 4-ch readout board

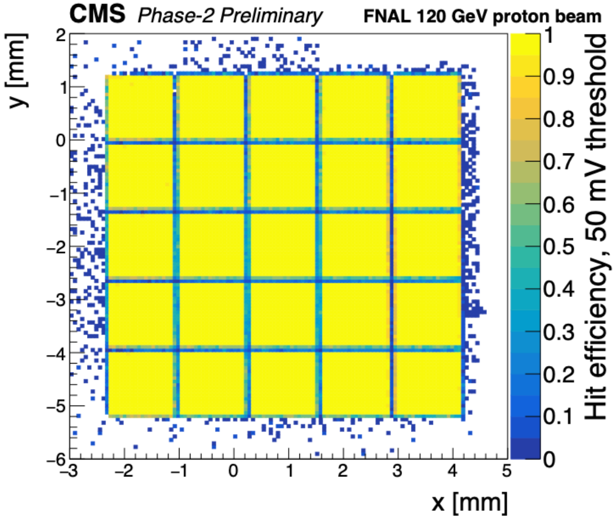


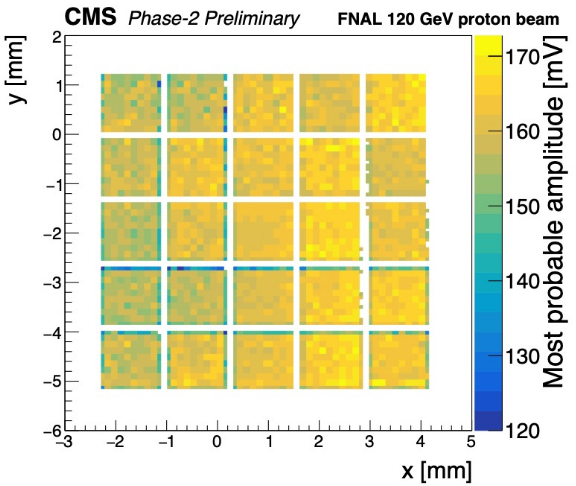
16-ch sensor LGAD on Fermilab readout board

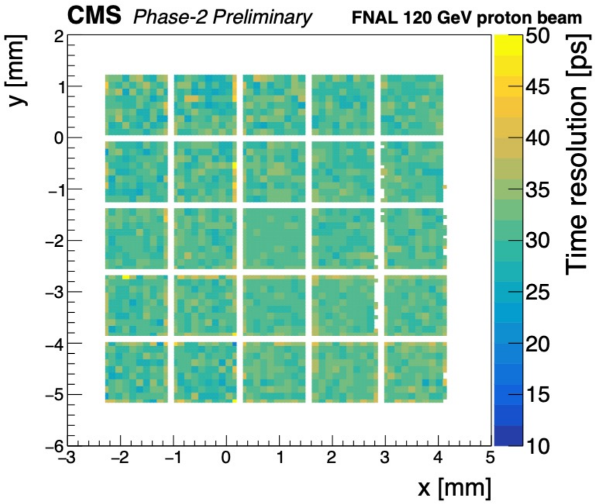
Readout electronics

- New development: low power 26-ch board
  - Goals: Increase the channel count, reduce power consumption, improve time resolution performance
  - Maintain low noise, and low jitter
  - Achieve sensor's intrinsic limitation on time resolution: around 30 ps resolutions (for 50 µm thickness)
- Very good performance measured in beam
  - Have been critical for measurements of large-area AC- and DC-LGAD sensors



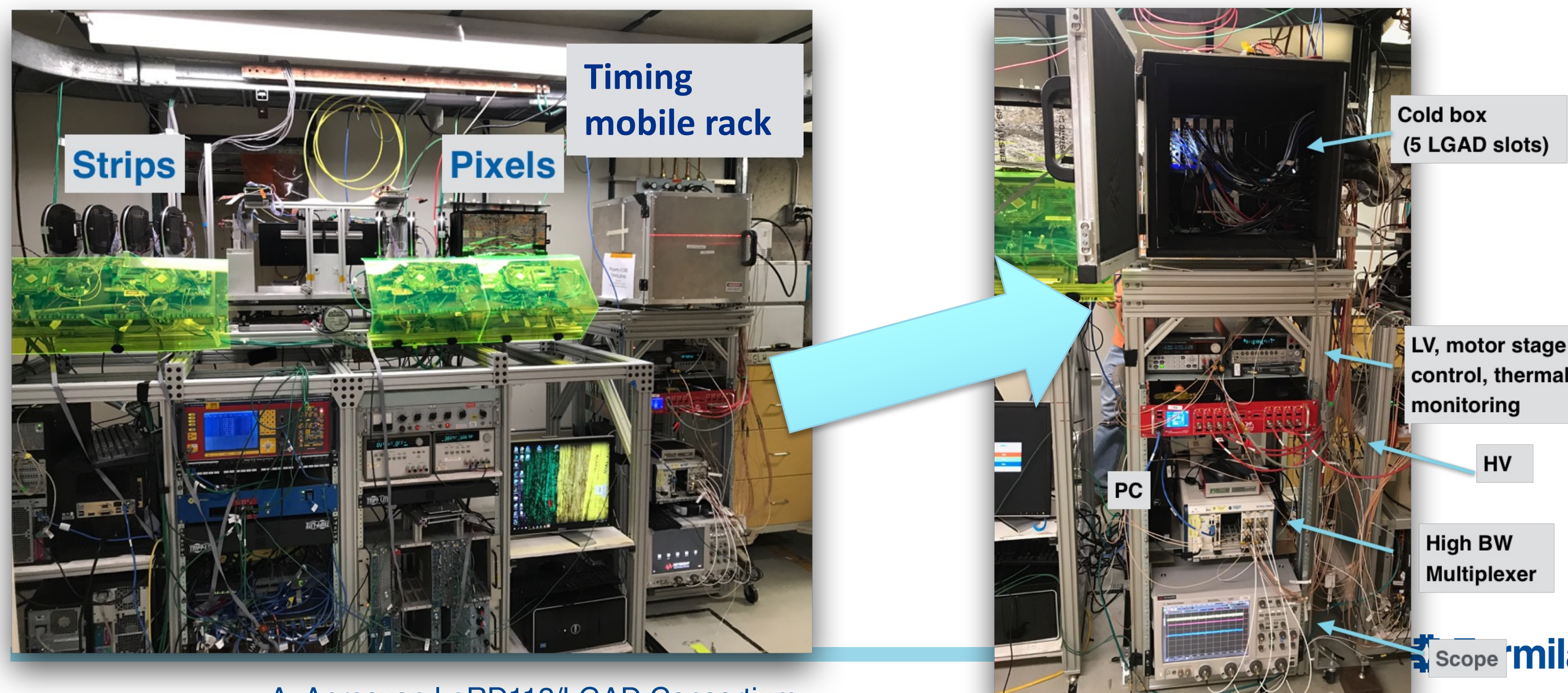






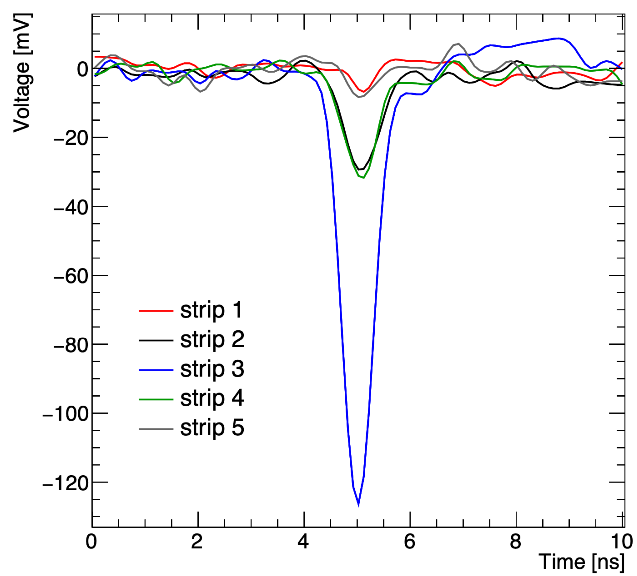
Fermilab 4D-trackers test beam infrastructure

- Permanent setup in FNAL test beam facility (FTBF)
  - Movable: slide in and out of beamline as needed, parasitic use of beam
  - Environmental controls: sensor temperature (-25 C to 20 C), and humidity, monitoring
  - Remote control (stages, HV, LV), logging & reconstruction; $\sigma_T \sim$ 10 ps time reference (MCP)
  - Cold operation of up to 10 prototypes at the same time
  - DAQ: high bandwidth, high ADC resolution scope 4- or 8-channel scope
  - Record 100k events per minute, tracker with ~10 µm resolution



Fermilab 4D-trackers test beam infrastructure

- Several improvements in the timing DAQ, telescope hardware and DAQ
  - 8-channel scope: critical for charge sharing measurements
- Procedure to align DUT with telescope was improved: alignment performed along Z-axis and 3-rotation angles
  - Results in ~5-7 um resolution on DUT



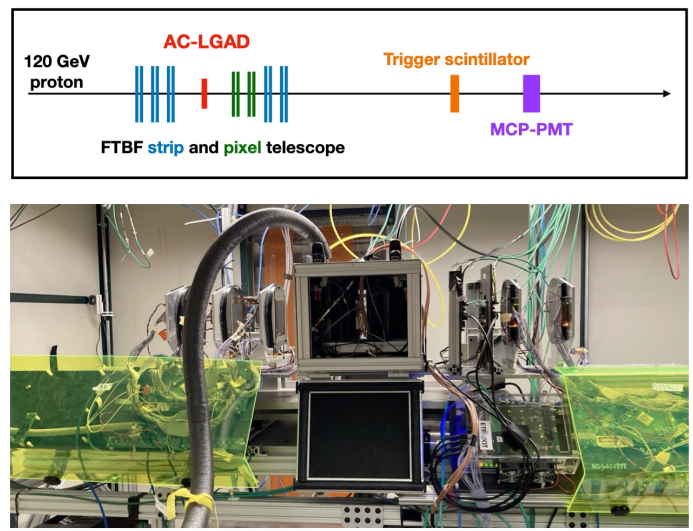
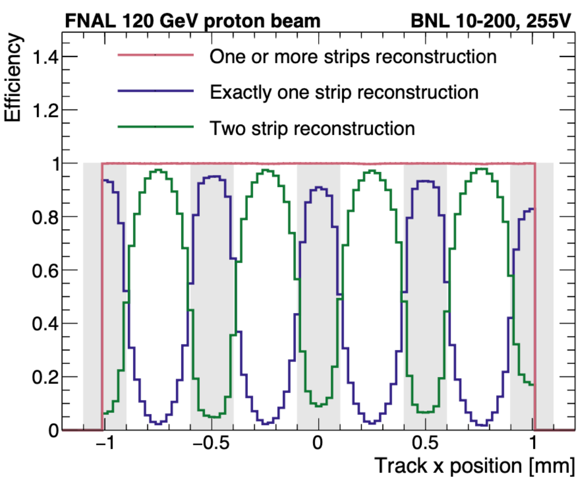
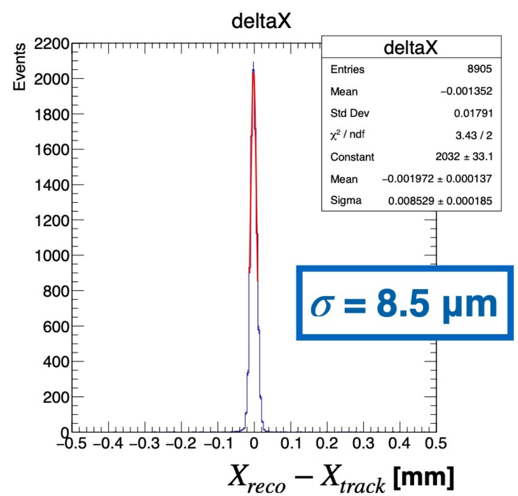


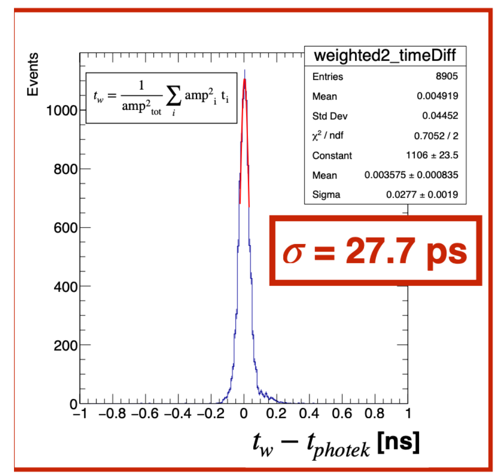
Figure 2: Diagram of the AC-LGAD and reference instruments along the beamline (top). The environmental chamber placed within the FTBF silicon telescope (bottom). The telescope comprises five pairs of orthogonal strip layers and two pairs of pixel layers, for a total of up to 14 hits per track.

AC-LGAD measurements in beams

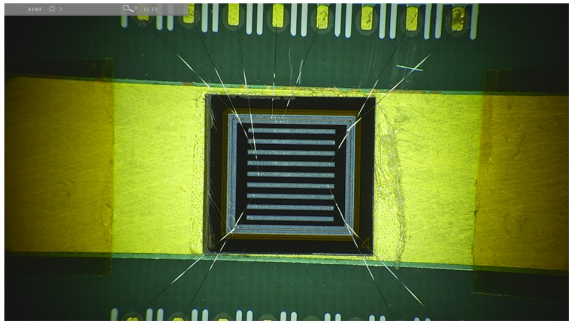
- Multiple collaborative test beam campaigns at Fermilab on measurements of AC-LGAD performance from BNL and HPK
- First demonstration of simultaneous **~5 um and ~30 ps resolutions** in a test beam



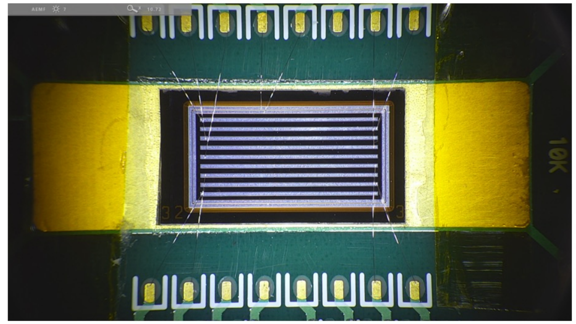




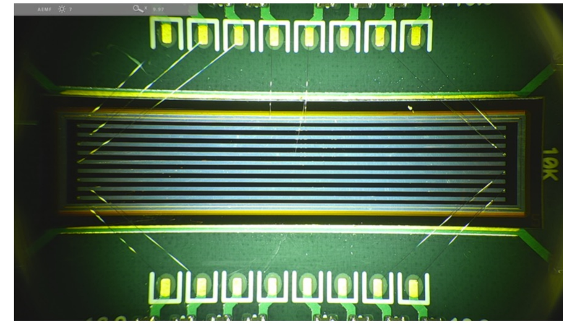
Study of the long AC-LGAD strips



5 mm



10 mm

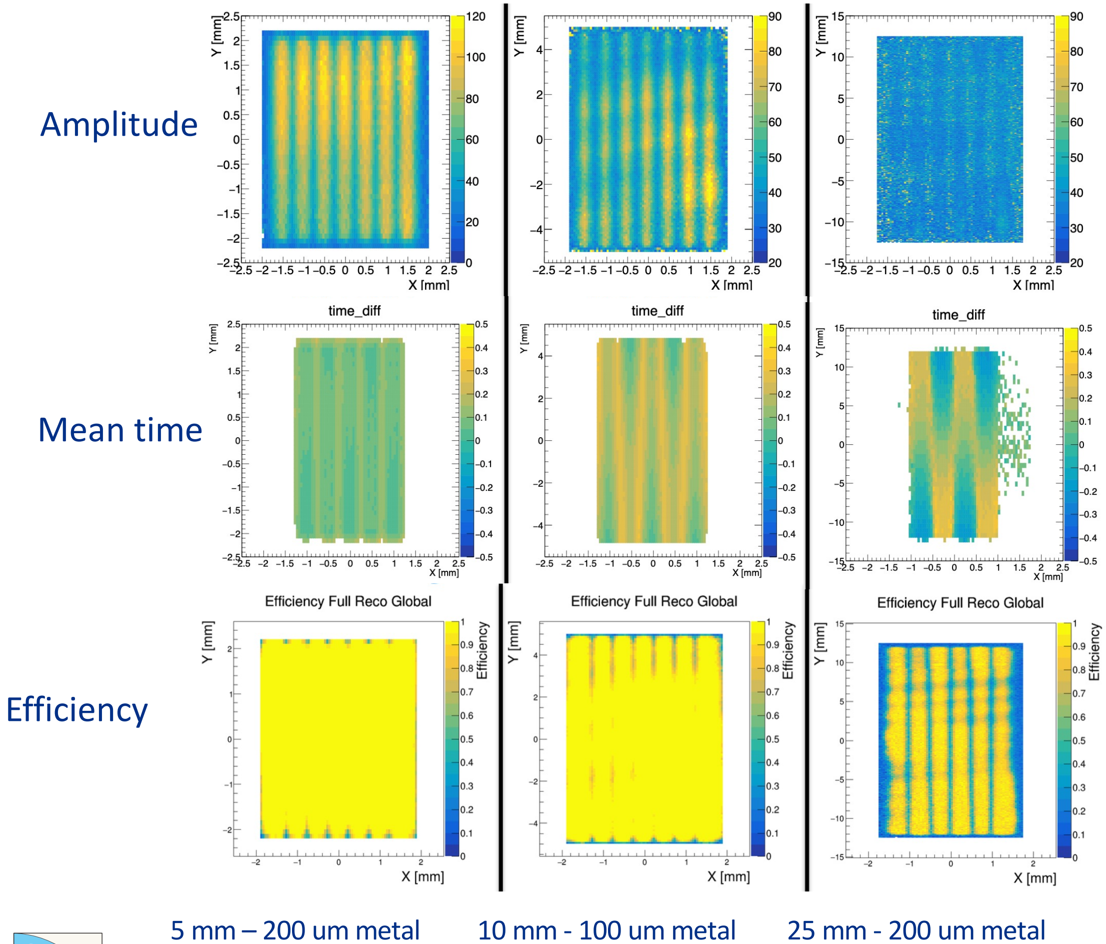


25 mm

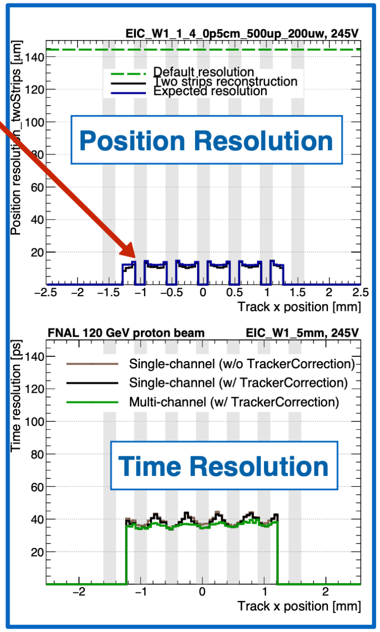
- Studies of large AC-LGAD sensors in beam
  - **Technology demonstrator for 4D-tracking and detectors for EIC**
- Multiple sensors, geometries and designs studied
  - Multi-institutional effort, students and postdocs
- Key insights for larger sensors
  - Gain uniformity is increasingly important
  - Large channel size (capacitance) flattens signal shape
  - Metal vs. pitch size is important for position reconstruction

Study of the long AC-LGAD strips

- Detailed maps of critical parameters of sensors



- **2-strip reconstruction not 100% outside of metal**
- **Can be mitigated with smaller metal**
  - Resolution on metal is metal size / sqrt(12)
  - Metal size of ~80 µm recovers uniform performance
- **Position resolution factor of 10 better than binary readout**
- **Using time delay tracking info can recover good timing resolution**



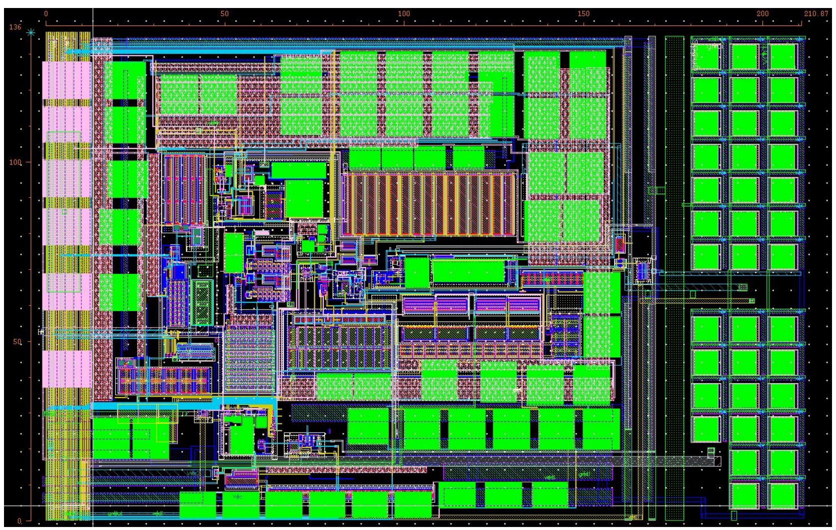
5 mm

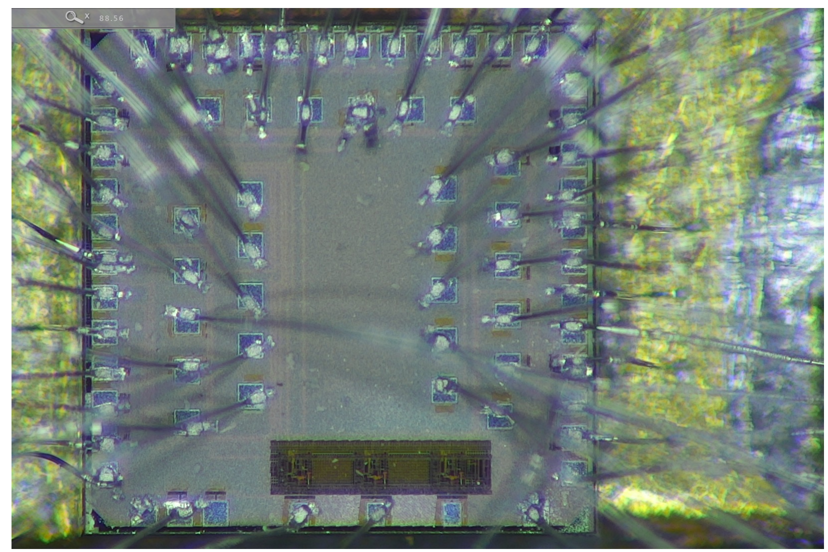
FCFDv0: Fermilab CFD chip v0

- Goals:
  - Develop a robust fast-timing measurement technique for fast detectors
  - 30 ps time resolution or better
  - Easy to use and stable: no corrections, or repeated calibrations and threshold adjustments
  - Very low dead-time after a hit (< 25 ns)
- Our approach:
  - Studied both LE and CFD approaches for AC-LGAD: *“A simulation model of front-end electronics for high-precision timing measurements with low-gain avalanche detectors”*, **NIM A 940 (2019), pp 119-124**
  - Adapt the Constant Fraction Discriminator (CFD) principle for a pixel – when paired with a TDC, *one time measurement* gives the final answer
  - Tailored the v0 design to LGAD requirements, as a demonstrator,
  - General principle could be useful for other applications, e.g. AC-LGAD, or LAPPD

FCFDv0

- First version of the chip to test and study the approach
  - Only analog output to measure the performance of the CFD approach
  - Measurements first performed using the internal charge injection circuit

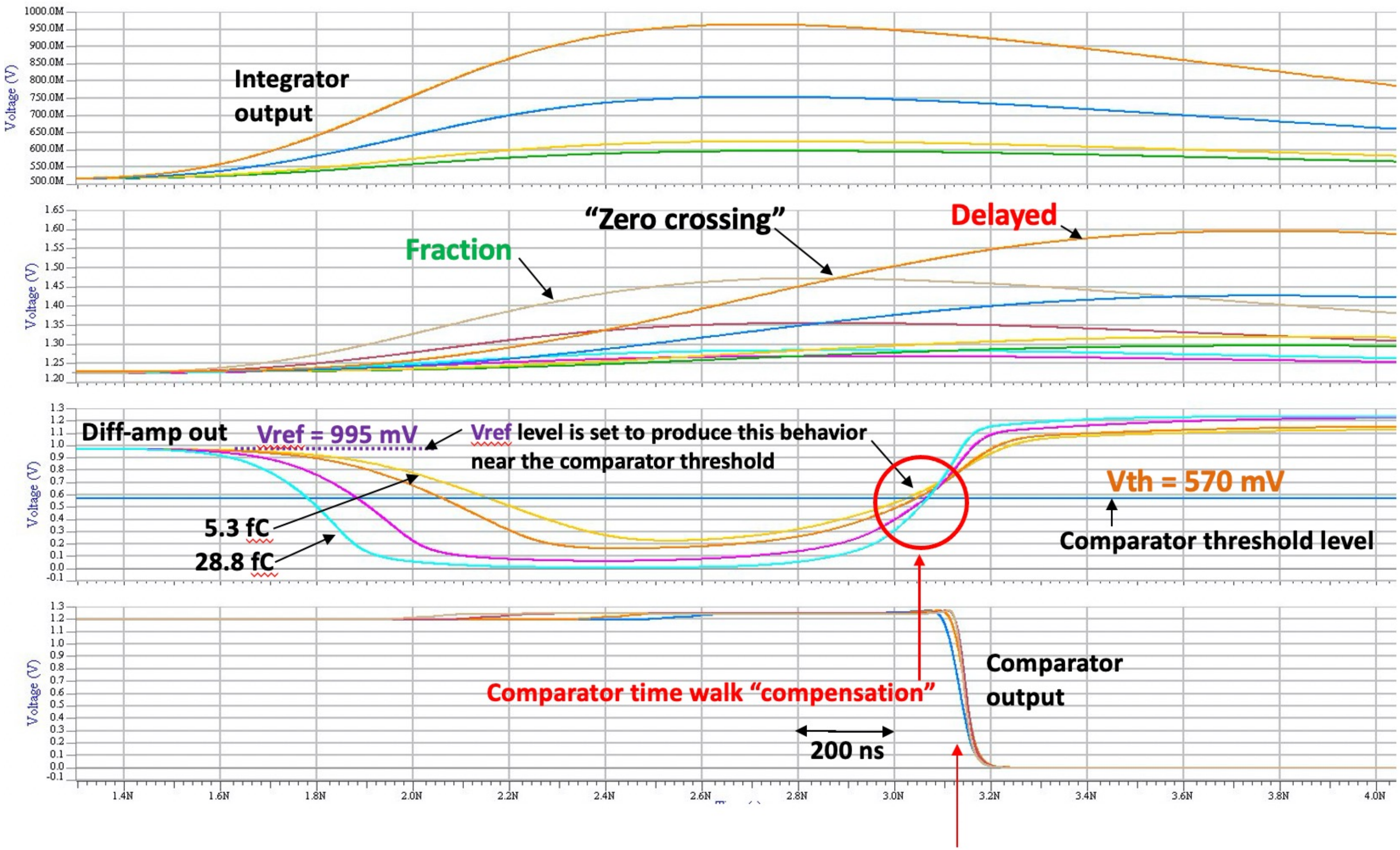




Simulation

Apply LGAD-like charge pulse to FCFD0 input.

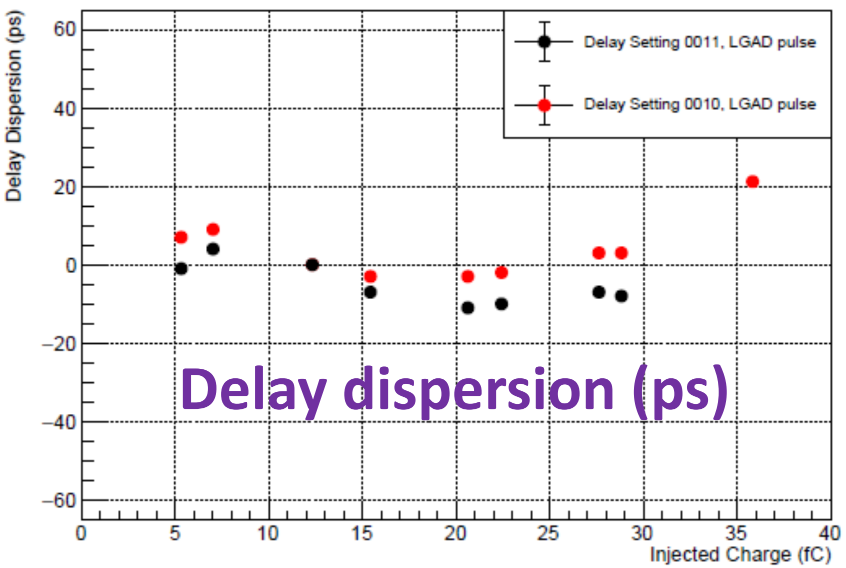
Inject 4 different amplitudes: Qin = 5.3 fC, 7.0 fC, 15.3 fC, 28.8 fC

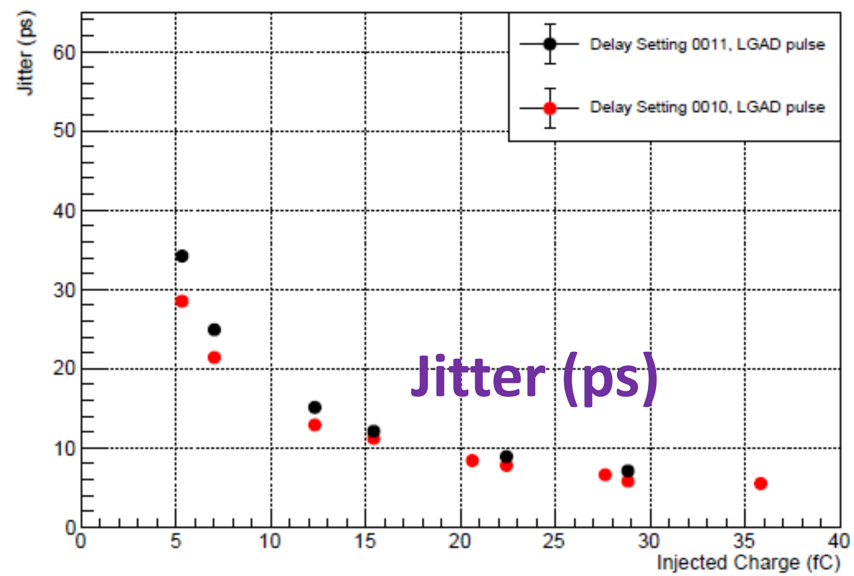


Comparator output has same delay for a range of input amplitudes

Testing with internal charge injection

- Measured delay dispersion and jitter vs. input charge for two different power modes
  - https://indico.cern.ch/event/1019078/contributions/4443948/attachments/2277824/3938152/FCFD0_TWEPP_talk.pdf

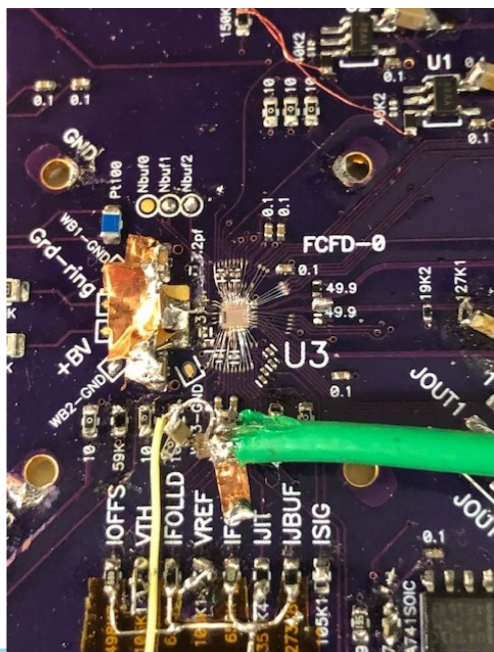


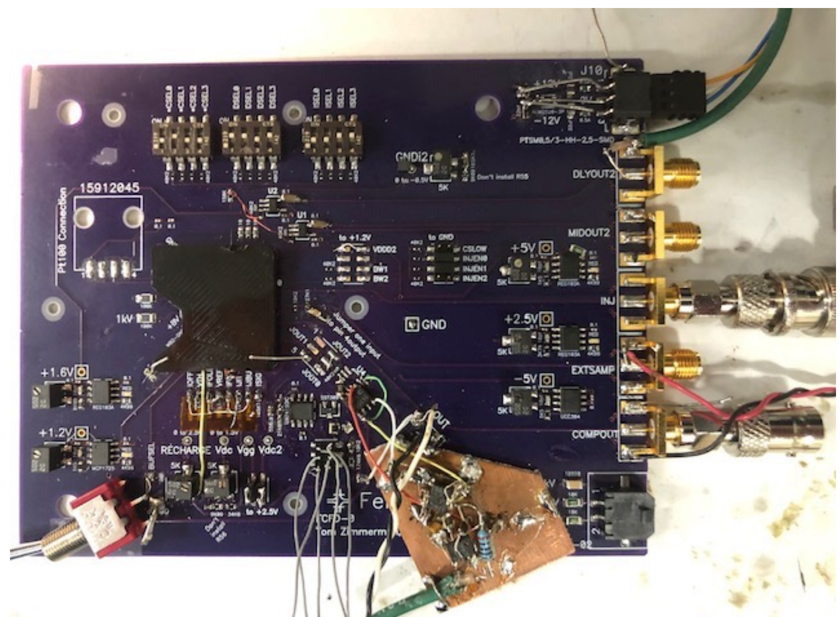


Negligible time-walk, intrinsic jitter around 8 ps at 30 fC

Testing with LGAD signals

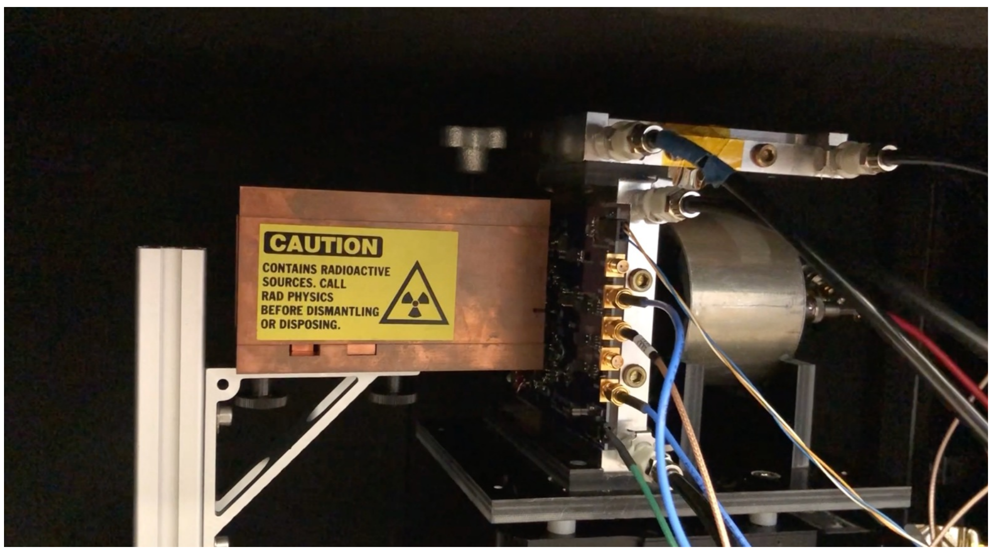
- Characterization of FCFDv0 with beta source and test beam
  - Designed dedicated board for measurements with LGADs
  - On-board regulators for charge injection, switch ON/OFF analog buffers
  - SMA-output of the comparator and analog buffer
- Wirebond LGAD sensor of CMS-size pixels (1.3x1.3 mm^2)



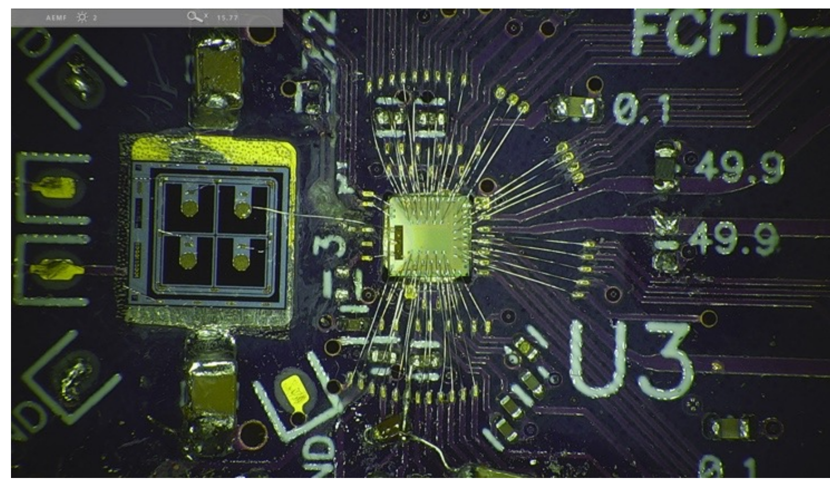


Beta-testing setup

- Board with sensor mounted inside environmental chamber in SiDet
- Test with IR laser and β-source,
  - Test beams to follow when beam returns this Winter



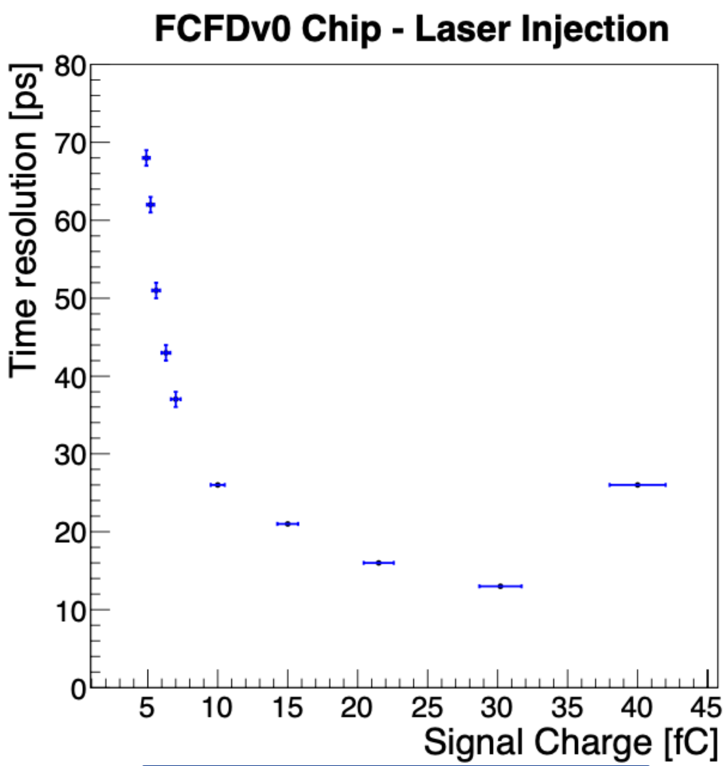
Board mounted with β-source



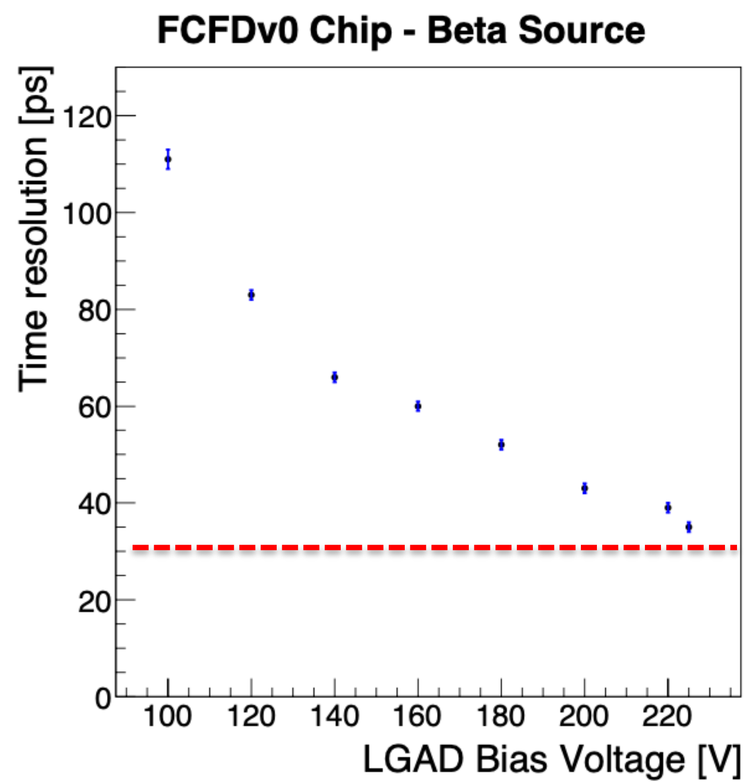
FCFD0 chip mounted to LGAD

Timing ASIC with CFD

- Measurements with laser and beta-source confirm the excellent expected time resolution



Time resolution with 1.3x1.3 mm^2 LGAD sensor



Time resolution with 1.3x1.3 mm^2 LGAD sensor

Next steps for FY23

- Develop the next version targeting EIC AC-LGADs
  - Focus on AC-LGAD readout which needs both amplitude and timing information from each channel
  - Multichannel chip for AC-LGAD strip detector, 10 channels
- Preliminary specs from our studies of AC-LGADs
  - Need to clarify the specs more precisely, measurements on CV for EIC spec AC-LGAD ongoing

Min Charge	*Max Charge*	*Min MPV Charge*	*Max MPV Charge*	*Capacitance*	*ADC Resolution*
2 fC	*64 fC*	*15 fC*	*25 fC*	*0.5-10 pF*	*10%*

Summary

- Good performance for the first generation CFD-chip produced in TSMC 65nm technology node
  – Precise measurements and calibrations of the chip on a bench, stable operations, low dead time

- Development of the next version is starting, targeting specifically AC-LGAD signals to achieve good timing and position resolutions

- Budget request for FY23: $80k
  – MPW production cost of the chip, and associated testing boards